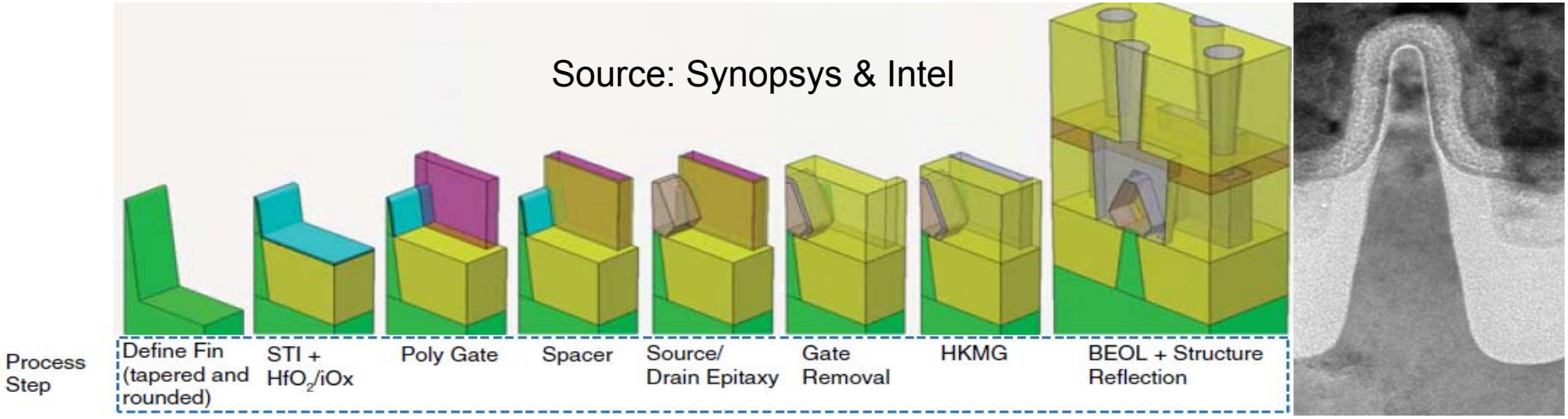
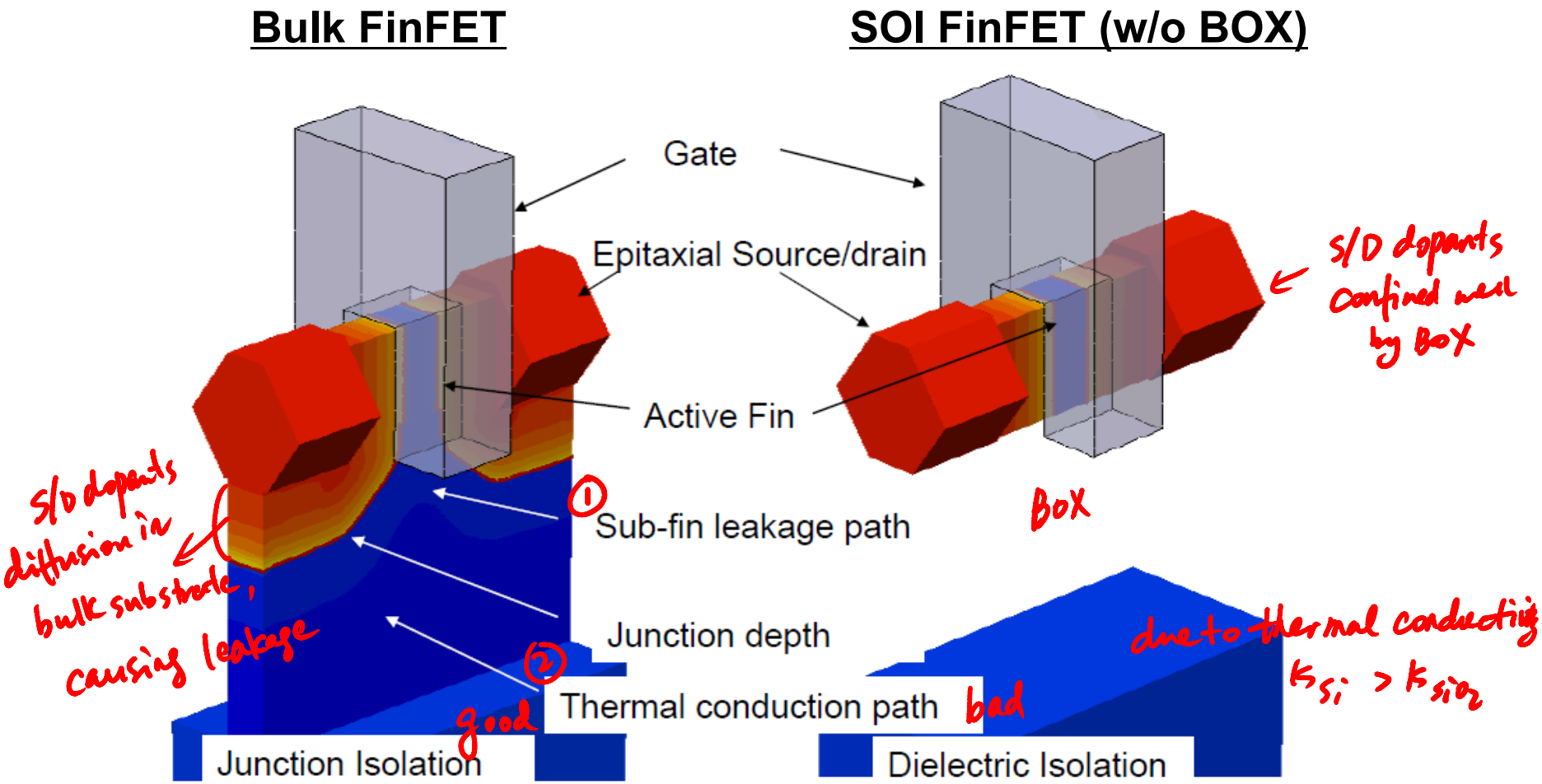


Lecture 7

- Thin-Body MOSFET's Process I
  - SOI *vs*. Bulk FinFETs
  - Fin Patterning Techniques
  - High-κ/Metal Gate Technologies

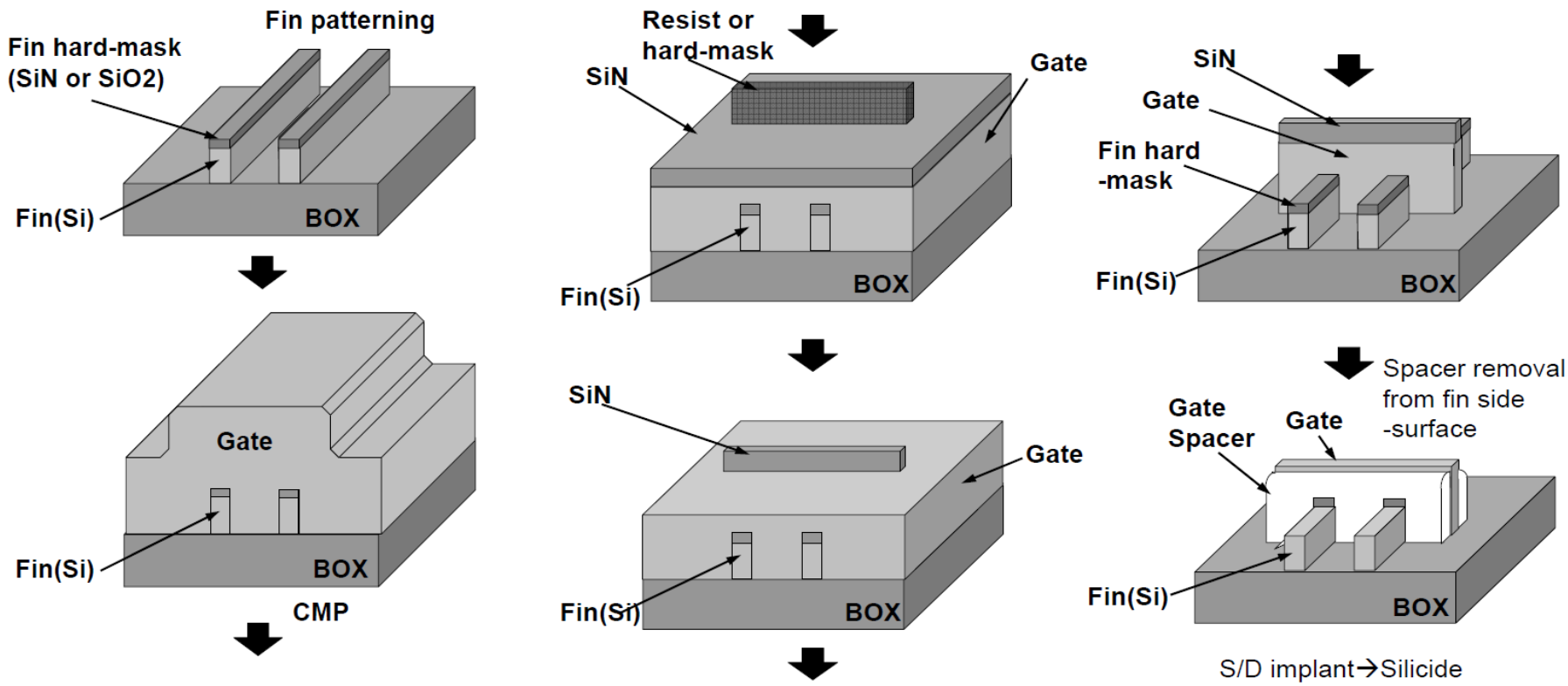
<u>Reading</u>: multiple research articles (reference list at the end of this lecture)

SOI *vs*. Bulk FinFET: Overall Structure



T. Hook (IBM), FDSOI Workshop (2013)

SOI FinFET Process Flow



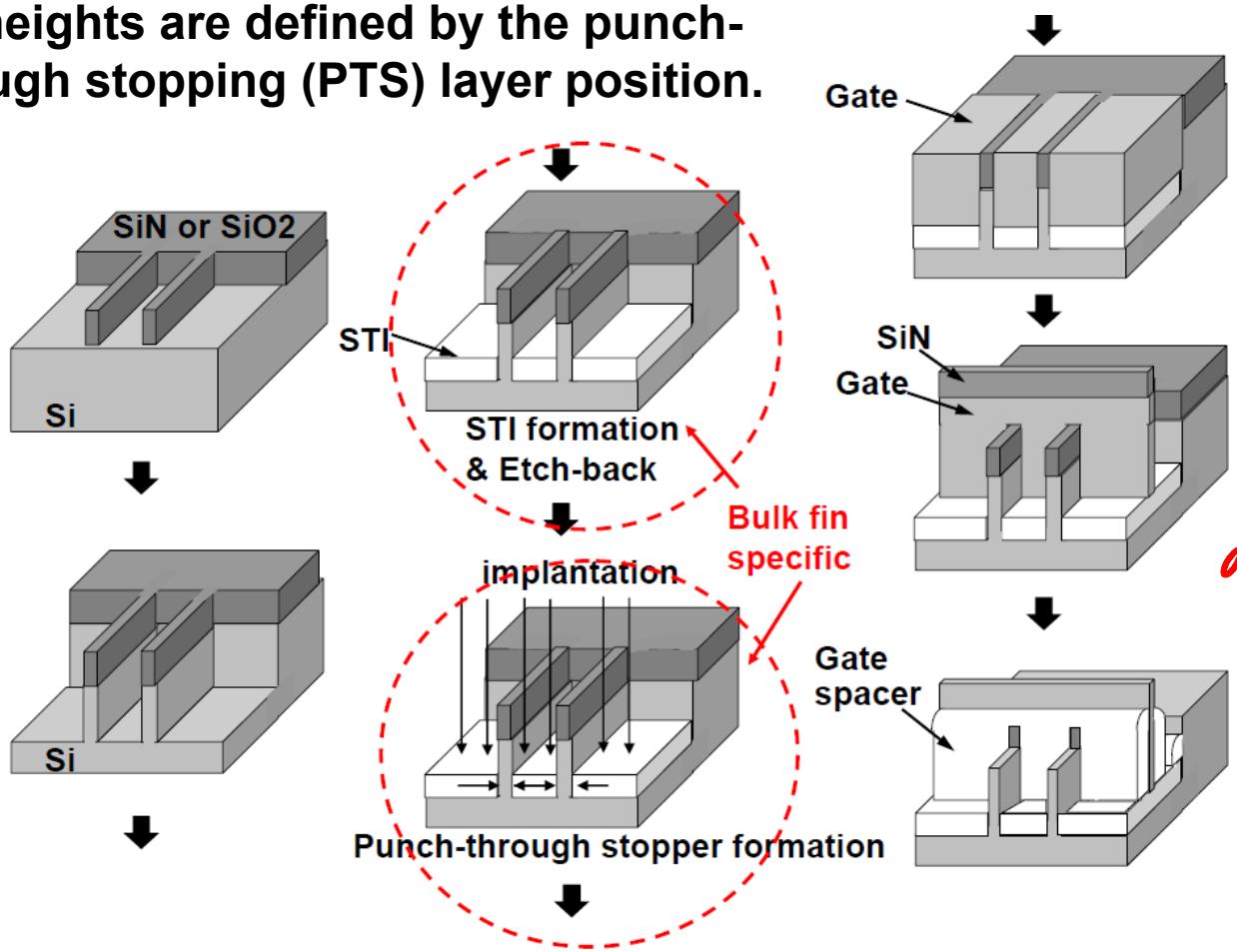
- Fin heights are defined by the SOI film thickness.
- Higher (SOI) substrate cost; yet cheaper doping/implantation cost.

no need for HALO, retrograde well isolation doping
*(LDD as well)

A. Yagishita (Toshiba), SOI Short Course (2009)

Bulk FinFET Process Flow

- **Fin heights are defined by the punch-through stopping (PTS) layer position.**



Fin height (H_{Fin}) defined by Etching + STI refilling

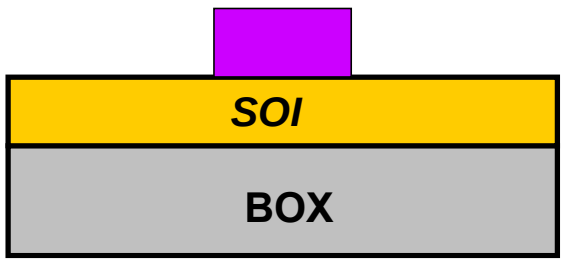
Multiple doping steps required
1) HALO OR Retrograde → PTS
2) Well Isolation

A. Yagishita (Toshiba), SOI Short Course (2009)

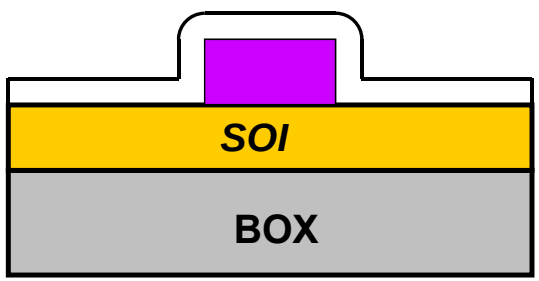
Fin Patterning

Spacer Lithography
a.k.a. Sidewall Image Transfer (SIT)
or Self-Aligned Double Patterning (SADP)

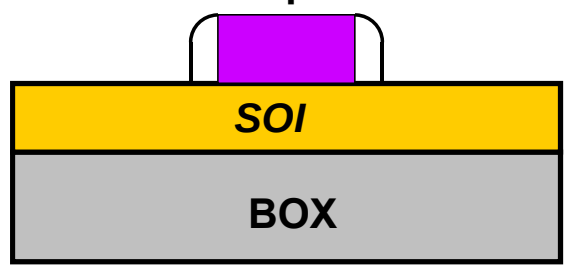
1. Deposit & pattern sacrificial layer



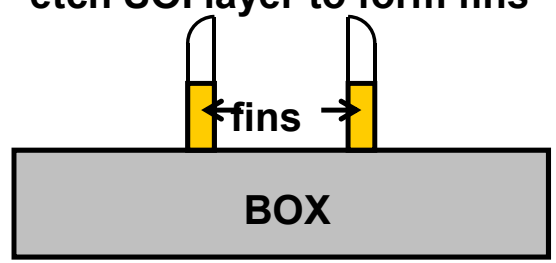
2. Deposit mask layer (SiO_2 or Si_3N_4)

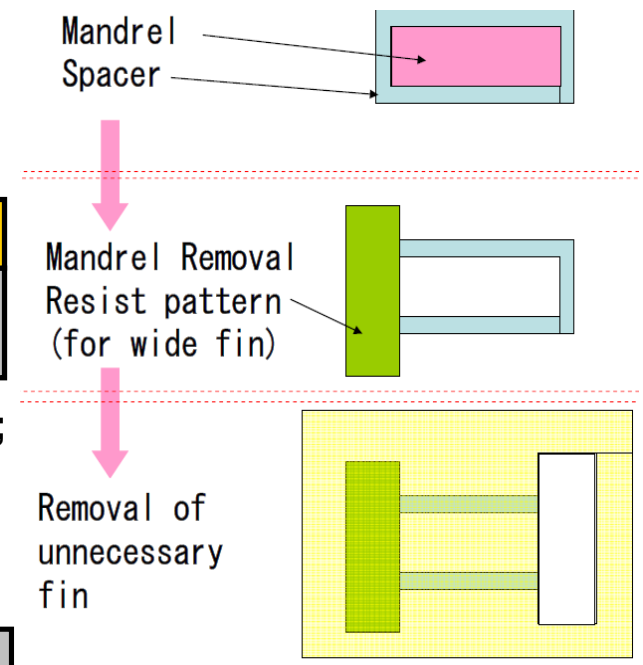


3. Etch back mask layer to form "spacers"



4. Remove sacrificial layer; etch SOI layer to form fins

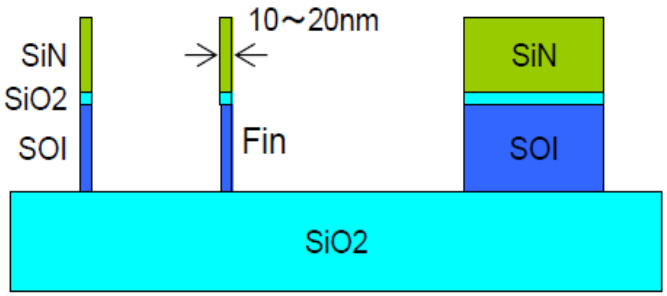


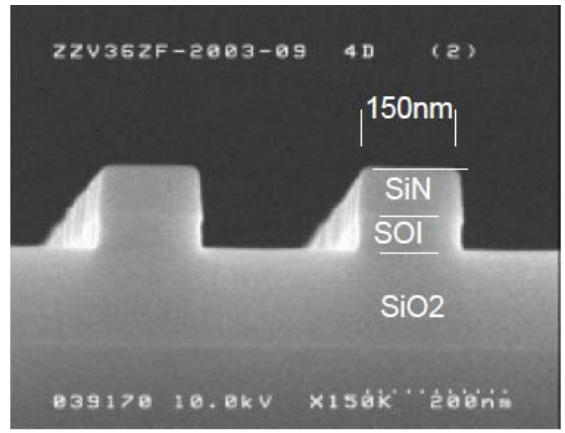


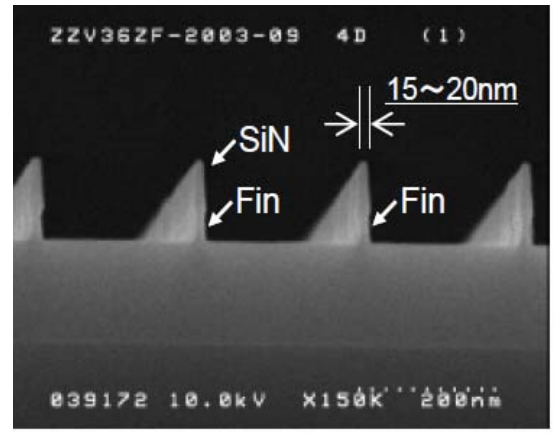
- **Note that fin pitch is 1/2× that of patterned layer**
- **Extra lithography steps required to etch the unused fins.**

Benefit on Multiple Device Pitch

- **By using spacer lithography technique, multiple fin pitches can be implemented using a single lithography step.**

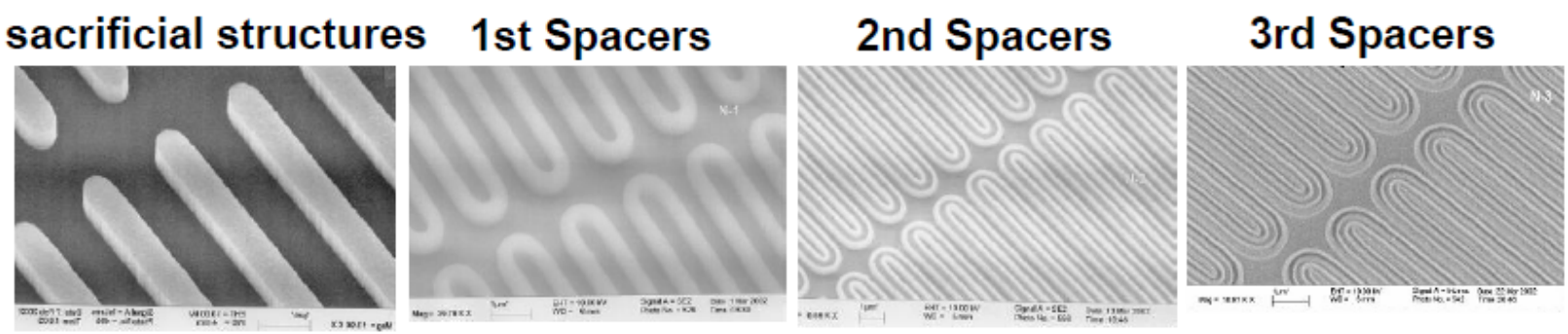






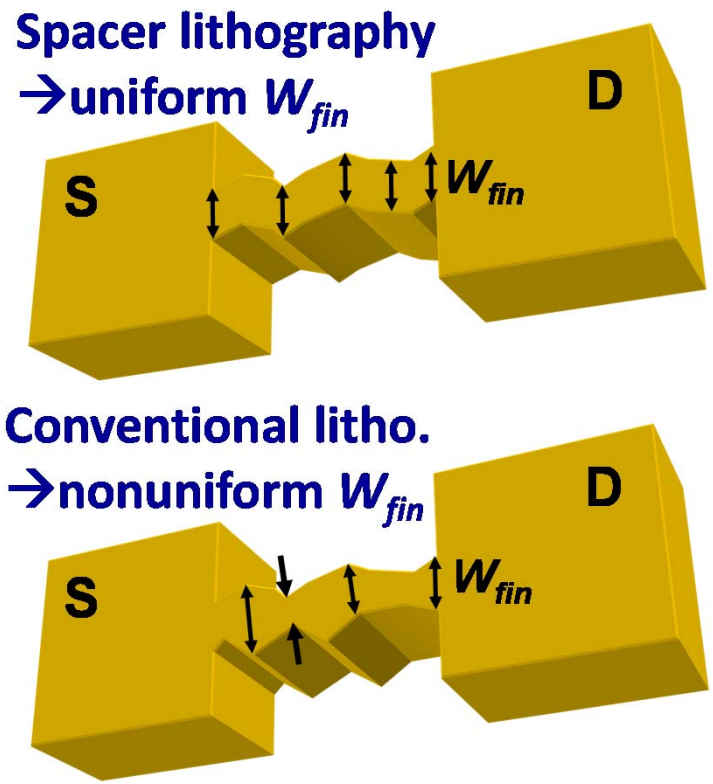
- **2^n lines after n^{th} lithography !**

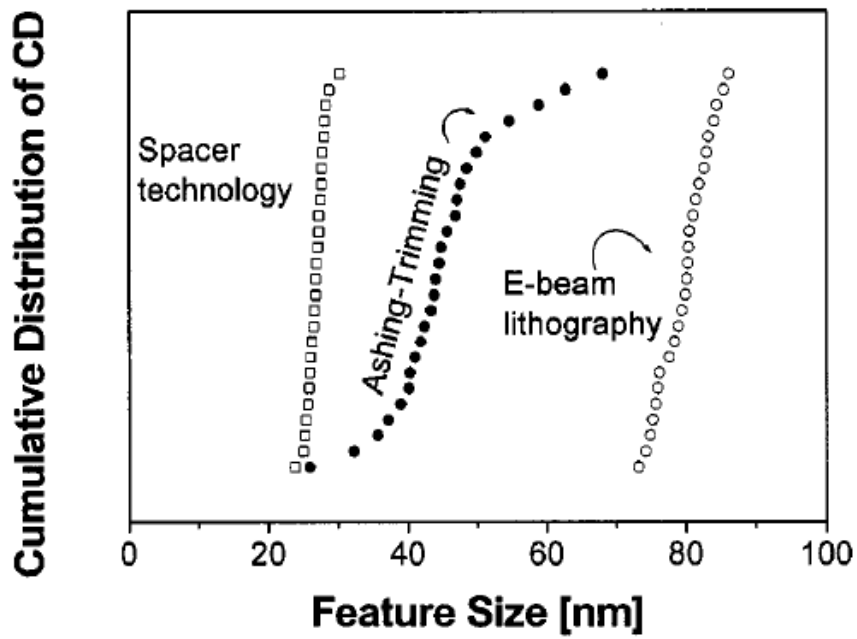
A. Yagishita (Toshiba), SOI Short Course (2009)



Benefit on Fin Edge Roughness

Y.-K. Choi, IEDM (2002)



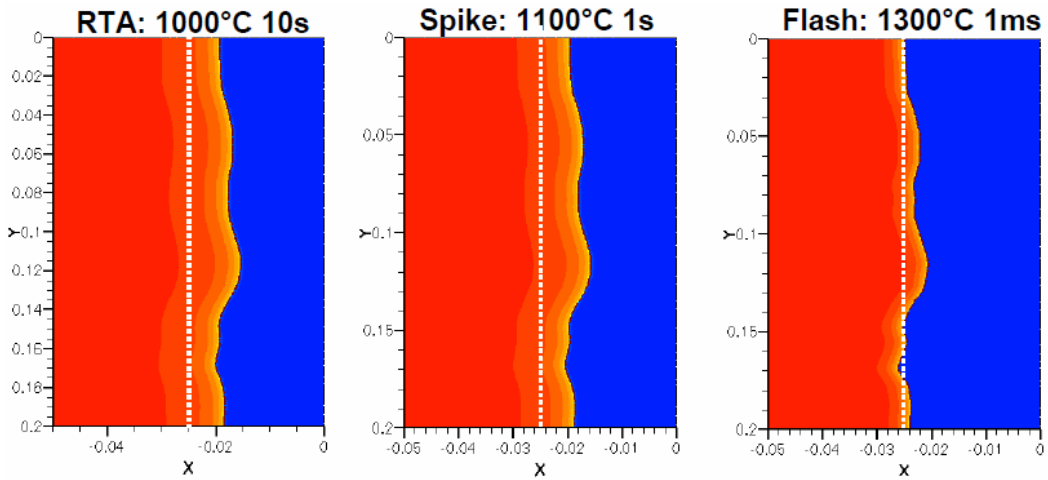


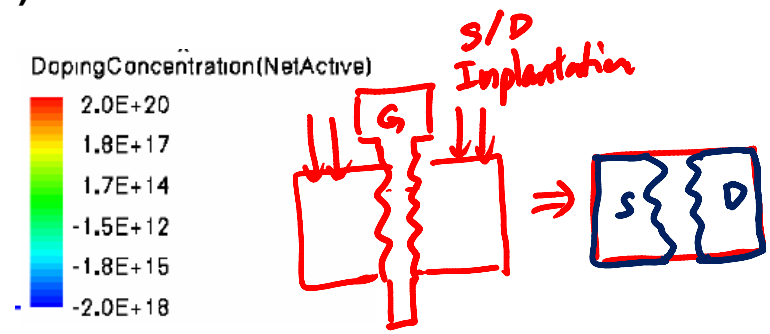
Y.-K. Choi, IEDM (2002)

- Spacer lithography technique provides more uniform fin width than the conventional lithography, due to $\sigma_{litho} > \sigma_{CVD}$

Benefit on Gate Edge Roughness

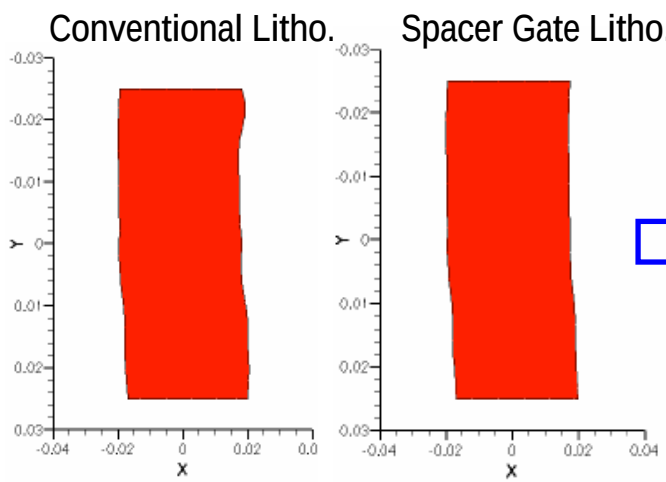
X. Sun, TSM (2010)



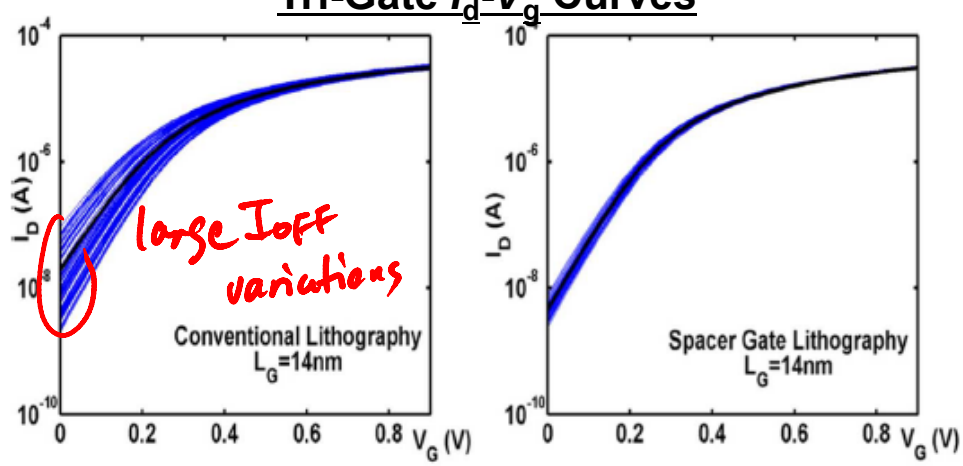


3keV 3E14cm^{-2} As implant through 10nm liner

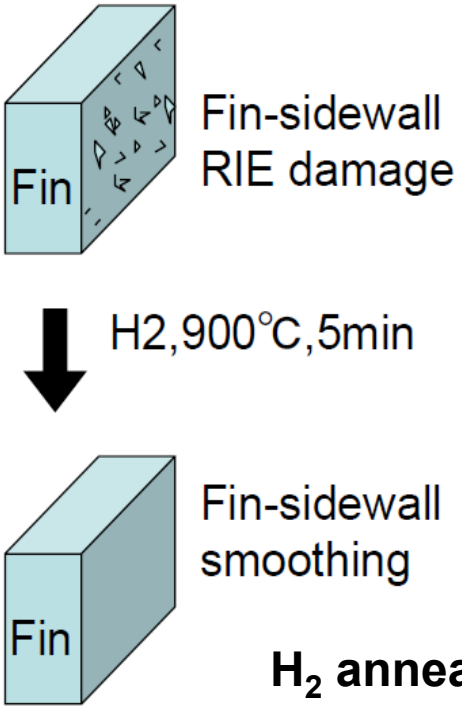
Less diffusion → Worse junction roughness



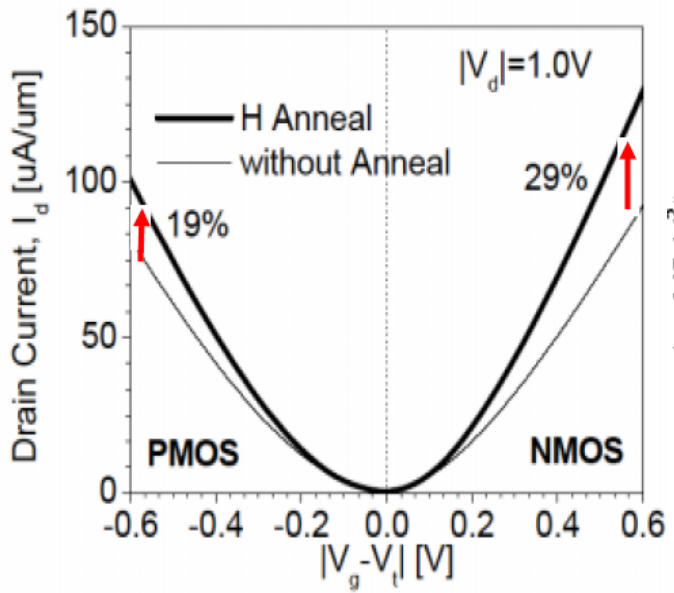
Tri-Gate I_d-V_g Curves



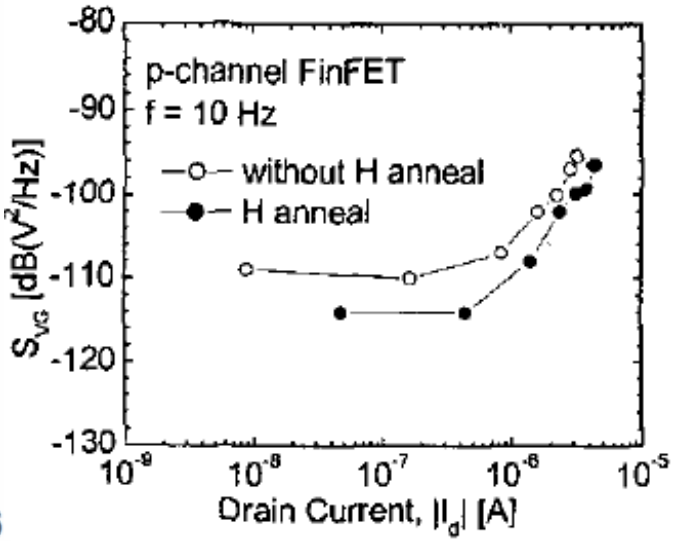
Fin Sidewall Damage Removal by H_2 Annealing



Mobility Improvement by H_2 Annealing

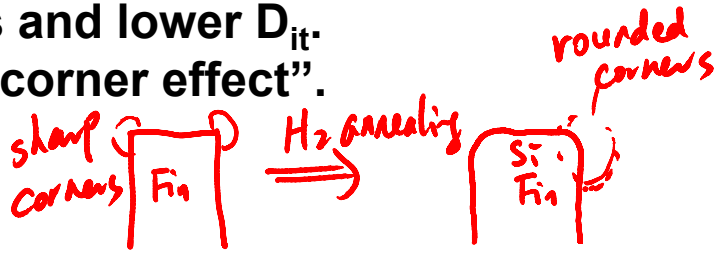


Equivalent Gate Input Noise



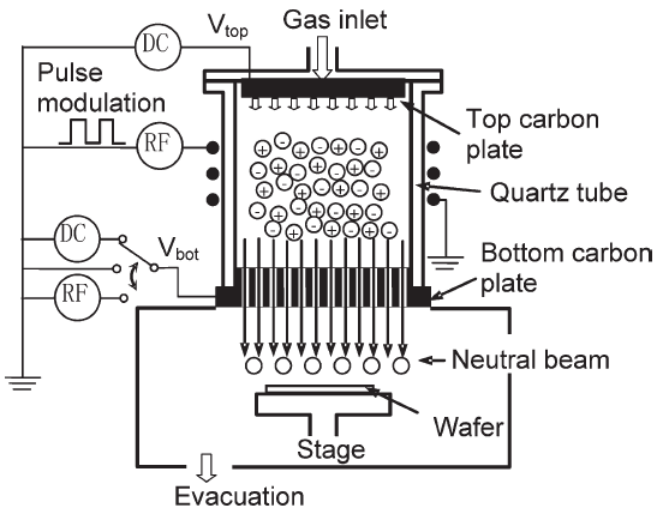
H_2 annealing causes Si atoms remigration at fin sidewall surfaces

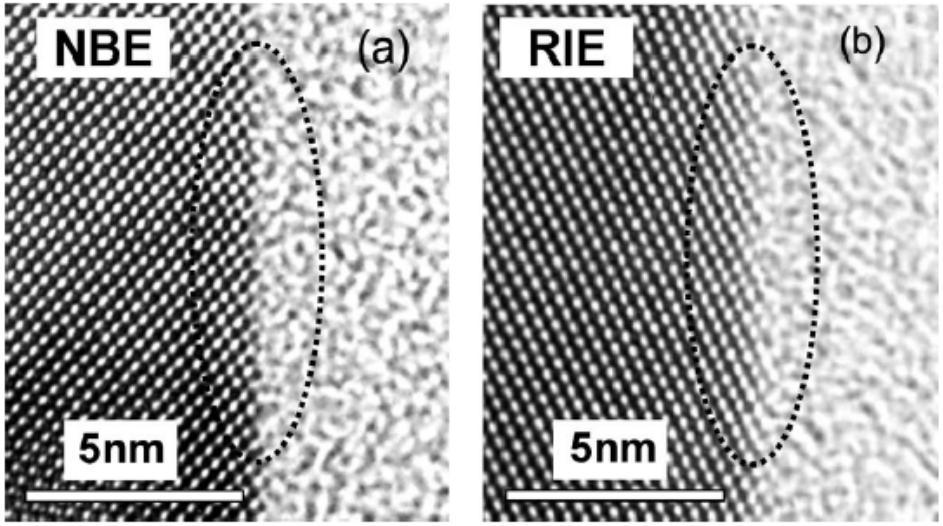
- **provides smaller surface roughness and lower D_{it}.**
- **reduces shape corners to mitigate "corner effect".**

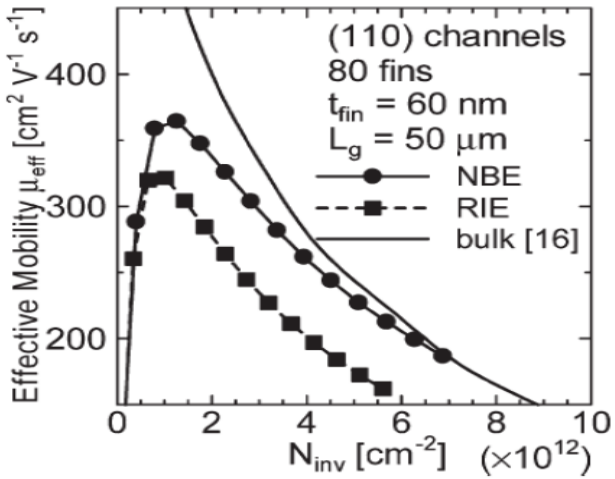


Y.-K. Choi, IEDM (2002)

Fin Sidewall Damage Removal by Neutral Beam Etching





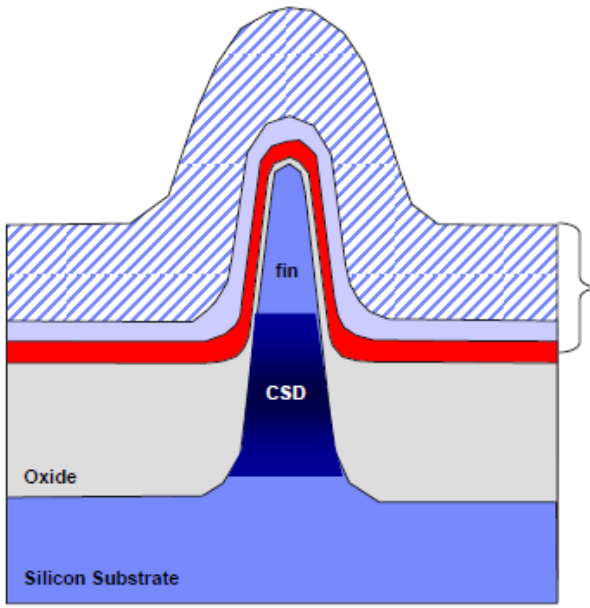


- **Neutral Beam Etching: negative ions in the plasma can be neutralized by passing through the carbon aperture.**
- **TEM picture shows more abrupt fin/oxide interface after NBE → Lower D_{it}**
- **Higher fin mobility w/ NBE**

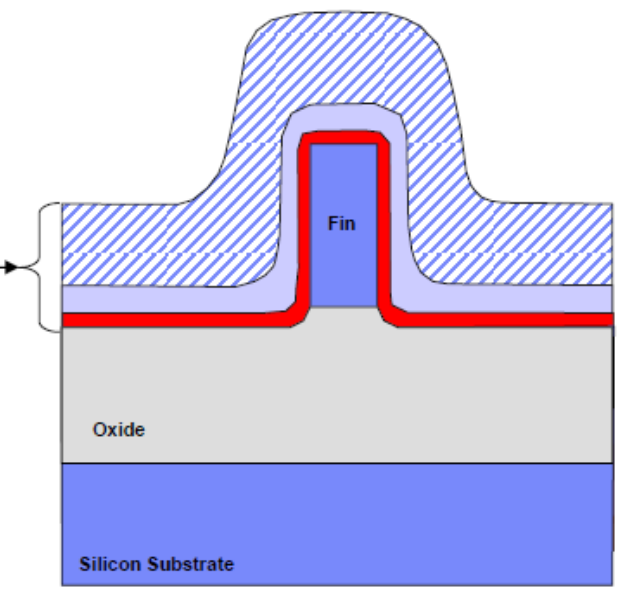
K. Endo, TED (2006)

SOI *vs*. Bulk FinFET: Isolation

Bulk FinFET



SOI FinFET (w/o BOX)

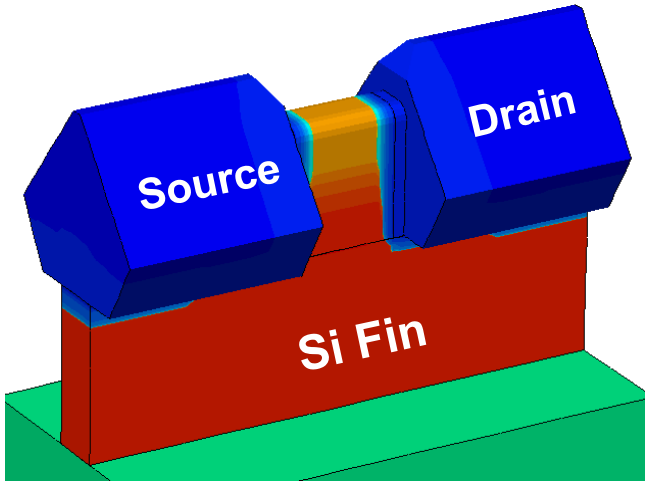


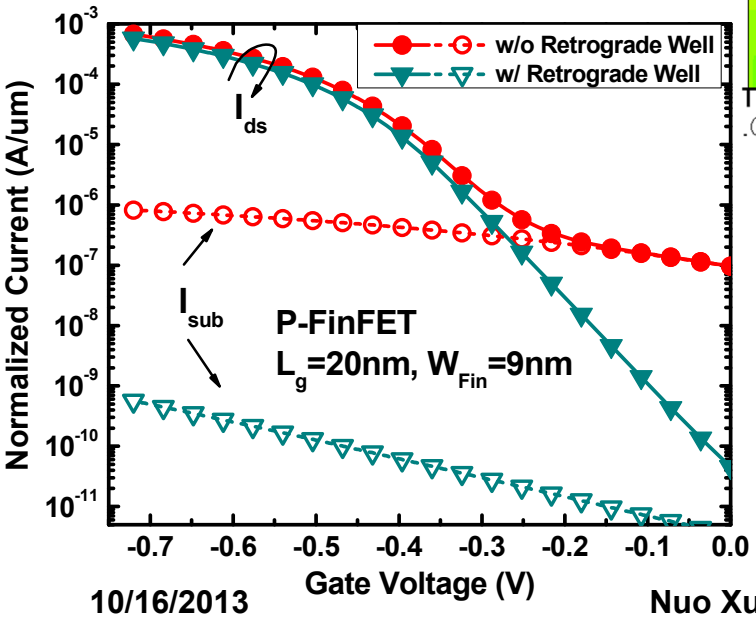
- Retrograde-well doping required as punch through-stop (PTS) layer. combined
- HALO is also often adopted.
- Tapered fin shape due to STI process.

- No doping process needed to avoid PT.
- Rectangular fin shape.

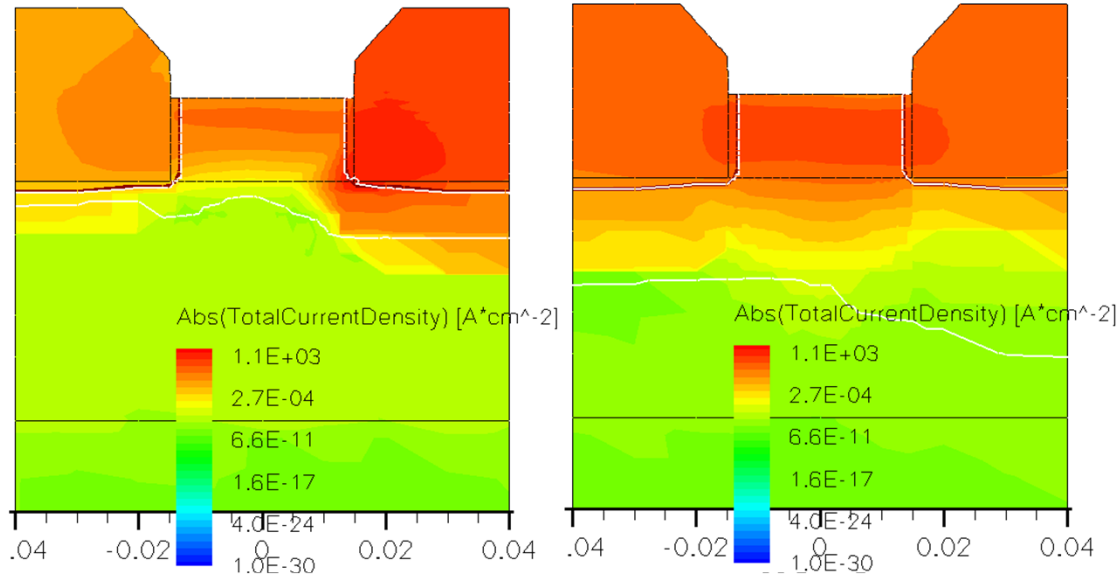
T. Hook (IBM), FDSOI Workshop (2013)

Impacts of Retrograde Well Doping



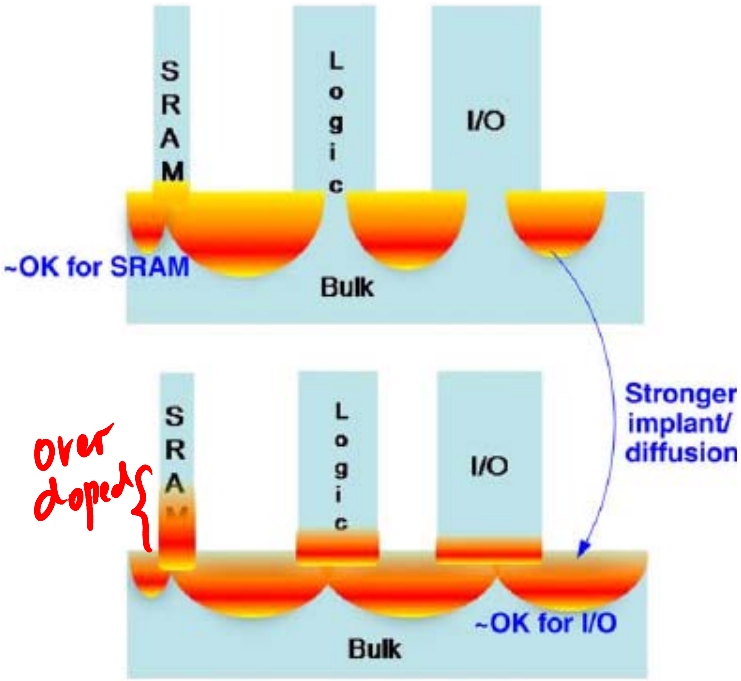


w/ Retrograde Well Doping **w/o Retrograde Well Doping**



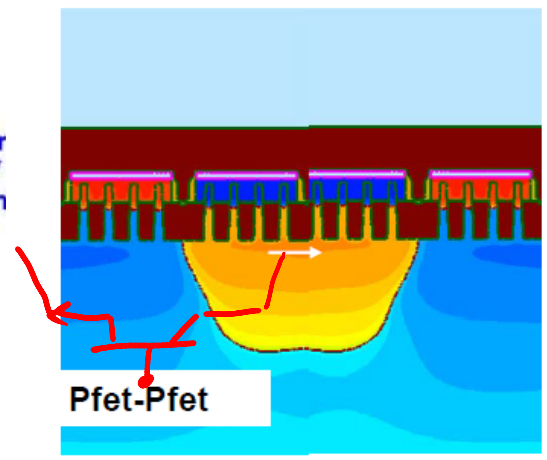
- **Even with the finite steepness of retrograde well doping (~15nm/dec in Si), it is still preferred to insert the doping peak around the fin base, causing some level of performance degradation in the fin.**

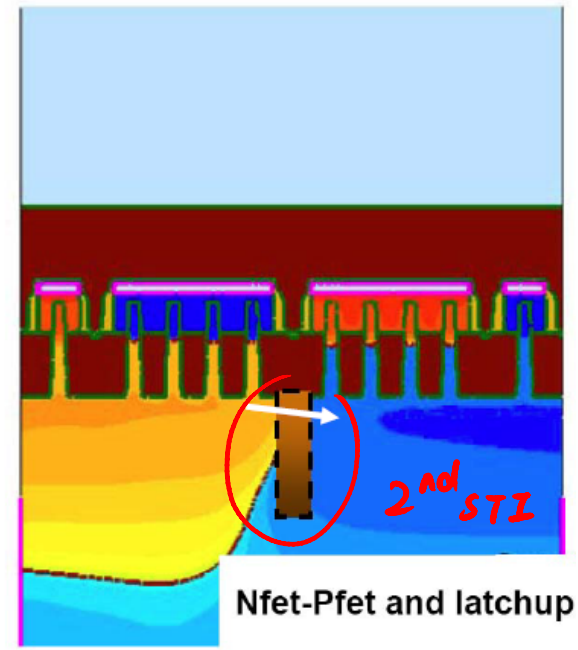
More Issues for Bulk FinFET Isolation



J. G. Fossum, SSE (2010)

Bulk FinFETs require
- Junction isolation masks and implants
- Well contacts
- Latchup prevention measures
  - Second STI
  - Heavily doped substrate



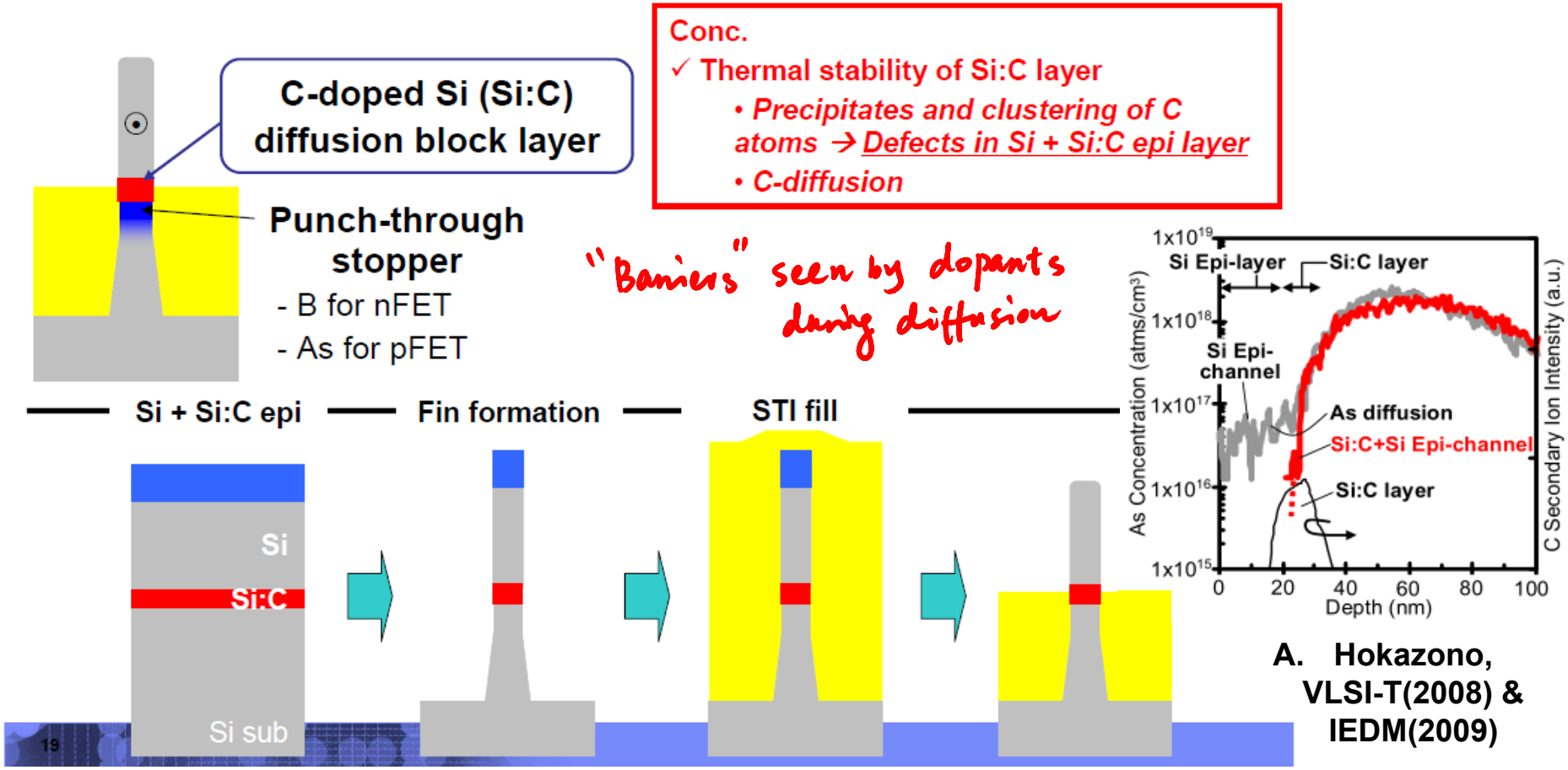


T. Hook (IBM), FDSOI Workshop (2013)

- **Single PTS doping can not be used for SoC circuits with multi-fin width.**
- **Additional STI required to separate N and P-bulk FinFET, to avoid CMOS latchup effect.**

Steep Retrograde Well Doping in Bulk FinFET

SSRW formation using Si + Si:C epi before STI formation



Conc.

✓ Thermal stability of Si:C layer

- *Precipitates and clustering of C atoms → Defects in Si + Si:C epi layer*
- *C-diffusion*

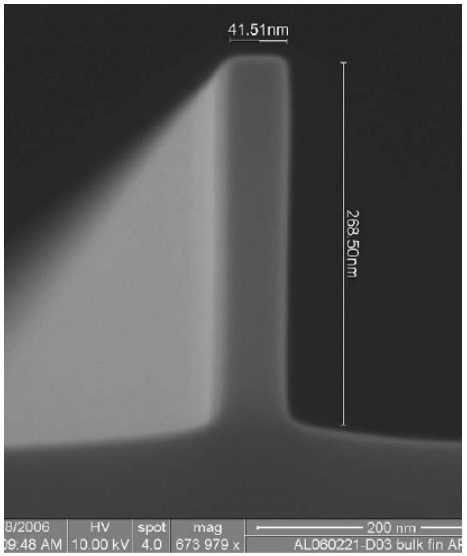
"Barriers" seen by dopants during diffusion

A. Hokazono, VLSI-T(2008) & IEDM(2009)

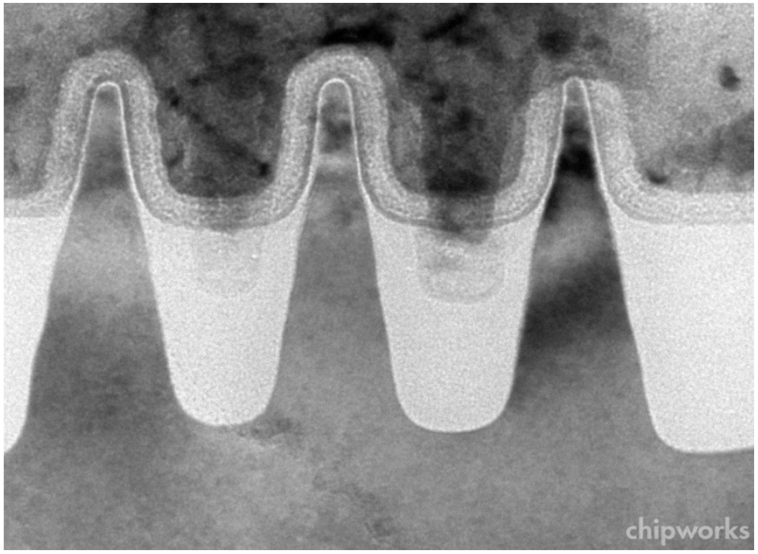
H. Bu (IBM), SOI Workshop (2011)

Fin Shape Variations in Bulk FinFETs

Rectangular shape

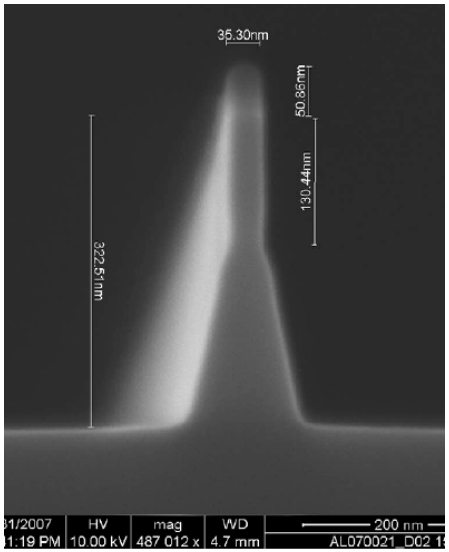


Trapezoidal shape (Intel's Tri-Gate)



Chipworks, 2012

"Hybrid"-shape



D. Shamiryan, SSE (2009)

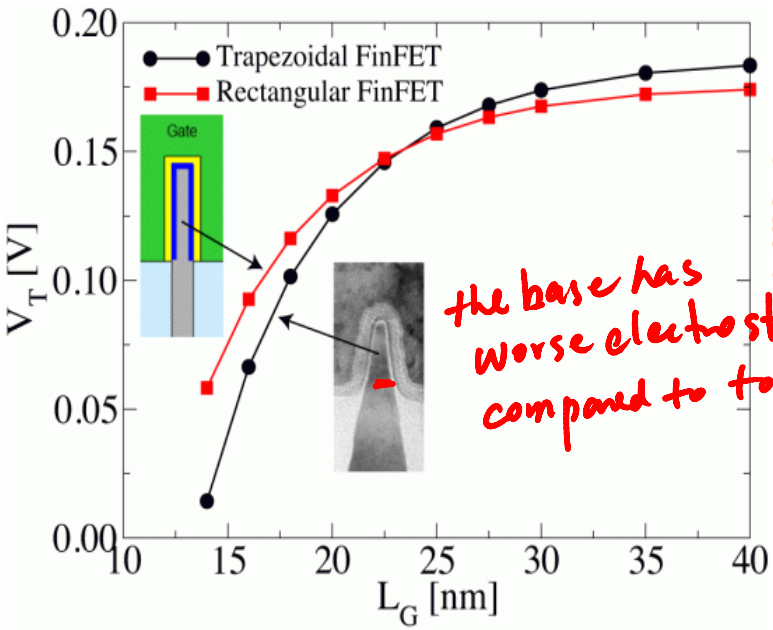
Typical STI trench tilt: 70º ~ 85º

Key requirements for bulk fin shape (process perspective):

- **Isolation trench refilling**
- **High aspect-ratio fin patterning**

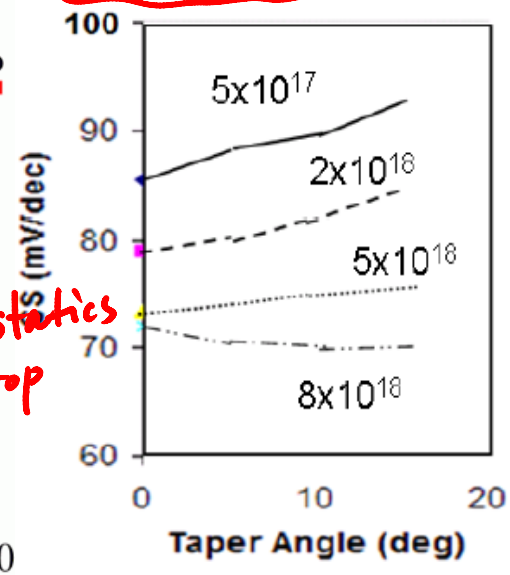
Impacts of Fin Shape on Electrostatics

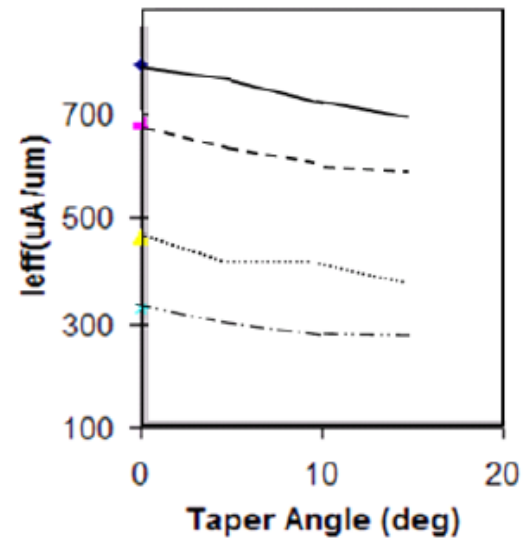
assuming same top fin width:



the base has worse electrostatics compared to top

A. Arsenov's group, GSS Website (2012)





T. Hook (IBM), FDSOI Workshop (2013)

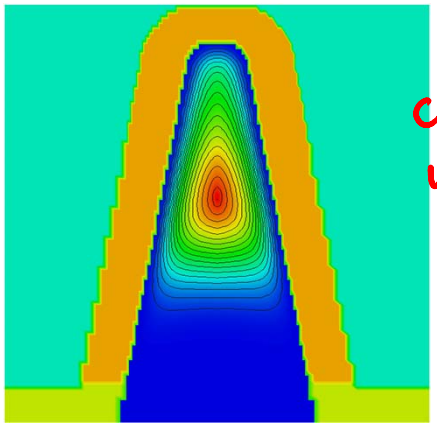
Key requirements for bulk fin shape (device performance/reliability perspective):

- **Good electrostatic control** ← requires narrow Fin base
- **Low corner electric field, to prevent TDDB or BTI** ← prefers triangular top

as W_{Fin} shrinks →

Impacts of Fin Shape on Current

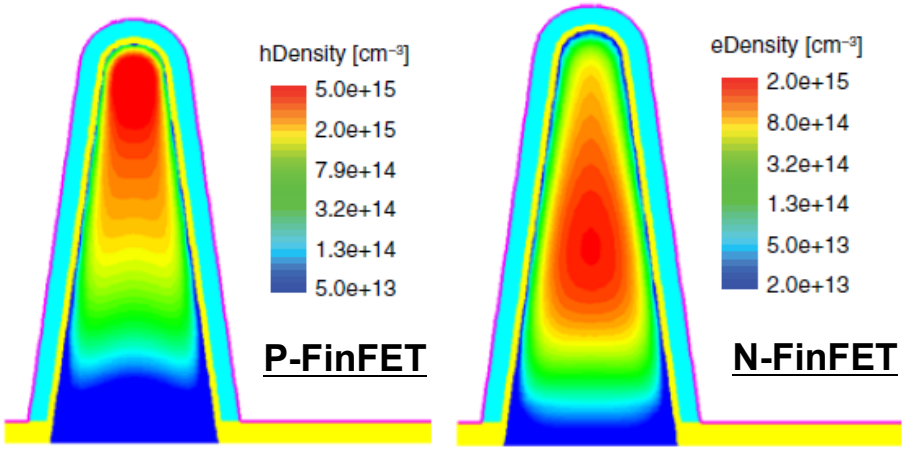
Charge concentration across a FinFET X-section as increasing gate voltage



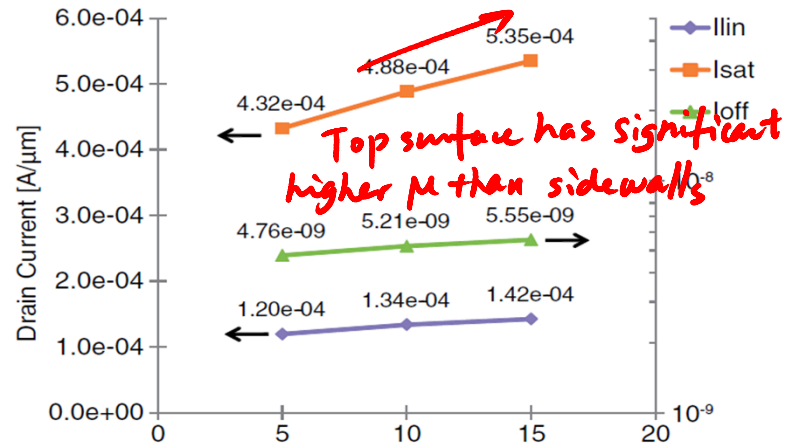
current is not uniform along fin height

A. Arsenov's group, GSS Website (2012)

Considering Quantum Mechanical + Strain Effect

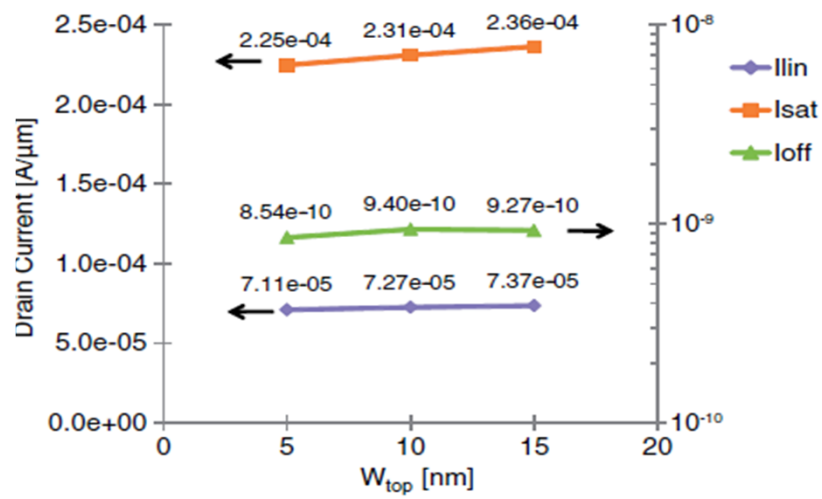


N-FinFET



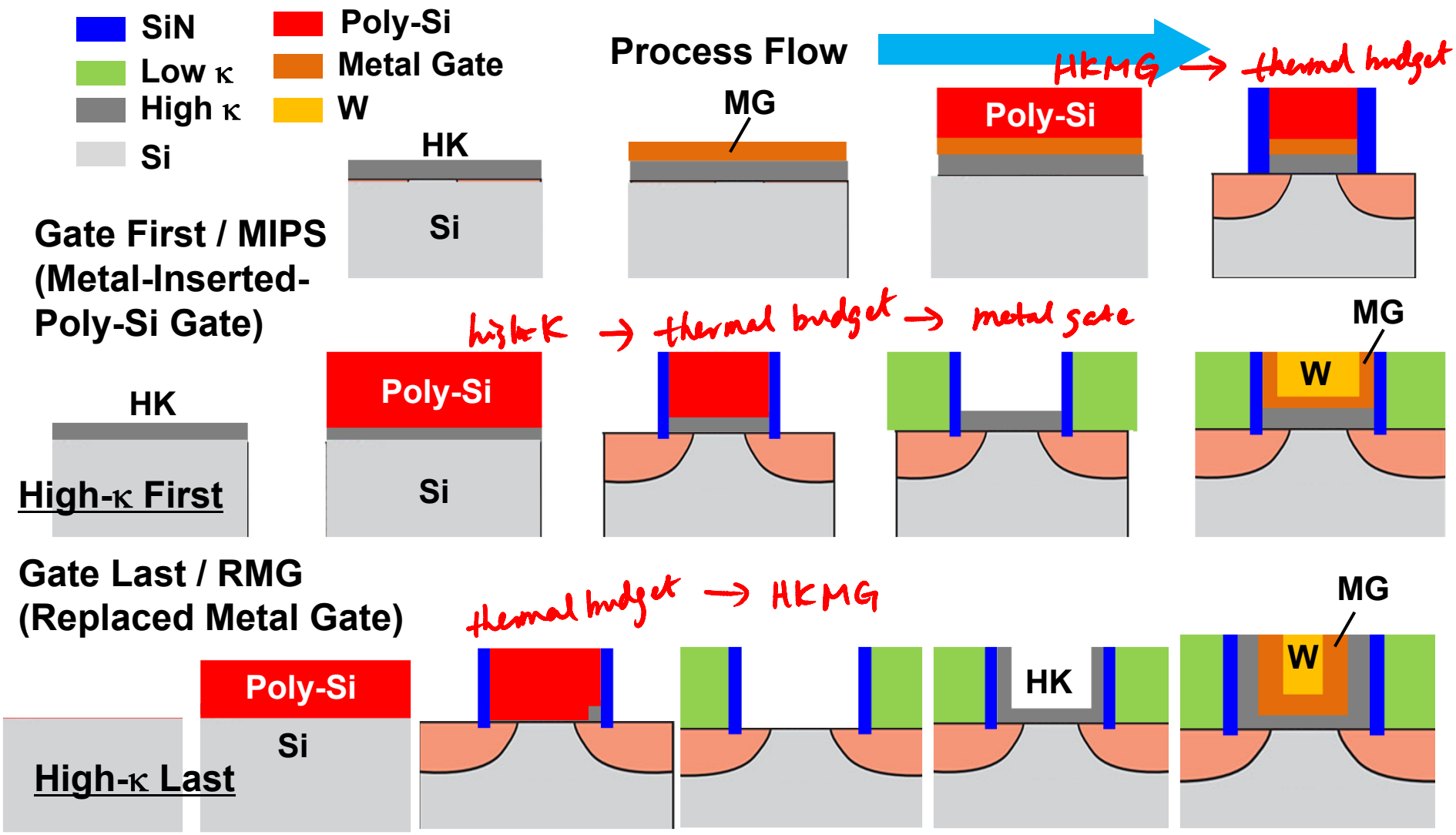
Top surface has significant higher μ than sidewalls

P-FinFET



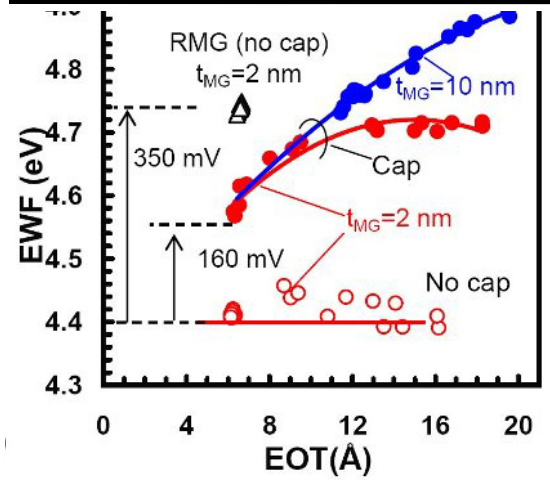
Simulation Data from Synopsys Inc., (2013)

High-κ/Metal Gate Technology

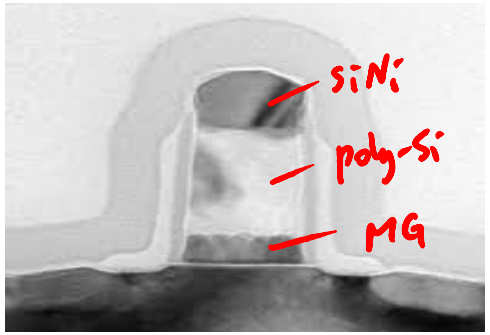


Gate First *vs*. Gate Last

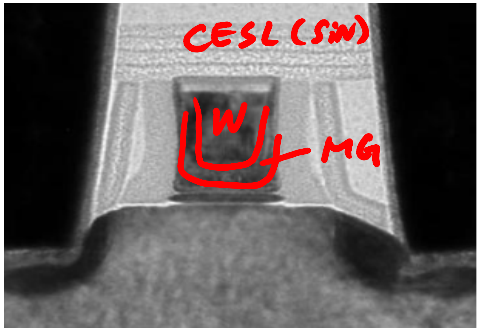
L. Ragnarsson, IEDM (2009)



Gate-First (MIPS)



Gate-Last (RMG)



High-κ Dielectric	First	First → Last
Metal Gate	First	Last
Thermal Budget	High	Low
EOT	Thick	Thin
Mobility	Low	High
Workfunction Control	Bad	Good
Cost	Low	High
Process Complexity	Low	High (CMP)

poly-Si
MG
HK
I.L.
Si

① leaving V_O^+ at HK layer → traps

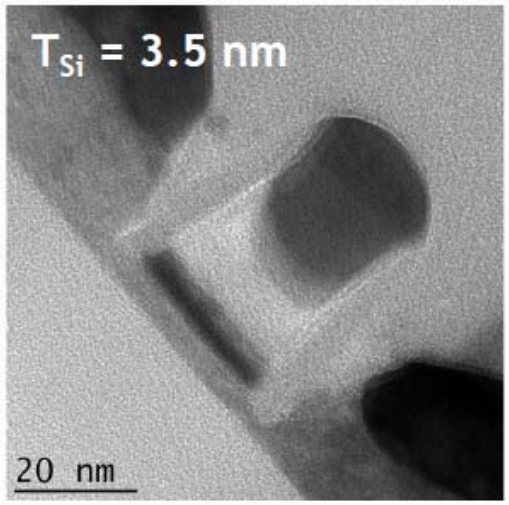
② $O^{2-} + Si \rightarrow SiO$
EOT ↑

③ O^{2-} change workfunction

TiN (MG)

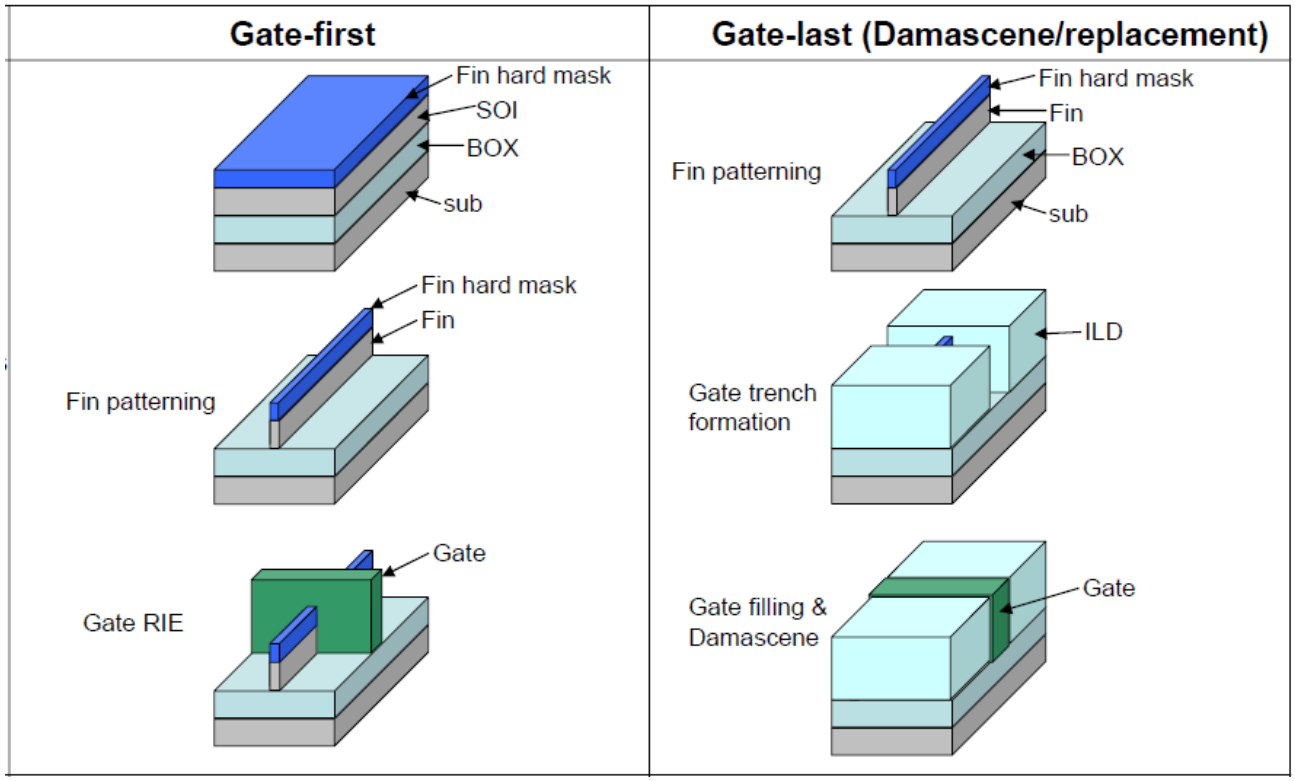
Thin-Body MOSFET Gate Process

IBM's ETSOI MOSFET



A. Khakifirooz, EDL (2012)

A. Yagishita (Toshiba), SOI Short Course (2009)



- **Extremely-thin UTB SOI is not compatible with high-κ-last process, due to the Si sacrifice during dummy (poly-Si) gate removal.**
- **FinFET RMG is challenging, due to the 3-D CMP process.**
- **Cost is the dominant issue.**

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