PROBLEM SET #2

Issued: Tuesday, Sept.15, 2009

Due (at 7 p.m.): Thursday, Sept. 24, 2009, in the EE C245 HW box in 240 Cory.

1. The cross-section below is to be etched via reactive ion etching (RIE). For this problem, assume that the RIE etch is 100% anisotropic and that it etches polysilicon at the rate of 1 μm/min and has a silicon-to-oxide selectivity of 5:1 as well as a silicon-to-photoresist selectivity of 2:1. Draw cross-sections of the structure after etching for (a) 2 min.; (b) 5 min.; and (c) 6 min.

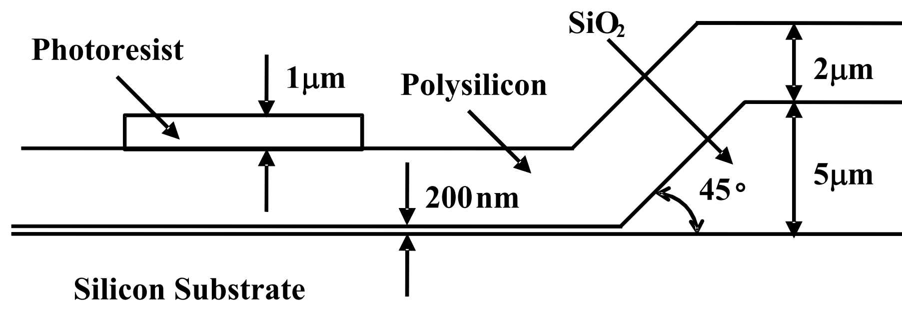

Figure 1

2. The linear coefficient of thermal expansion of the glass used for a photolithography mask is given by the expression

$$TC_F = \frac{1}{L}\frac{\partial L}{\partial T} \approx \frac{\Delta L}{L}\frac{1}{\Delta T}$$

where L is a length on the mask and T is temperature. Let TC_F=3 ppm/^{o}C for a given mask. Suppose that an alignment accuracy of 0.5 μm across a 6-inch silicon substrate is required from one layer to the next. Assume the thermal expansion of silicon is negligible in comparison and that all previous masking steps were done with masks at the same temperature as the silicon wafer.

(a) Assuming that a scanning 1:1 projection printer with global alignment is used, how close should the temperature of the mask be kept relative to the silicon wafer during alignment in order to achieve this accuracy? (i.e., what is the maximum allowable temperature deviation?)

(b) Repeat (a) for the case of a 5:1 projection stepper with die-to-die alignment. Assume the die size is 1 cm^2. Is this better than for the 1:1 projection printer?

3. Figure 2 presents a 2 μm-thick polysilicon film sandwiched between two 2μm thick phosphosilicate glass (PSG) films, each deposited via LPCVD so that they contain 10 wt. % of phosphorous. The cross-section of this device is shown below. The wafer is then annealed at 1000 ^{o}C in an N_2 ambient.

[*Assume for this problem that the diffusion coefficient D_0 of poly-silicon is 10 times larger than that of single crystal silicon (SCS). Also, assume that the solid-solubility limit and electrically active concentration limits, as well as carrier mobility of polysilicon, are the same as SCS. Some of this isn't actually entirely true, but it makes the problem more tractable. Finally, note that there is additional information in the table following Figure 2.*]

(a) Calculate the concentration of phosphorus in PSG.

(b) Suppose the polysilicon beam is initially uniformly doped with gallium to a concentration $N_A = 10^{15}$ cm^{-3}. If you would like to counterdope the top and bottom sides of the beam with phosphorous to junction depths of 800 nm on each side, how long would you need to keep the wafer in the diffusion furnace?

(c) What is the sheet resistance of the doped poly-silicon layer?

(d) Suppose the above doping process is not the only high-temperature step in your process, but entails the following subsequent steps:

1. An LTO deposition at a temperature of 400 ^{o}C over a time period of 100 min.
2. Poly-silicon deposition at a temperature of 600 ^{o}C over a time period of 120 min.
3. A rapid thermal anneal at temperature of 1050 ^{o}C over a time period of 1 min.

i. Rank the four thermal steps from the greatest effect on the phosphorus diffusion profile to the least.

ii. What is the new doping depth after these additional three steps?

Figure 2

	P	SiO_2
Density (g/cm^3)	2.34	2.20
Molar Mass (g/mol)	31	60