EE C245 – ME C218
Introduction to MEMS Design
Fall 2010

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Lecture Module 6: Bulk Micromachining

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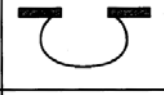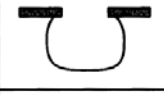
Lecture Outline

- Reading: Senturia Chpt. 3, Jaeger Chpt. 11, Handouts: "Bulk Micromachining of Silicon"
- Lecture Topics:
  - ↳ Bulk Micromachining
  - ↳ Anisotropic Etching of Silicon
  - ↳ Boron-Doped Etch Stop
  - ↳ Electrochemical Etch Stop
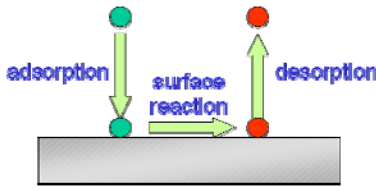 - ↳ Isotropic Etching of Silicon
  - ↳ Deep Reactive Ion Etching (DRIE)

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Bulk Micromachining

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- Basically, etching the substrate (usually silicon) to achieve microstructures
- Etching modes:
  - ↳ Isotropic vs. anisotropic
  - ↳ Reaction-limited
    - ☞ Etch rate dep. on temp.
  - ↳ Diffusion-limited
    - ☞ Etch rate dep. on mixing
    - ☞ Also dependent on layout & geometry, i.e., on loading
- Choose etch mode based on
  - ↳ Desired shape
  - ↳ Etch depth and uniformity
  - ↳ Surface roughness (e.g., sidewall roughness after etching)
  - ↳ Process compatiblity (w/ existing layers)
  - ↳ Safety, cost, availability, environmental impact

	Wet etch	Plasma (dry) etch
Isotropic		
Anisotropic	{111}	

adsorption   surface reaction   desorption

slowest step controls rate of reaction

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Mechanical Properties of Silicon

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- Crystalline silicon is a hard and brittle material that deforms elastically until it reaches its yield strength, at which point it breaks.
  - ↳ Tensile yield strength = 7 GPa (~1500 lb suspended from 1 mm²)
  - ↳ Young's Modulus near that of stainless steel
  - ↳ {100} = 130 GPa; {110} = 169 GPa; {111} = 188 GPa
  - ↳ Mechanical properties uniform, no intrinsic stress
  - ↳ Mechanical integrity up to 500°C
  - ↳ Good thermal conductor
  - ↳ Low thermal expansion coefficient
  - ↳ High piezoresistivity

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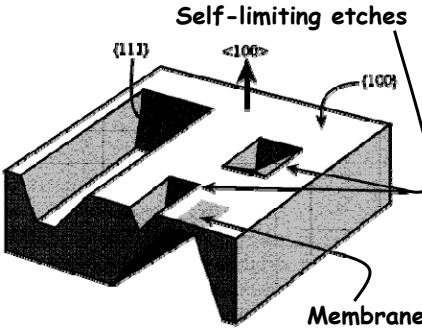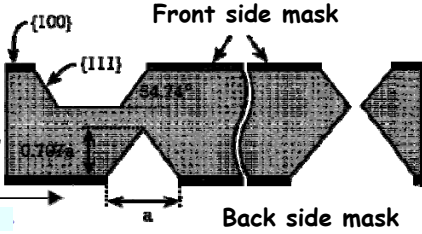
Anisotropic Etching of Silicon

- Etching of Si w/ KOH
  $$Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e^-$$
  $$4H_2O + 4e^- \rightarrow 4(OH)^- + 2H_2$$
- Crystal orientation dependent etch rates
  - ⤷ {110}:{100}:{111}=600:400:1
  - ⤷ {100} and {110} have 2 bonds below the surface & 2 dangling bonds that can react
  - ⤷ {111} plane has three of its bonds below the surface & only one dangling bond to react → much slower E.R.
  - ⤷ {111} forms protective oxide
  - ⤷ {111} smoother than other crystal planes → good for optical MEMS (mirrors)
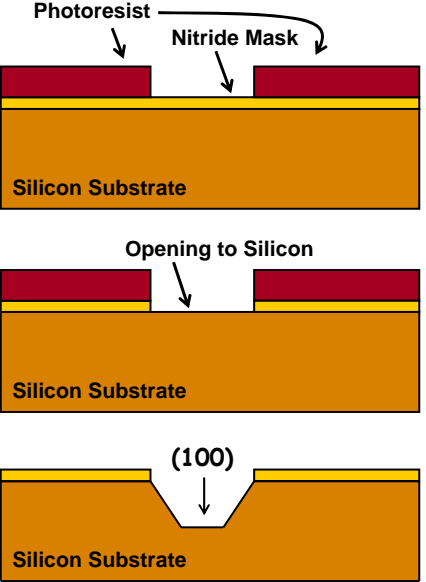
Self-limiting etches

Membrane

Front side mask

Back side mask

Anisotropic Etching of Silicon

Photoresist

Nitride Mask

Silicon Substrate

Opening to Silicon

Silicon Substrate
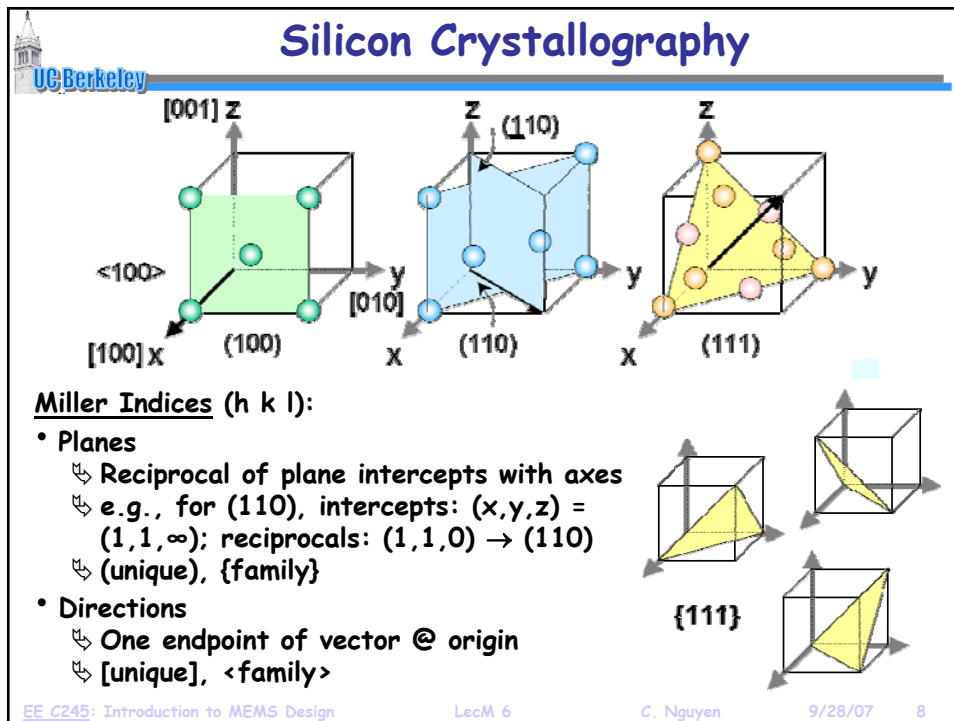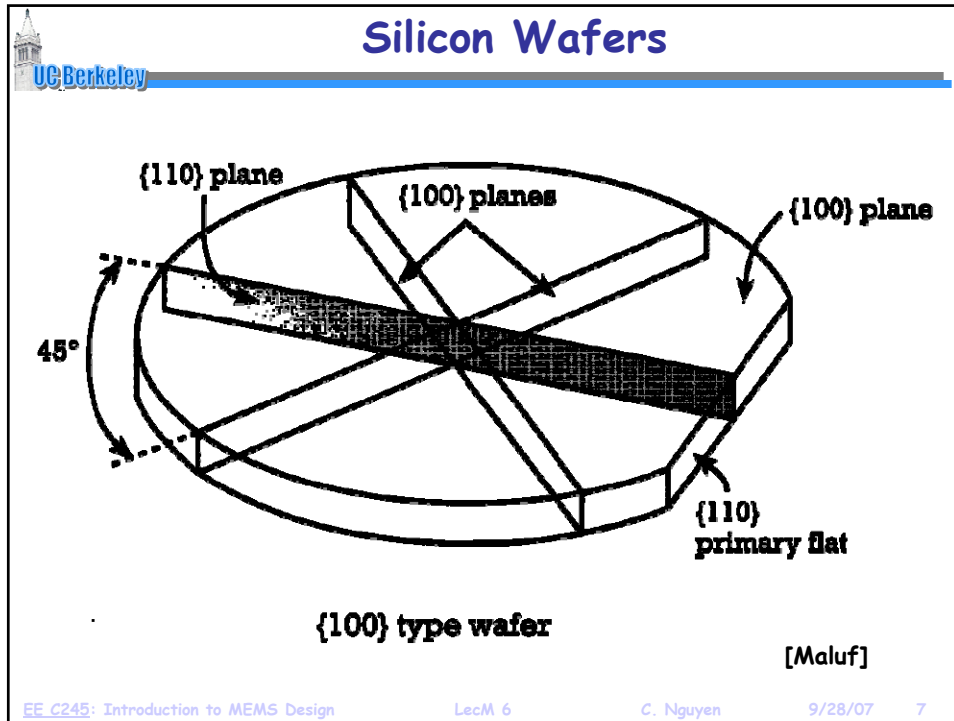
(100)

Silicon Substrate

- Deposit nitride:
  - ⤷ Target = 100nm
  - ⤷ 22 min. LPCVD @800°C
- Lithography to define areas of silicon to be etched
- Etch/pattern nitride mask
  - ⤷ RIE using SF_6
  - ⤷ Remove PR in PRS2000
- Etch the silicon
  - ⤷ Use 1:2 KOH:H_2O (wt.), stirred bath @ 80°C
  - ⤷ Etch Rates:
    - ☞ (100) Si → 1.4 µm/min
    - ☞ Si_3N_4 → ~ 0 nm/min
    - ☞ SiO_2 → 1-10 nm/min
    - ☞ Phoforesist, Al → fast
- Micromasking by H_2 bubbles leads to roughness
  - ⤷ Stir well to displace bubbles
  - ⤷ Can also use oxidizer for (111) surfaces
  - ⤷ Or surfactant additives to suppress bubble formation

Silicon Wafers

{110} plane

{100} planes

{100} plane

45°

{110} primary flat

{100} type wafer

[Maluf]

Silicon Crystallography

[001] z

z , (110)

z

<100>

y

y

y

[010]

[100] x   (100)

x   (110)

x   (111)

Miller Indices (h k l):

• Planes
  ↳ Reciprocal of plane intercepts with axes
  ↳ e.g., for (110), intercepts: $(x,y,z) = (1,1,\infty)$; reciprocals: $(1,1,0) \rightarrow (110)$
  ↳ (unique), {family}

• Directions
  ↳ One endpoint of vector @ origin
  ↳ [unique], <family>

{111}

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Determining Angles Between Planes

- The angle between vectors [abc] and [xyz] is given by:

$$ax + by + cz = |(a,b,c)| \cdot |(x,y,z)| \cdot \cos\theta$$

$$\theta_{(a,b,c),(x,y,z)} = \cos^{-1}\left[\frac{ax+by+cz}{|(a,b,c)| \cdot |(x,y,z)|}\right]$$

- For {100} and {110} → 45°
- For {100} and {111} → 54.74°
- For {110} and {111} → 35.26°, 90°, and 144.74°

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Silicon Crystal Origami

Judy

- Silicon fold-up cube
- Adapted from Profs. Kris Pister and Jack Judy
- Print onto transparency
- Assemble inside out
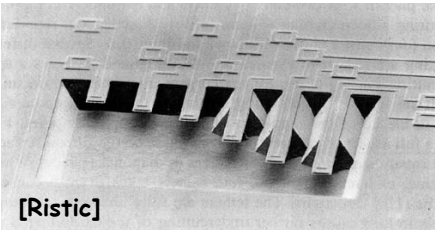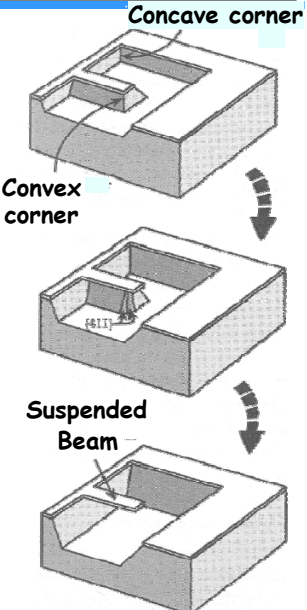- Visualize crystal plane orientations, intersections, and directions

[Judy, UCLA]

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Undercutting Via Anisotropic Si Etching

- Concave corners bounded by {111} are not attacked
- ... but convex corners bounded by {111} are attacked
  - ✎ Two {111} planes intersecting now present two dangling bonds → no longer have just one dangling bond → etch rate fast
  - ✎ <u>Result</u>: can undercut regions around convex corners
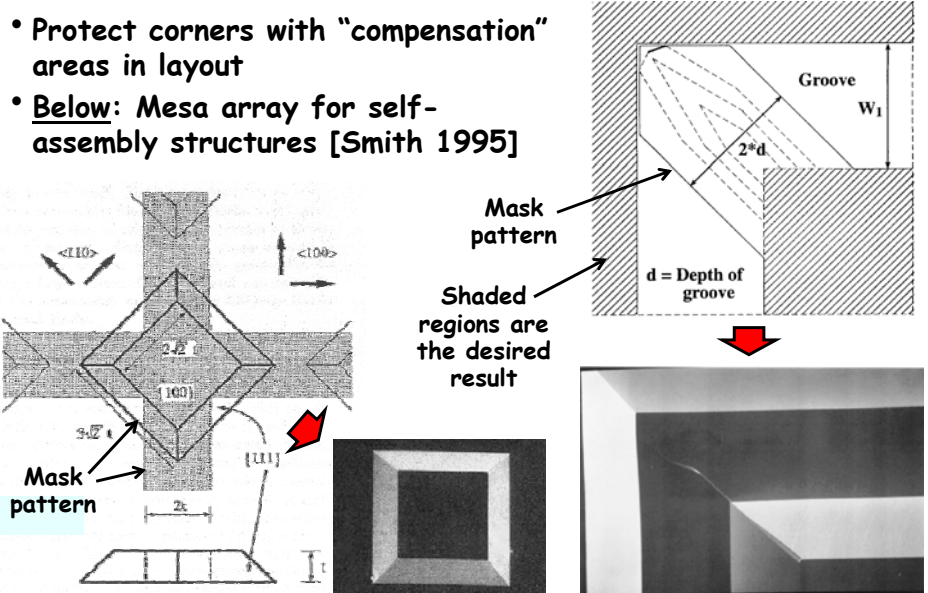
[Ristic]

Concave corner

Convex corner

{411}

Suspended Beam

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Corner Compensation

- Protect corners with "compensation" areas in layout
- <u>Below</u>: Mesa array for self-assembly structures [Smith 1995]

<110>   <100>

2√2 t

[100]

3√2 t

{111}

Mask pattern

2t

t

Mask pattern

Groove

W₁

2*d

d = Depth of groove

Shaded regions are the desired result

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Other Anisotropic Silicon Etchants

- TMAH, Tetramethyl ammonium hydroxide, 10-40 wt.% (90°C)
  - Etch rate (100) = 0.5-1.5 μm/min
  - Al safe, IC compatible
  - Etch ratio (100)/(111) = 10-35
  - Etch masks: SiO_2 , Si3N$_4$ ~ 0.05-0.25 nm/min
  - Boron doped etch stop, up to 40× slower
- EDP (115°C)
  - Carcinogenic, corrosive
  - Etch rate (100) = 0.75 μm/min
  - Al may be etched
  - R(100) > R(110) > R(111)
  - Etch ratio (100)/(111) = 35
  - Etch masks: SiO_2 ~ 0.2 nm/min, Si_3N_4 ~ 0.1 nm/min
  - Boron doped etch stop, 50× slower

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Boron-Doped Etch Stop

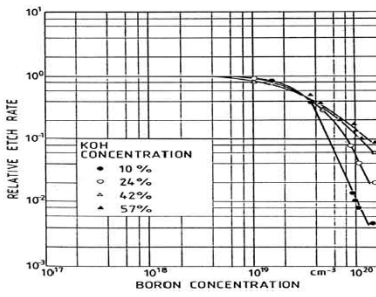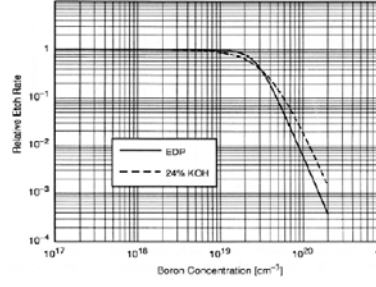EE C245: Introduction to MEMS Design   LecM 6   C. Nguyen   9/28/07   14

Boron-Doped Etch Stop

- Control etch depth precisely with boron doping (p++)
  - ↳ [B] > 10^{20} cm^{-3} reduces KOH etch rate by 20-100×
  - ↳ Can use gaseous or solid boron diffusion
  - ↳ Recall etch chemistry:
    $Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e^-$
    $4H_2O + 4e^- \rightarrow 4(OH)^- + 2H_2$
  - ↳ At high dopant levels, injected electrons recombine with holes in valence band and are unavailable for reactions to give OH$^-$
- Result:
  - ↳ Beams, suspended films
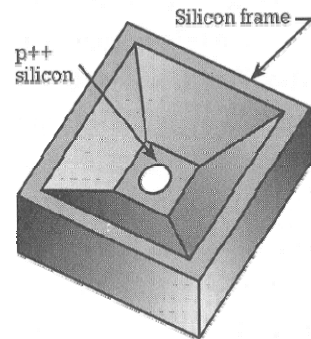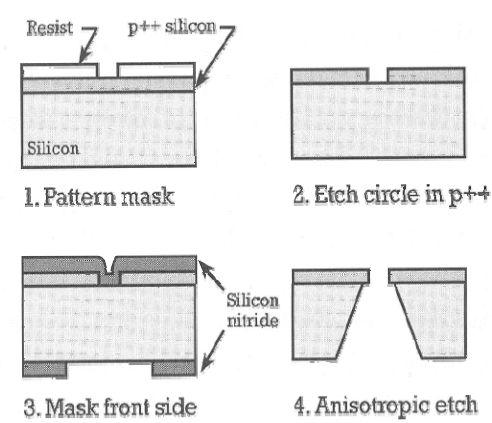 - ↳ 1-20 μm layers possible

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Ex: Micronozzle

- Micronozzle using anisotropic etch-based fabrication
- Used for inkjet printer heads

[Maluf]

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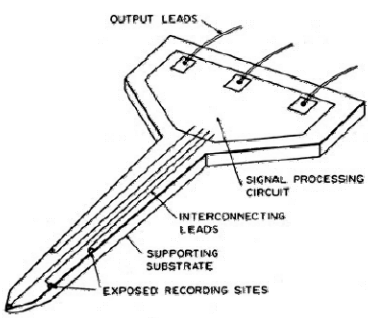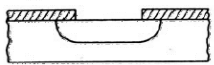
Ex: Microneedle

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- **Below**: micro-neurostimulator
  - ⮱ Used to access central nervous system tissue (e.g., brain) and record electrical signals on a cellular scale
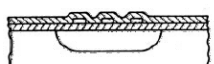- Wise Group, Univ. of Michigan

Sharp Probe Tip

OUTPUT LEADS

SIGNAL PROCESSING CIRCUIT
INTERCONNECTING LEADS
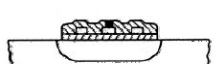SUPPORTING SUBSTRATE
EXPOSED RECORDING SITES

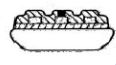Multi-Channel Recording Array Structure

Selectively diffuse p++ into substrate

Deposit interconnect pattern and insulate conductors
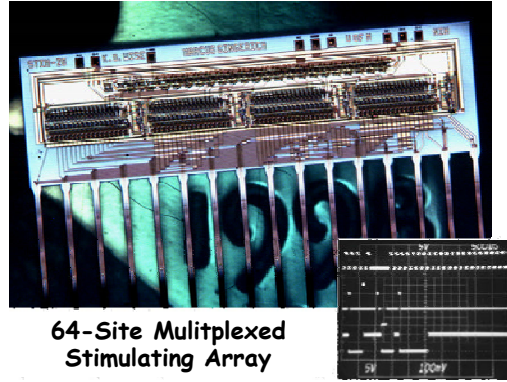
Pattern dielectric and metallize recording sites

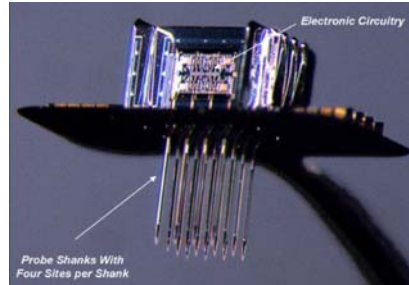Dissolve away the wafer (no mask needed)

Ex: Microneedles (cont.)

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Electronic Circuitry

Probe Shanks With Four Sites per Shank

64-Site Mulitplexed Stimulating Array

[Wise, U. of Michigan]

- **Micromachined with on-chip CMOS electronics**
- **Both stimulation and recording modes**
- **400 mm site separations, extendable to 3D arrays**
- **Could be key to neural prosthesis systems focusing on the central nervous system**

Electrochemical Etch Stop

Electrochemical Etch Stop

- **When silicon is biased with a sufficiently large anodic potential relative to the etchant → get oxidation (i.e., electrochemical passivation), which then prevents etching**
- **For passivation to occur, current flow is required**
- **If current flow can be prevented → no oxide growth, and etching can proceed**
  - ⤷ **Can prevent current flow by adding a reverse-biased diode structure**

Masking Material

+

V_{pass}

−

(100) p-type Si

Etchant

Electrode

Oxide Forms

Diffuse n-type to make a pn-junction

n-type

(100) p-type Si

+

V_{pass}

−

Etchant Solution

Electrode

No Oxide Formation

Electrochemical Etch Stop

- Electrochemical etch stop
  - n-type epitaxial layer grown on p-type wafer forms p-n junction diode
  - $V_p > V_n \rightarrow$ electrical conduction (current flow)
  - $V_p < V_n \rightarrow$ reverse bias current (very little current flow)
- Passivation potential: potential at which thin SiO_2 film forms
  - different for p-Si and n-Si, but basically need the Si to be the anode in an electrolytic setup
- Setup:
  - p-n diode in reverse bias
  - p-substrate floating → etched
  - n-layer above passivation potential → not etched

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Electrochemical Etching of CMOS

- N-type Si well with circuits suspended f/ SiO_2 support beam
- Thermally and electrically isolated
- If use TMAH etchant, Al bond pads safe

[Reay, et al. (1994)]
[Kovacs Group, Stanford]

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Ex: Bulk Micromachined Pressure Sensors

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- Piezoresistivity: change in electrical resistance due to mechanical stress
- In response to pressure load on thin Si film, piezoresistive elements change resistance
- Membrane deflection < 1 μm

n-type epilayer, p-type substrate — **Deposit insulator**

Diffuse piezoresistors

Deposit & pattern metal

Electrochemical etch of backside cavity

Anodic bonding of glass

[Maluf]

(100) Si diaphragm — Bondpad — P-type diffused piezoresistor — Metal conductors — n-type epitaxial layer

R_2 R_1 R_3

(111)

Backside port — Etched cavity — Anodically bonded Pyrex substrate

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Ex: Pressure Sensors

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- **Below**: catheter tip pressure sensor [Lucas NovaSensor]
    ↳ Only 150×400×900 μm^3

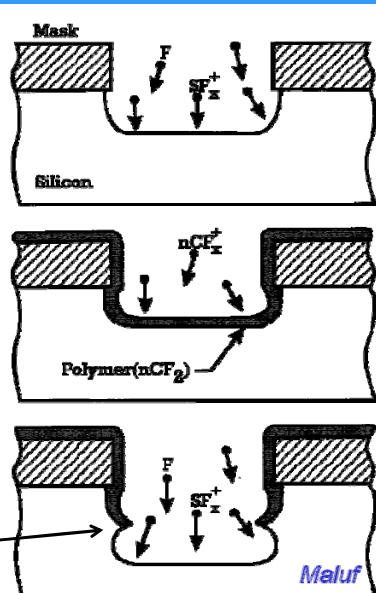
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Deep Reactive-Ion Etching (DRIE)

The Bosch process:
- Inductively-coupled plasma
- Etch Rate: 1.5-4 μm/min
- Two main cycles in the etch:
  - Etch cycle (5-15 s): SF_6 (SF_x^+) etches Si
  - Deposition cycle: (5-15 s): C_4F_8 deposits fluorocarbon protective polymer (CF_2^-)$_n$
- Etch mask selectivity:
  - SiO_2 ~ 200:1
  - Photoresist ~ 100:1
- Issue: finite sidewall roughness
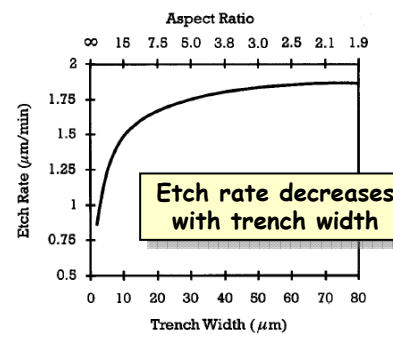 - scalloping < 50 nm
- Sidewall angle: $90° \pm 2°$
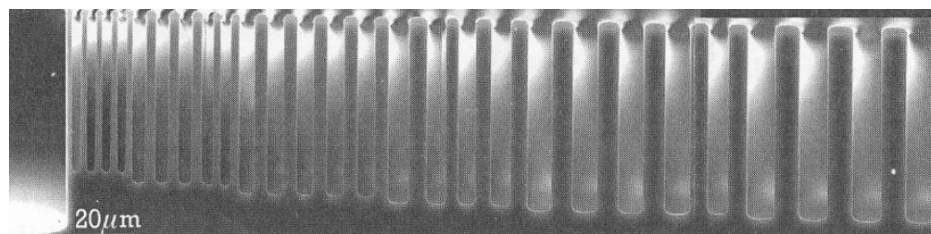
Maluf

DRIE Issues: Etch Rate Variance

20μm

- Etch rate is diffusion-limited and drops for narrow trenches
  - Adjust mask layout to eliminate large disparities
  - Adjust process parameters (slow down the etch rate to that governed by the slowest feature)

Etch rate decreases with trench width

DRIE Issues: "Footing"

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- **Etch depth precision**
  - ↳ Etch stop: buried layer of SiO_2
  - ↳ Due to 200:1 selectivity, the (vertical) etch practically just stops when it reaches SiO_2
- **Problem**: Lateral undercut at Si/SiO$_2$ interface → "footing"
  - ↳ Caused by charge accumulation at the insulator

Poor charge relaxation and lack of neutralization of e⁻'s at insulator
↓
Ion flux into substrate builds up (+) potential

Charging-induced potential perturbs the E-field
↓
Distorts the ion trajectory
↓
Result: strong and localized damage to the structure at Si-SiO$_2$ interface → "footing"

mask
Si
insulation layer
Charge accumulation

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Recipe-Based Suppression of "Footing"

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- Use **higher process pressure** to reduce ion charging [Nozawa]
  - ↳ High operating pressure → concentration of (-) ions increases and can neutralize (+) surface charge
  - ↳ Issue: must introduce as a separate recipe when the etch reaches the Si-insulator interface, so must be able to very accurately predict the time needed for etching
- **Adjust etch recipe** to reduce overetching [Schmidt]
  - ↳ Change C_4F_8 flow rate, pressure, etc., to enhance passivation and reduce overetching
  - ↳ Issue: Difficult to simultaneously control footing in a narrow trench and prevent grass in wide trenches
- Use **lower frequency plasma** to avoid surface charging [Morioka]
  - ↳ Low frequency → more ions with low directionality and kinetic energy → neutralizes (-) potential barrier at trench entrance
  - ↳ Allows e⁻'s to reach the trench base and neutralize (+) charge → maintain charge balance inside the trench

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Metal Interlayer to Prevent "Footing"

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Pre-defined metal interlayer grounded to substrate supplies e's to neutralize (+) charge and prevent charge accumulation at the Si-insulator interface

(a) Photolithography 1 (sacrificial)

(b) Preparatory trenches

(c) Metal interlayer deposition

(d) Lift-off (remove PR)

(e) Anodic Bonding

(f) Silicon Thinning

(g) Photolithography 2

(h) DRIE

(i) Remove metal interlayer

(i) Metallize

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Footing Prevention (cont.)

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* **Below**: DRIE footing over an oxide stop layer
* **Right**: efficacy of the metal interlayer footing prevention approach

[Kim, Stanford]

No metal interlayer

Footing

No footing

With metal interlayer
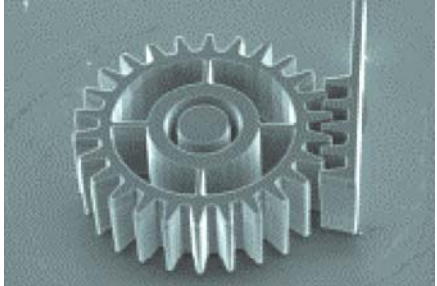
[Kim, Seoul Nat. Univ.]
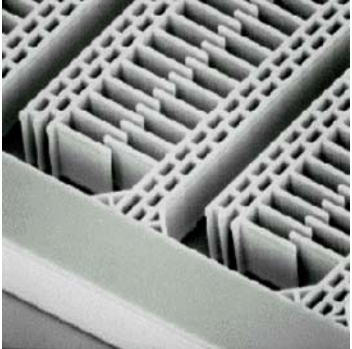
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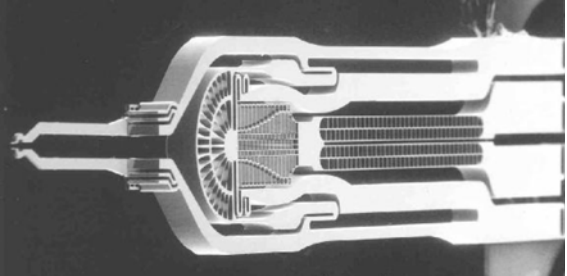
DRIE Examples

High aspect-ratio gear

Tunable Capacitor [Yao, Rockwell]

Microgripper [Keller, MEMS Precision Instruments]

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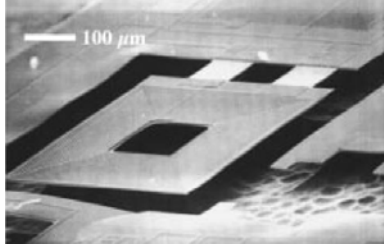
Vapor Phase Etching of Silicon

- Vapor phase Xenon Difluoride (XeF_2)
  $$2XeF_{2(g)} + Si_{(s)} \rightarrow 2Xe_{(g)} + SiF_{4(g)}$$
- Set-up:
  - ↳ Xe sublimes at room T
  - ↳ Closed chamber, 1-4 Torr
  - ↳ Pulsed to control exothermic heat of reaction
- Etch rate: 1-3 μm/min, isotropic
- Etch masks: photoresist, SiO_2, Si_3N_4, Al, other metals
- Issues:
  - ↳ Etched surfaces have granular structure, 10 μm roughness
  - ↳ Hazard: XeF_2 reacts with H_2O in air to form Xe and HF

Xactix XeF_2 Etcher

Inductor w/ no substrate [Pister]
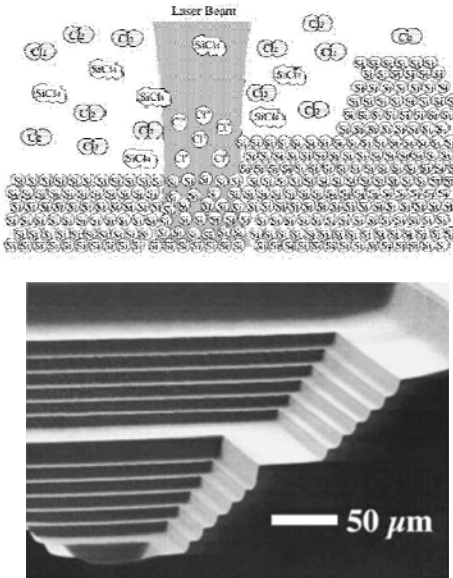
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Laser-Assisted Chemical Etching

- Laser creates Cl radicals from $Cl_2 \rightarrow$ reaction forms $SiCl_2$
- Etch rate: 100,000 μm^3/s
  - ↳ Takes 3 min. to etch 500×500×125 μm^3 trench
- Surface roughness: 30 nm rms
- Serial process: patterned directly from CAD file

- <u>At right</u>:
  - ↳ Laser assisted etching of a 500×500 μm^2 terraced silicon well
  - ↳ Each step is 6 μm-deep

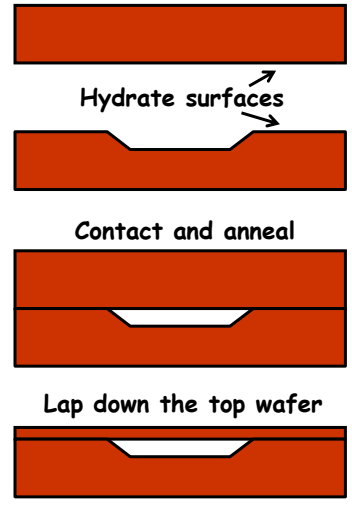*EE C245: Introduction to MEMS Design*   LecM 6   C. Nguyen   9/28/07   33

Wafer Bonding

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Fusion Bonding

- **Two ultra-smooth (<1 nm roughness) wafers are bonded without adhesives or applied external forces**
- **Procedure:**
  - ↳ **Prepare surfaces: must be smooth and particle-free**
    - ☛ **Clean & hydrate: O_2 plasma, hydration, or HF dip**
  - ↳ **When wafers are brought in contact at room temperature, get hydrogen bonding and/or van der Waals forces to hold them together**
  - ↳ **Anneal at 600-1200°C to bring the bond to full strength**
- **Result: a bond as strong as the silicon itself!**

Hydrate surfaces

Contact and anneal

Lap down the top wafer
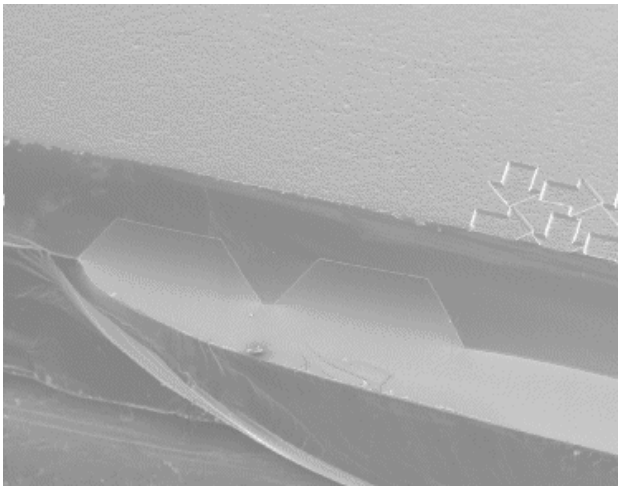
Works for Si-to-Si bonding and Si-to-SiO$_2$ bonding

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Fusion Bonding Example

- **Below: capacitive pressure sensor w/ fusion-bonded features**

[Univ. of Southampton]

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Anodic Bonding

- Bonds an electron conducting material (e.g., Si) to an ion conducting material (e.g., sodium glass = Pyrex)
- Procedure/Mechanism:
  - ↪ Press Si and glass together
  - ↪ Elevate temperature: 180-500°C
  - ↪ Apply (+) voltage to Si: 200-1500V
    - ☛ (+) voltage repels Na⁺ ions from the glass surface
    - ☛ Get net (-) charge at glass surface
    - ☛ Attractive force between (+) Si and (-) glass → intimiate contact allows fusing at elevated temp.
  - ↪ Current drops to zero when bonding is complete

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Anodic Bonding (cont.)

- <u>Advantage</u>: high pressure of electrostatic attraction smoothes out defects
- <u>Below</u>: 100 mm wafers, Pyrex glass 500 μm-thick, 430°C, 800V, N₂ @ 1000 mbar

1. after 5 sec — Only center bond pin active
2. after 20 sec — All bond pins active
3. after 2,5 min — Bond front spreads
4. after 8 min — Bond 98% completed

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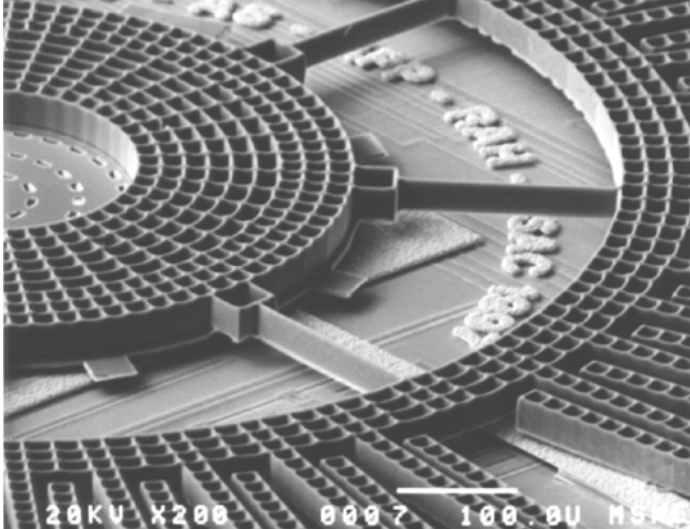## Metal Layer Bonding

- Pattern seal rings and bond pads photolithographically
- **Eutectic bonding**
  - ↳ Uses eutectic point in metal-Si phase diagrams to form silicides
  - ↳ Au and Si have eutectic point at 363°C
  - ↳ Low temperature process
  - ↳ Can bond slightly rough surfaces
  - ↳ <u>Issue</u>: Au contamination of CMOS
- **Solder bonding**
  - ↳ PbSn (183°C), AuSn (280°C)
  - ↳ Lower-T process
  - ↳ Can bond very rough surfaces
  - ↳ <u>Issue</u>: outgassing (not good for encapsulation)
- **Thermocompression**
  - ↳ Commonly done with electroplated Au or other soft metals
  - ↳ Room temperature to 300°C
  - ↳ Lowest-T process
  - ↳ Can bond rough surfaces with topography

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Thermocompression Bonding

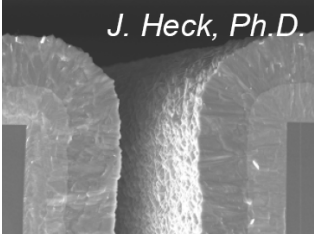- <u>Below</u>: Transfer of hexsil actuator onto CMOS wafer

[Singh, et al, Transducers'97]

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Hexsil MEMS

- **Achieves high aspect ratio structures using conformal thin films in mold trenches**
- **Parts are demolded (and transferred to another wafer)**
- **Mold can be reused**
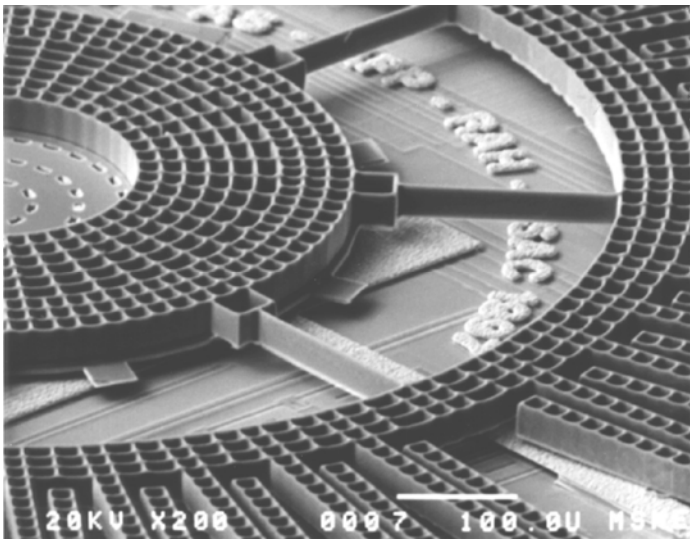- **Design with honeycomb structure for strength**

J. Heck, Ph.D.

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Hexsil MEMS Actuator

- **Below**: Transfer of hexsil actuator onto CMOS wafer

[Singh, et al, Transducers'97]

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Silicon-on-Insulator (SOI) MEMS

- No bonding required
- Si mechanical structures anchored by oxide pedestals
- Rest of the silicon can be used for transistors (i.e., CMOS compatible)

SOI MEMS Examples

[Brosnihan]
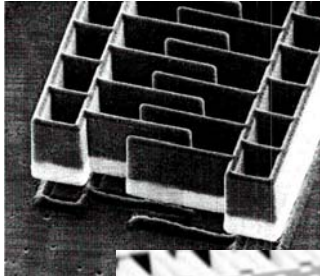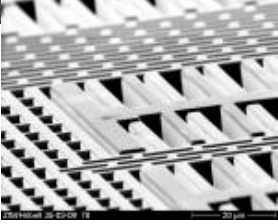
Micromirror
[Analog Devices]
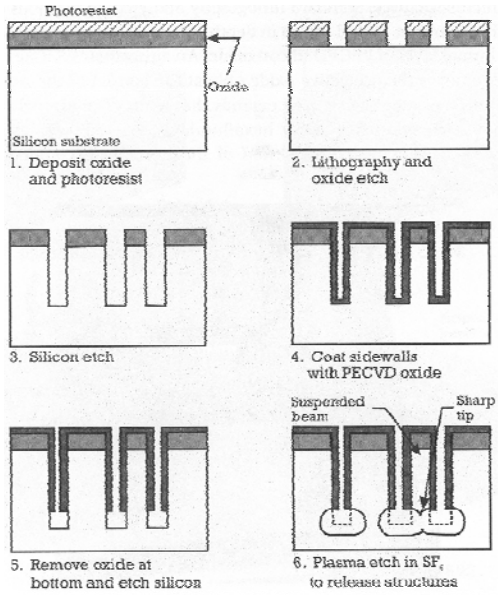
The SCREAM Process

- **SCREAM**: **S**ingle **C**rystal **R**eactive **E**tching and **M**etallization process

1. Deposit oxide and photoresist
2. Lithography and oxide etch
3. Silicon etch
4. Coat sidewalls with PECVD oxide
5. Remove oxide at bottom and etch silicon
6. Plasma etch in SF₆ to release structures