Circuit Sensitivity to Interconnect Variation

Zhihao Lin, *Member, IEEE,* Costas J. Spanos, *Senior Member, IEEE,* Linda S. Milor, *Member, IEEE,* and Y. T. Lin

Abstract—**Deep submicron technology makes interconnect one of the main factors determining the circuit performance. Previous work shows that interconnect parameters exhibit a significant amount of spatial variation. In this work, we develop approaches to study the influence of the interconnect variation on circuit performance and to evaluate the circuit sensitivity to interconnect parameters. First, an accurate interconnect modeling technique is presented, and an interconnect model library is developed. Then, we explore an approach using parameterized interconnect models to study circuit sensitivity via a ring oscillator circuit. Finally, we present an alternative approach using statistical experimental design techniques to study the sensitivity of a large and complicated circuit to interconnect variations.**

Index Terms—**Circuit analysis, interconnect, statistical analysis, worst case design.**

I. INTRODUCTION

THE CONTINUOUSLY increasing scale of integration used in the design and processing of integrated circuits has drawn special attention toward interconnect effects. As the minimum feature size in VLSI systems drops to 0.25 μm and below, interconnect characteristics are becoming limiting factors on performance, since the time constant associated with interconnect is scaled by a smaller factor compared to those of devices. Future chip complexity and speed advances will depend on the ability to model the electrical behavior of interconnect in an accurate and efficient fashion.

Critical path delays in circuits depend upon interconnect as well as on device parameters. The effects of device parameter variations have been widely studied [12]–[16]. However, these simulations currently do not take into account the effects of interconnect parameter variations. As a result, the yield estimation and circuit optimization based on these studies may not be able to provide accurate results in current and future technologies, where more and more significant portions of path delays will result from interconnect.

With current technology, the impact of interconnect parameter variations on signal delays may already be quite significant [2]. Thus, it becomes necessary to comprehend and anticipate the effects of interconnect parameter variation in the design process. Specifically, a methodology to asses the impact of random and systematic variations in interconnect parameters to circuit performance must be developed.

A modeling framework to study the sensitivity of circuit performance to interconnect parameter variations will allow circuit designers to meet timing targets while taking into account the random and systematic source of interconnect parameter variations. It will also help the process designers to design new technologies while taking the sensitivity information into consideration. Finally, the sensitivity study results will help make the circuit more robust against the variation.

Overall, the goal of this paper is to address the problem of interconnect variations, look for a methodology to model interconnect wires, and develop approaches to quantify and investigate interconnect parameter variations on circuit performance under current and future technologies. The ultimate objective is to facilitate optimal circuit and process design, reduce time-to-yield, and improve the final yield.

Two approaches to study the circuit sensitivity to interconnect parameter variations are developed in this paper. The first approach is based on a parameterized interconnect model library. The parameterized interconnect models allow us to manipulate interconnect parameters, and to generate a circuit description that is suitable for performance sensitivity study. The second approach uses statistical experimental design techniques to analyze complicated circuits via simulation experiments. The first approach is illustrated with the help of a ring oscillator circuit, and the second approach is illustrated with a large multiplier circuit.

II. INTERCONNECT MODELING

A. Introduction

In order to understand and account for interconnect effects in the design process, it is necessary to extract its parasitic parameters and model the interconnection. It is essential that the electrical behavior of interconnect is modeled accurately. The accuracy of interconnect models is the very basis of achieving meaningful predictions of circuit behavior and obtain reliable sensitivity evaluations. The models should also be suitable for statistical circuit simulation and sensitivity analysis, which is the purpose of this work.

One approach to interconnect modeling is to construct an equivalent electrical circuit representation. The equivalent circuits that represent the interconnections can be combined with the equivalent circuits that describe the active devices, and the behavior of the entire circuit can be analyzed with a circuit simulator such as HSPICE.

There are two steps to the process of constructing an equivalent circuit model for an interconnect wire. The first step is to determine the nature of the equivalent circuit, that is, what kinds of circuit elements are important, and how many degrees

of freedom are required for the level of accuracy desired. The second step is to determine the value associated with each element in the equivalent circuit.

Reference [10] claims that the equivalent circuit for an average length on-chip interconnection in CMOS chips can be constructed using capacitors and resistors. In modern lossy on-chip interconnect, the inductive voltage drop is negligible compared to resistive voltage drop up to clock frequencies of 1–2 GHz. Thus, on-chip interconnect lines may be approximated by an RC line. So, throughout this work, all on-chip interconnects are modeled as RC networks.

Once it has been determined what types of circuit elements are required to model a particular class of on-chip interconnections, one must then decide how many circuit elements of each type are needed and evaluate the values of interconnect parasitics.

There are many ways to extract the parasitics. The applications of empirical formulae to general submicron interconnect wires are rather limited because of the complexity of interconnect configurations in multilevel submicron technology, especially in extracting the coupling capacitance. These formulae can not cover layout configurations having multiple dielectric and metal layers. Furthermore, they are not accurate enough to capture the variations of the layout and technology parameters of interconnect. So their applicability in our work of sensitivity study over the technology parameters is not appropriate.

In "exact" computations of electrical circuit parameters, one appeals to the theory of electromagnetic fields; that is, "exact" computations involve the numerical analysis of two or three dimensional integral or partial-differential equations for the values of an electromagnetic field.

Since multilevel interconnect technologies use multiple conductors with different thicknesses and multiple insulators with possibly different dielectric constants, numerical simulations are mandatory for accurate resistance and capacitance modeling [20]–[22]. Numerical techniques have been developed for rigorous interconnect capacitance extraction.

B. Interconnect Model Library

We have concluded the necessity of numerically based simulation to perform interconnect parasitics extraction. However, numerical simulation is computationally intensive and real-time simulation is too time-consuming. Furthermore, in our approach to perform sensitivity study, all interconnect wires are to be modeled using closed-form analytical models, which requires parameterized interconnect models. To cope with this problem, a realistic approach is to construct a parameterized interconnect model library based on numerical simulations. Then the circuit description can be generated with the help of the model library which contains models of typical two-dimensional interconnect structures. The circuit description will thus become the basis of sensitivity study and statistical circuit simulation.

Fig. 2 shows the flow of this interconnect modeling approach and model library building. The sensitivity analysis is performed assuming that the variation of technology pa-
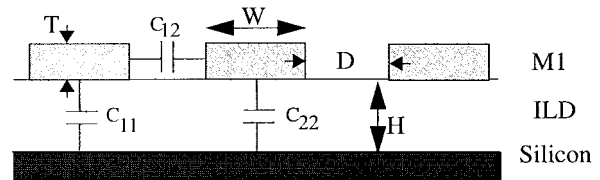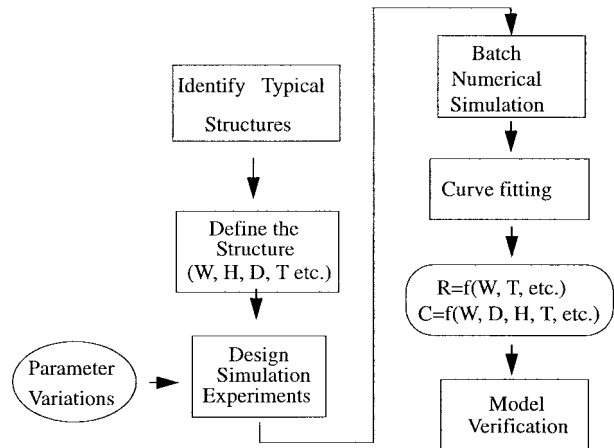

Fig. 1. Cross section of an interconnect structure.

Fig. 2. Interconnect modeling flow.

rameters, interlayer dielectric thickness, conductor thickness, is within about $\pm 20\%$[1] of its nominal value for a given technology. At the same time, the ranges of the layout parameters, such as metal width, interwire spacing, are set according to the design rules and their possible design ranges. Each parameter is divided into several levels, and a full factorial design is used to generate the simulation points for each structure. The input file to the numerical simulator is generated to contain all the simulation points, and two dimensional simulations are performed in batch-mode using a numerically based extractor [23] to evaluate the unit length capacitance and resistance values. The numerical data are then fitted to an analytical expression using a special curve-fitting technique which will be discussed in more detail later.

In the following sections, we will use the structure in Fig. 1 as an example to illustrate the approach in more detail.

The interconnect structure shown in Fig. 1 is defined in terms of four parameters: metal width W, interwire distance D, metal thickness T, and ILD thickness H. The three capacitances, C_{22}, C_{11}, and C_{12} are of interest and their models are constructed. Notice that all interwire distances are the same in this structure.

The input file to the numerical extractor Raphael is generated as follows: each parameter, W, D, T, and H, is set at six, six, seven, and seven levels, respectively. Using a full factorial design, a total number of 1764 simulation points (combination of different levels of the four parameters) are generated, and the input file for Raphael is thus created based on these points.

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[1] Based on this assumption, all the variations that are less than 20% of their normal values will be covered by the models. Though this value may not exactly reflect the realistic situation, it does not affect the flow of this approach.

Analytical models are then constructed based on the simulation results. This is discussed in the next section.

C. Curve-Fitting Technique

The objective is to create a model $y = F(x)$ that maps the relationship between the set of parameters defining the physical interconnect and the values of the parasitics of the interconnect. Here y is the n dimensional vector representing the capacitance and resistance to be modeled, and x is the m dimensional input vector containing all the interconnect parameters. This is implemented using simple polynomial expressions and linear regression [24].

The capacitance models can include quadratic and higher order terms of the parameters, together with their interaction terms. In order to achieve an accurate model, the first step is to determine the terms to be included in the final model. After the model terms have been determined, the coefficient of each term can be estimated using the least square technique. However, choosing the terms of the model is a difficult task. In this section, we present a systematic way to address this problem. This efficient and systematic solution is guided by the simple physical relationships between the input variables and the resulting capacitance.

First, we select the data points that are obtained by varying one parameter with the other parameters fixed. Then these data points are fitted over this parameter using step-wise regression. This is easy since only one variable or parameter is involved. In this way, one will get a separate model related to each of the parameters. These models are simple polynomial functions. In some cases, nonlinear data transformations are necessary in order to apply a linear model. Combining these separate models, the final model terms are easy to identify. This is illustrated as follows:

Suppose that capacitance C is an unknown polynomial function of two variables, W and D. That is, $C = f(W, D)$. The goal is to choose the proper model terms based on discrete data points.

Let us assume that by curve-fitting over W with D fixed, one finds that C is a linear function of W, that is,

$$C = aW + b. \tag{1}$$

In the above equation, both a and b are constants. They will take different values when D is fixed at different points. So a and b are only functions of D, i.e.,

$$a = f_1(D) \quad \text{and} \quad b = f_2(D) \tag{2}$$

then (1) can be rewritten as

$$C = f_1(D)W + f_2(D). \tag{3}$$

Suppose that C is fitted over D with W fixed, and the fitting result shows C is a second order polynomial function of D. Following the same argument as above, one can conclude that C can also be expressed as

$$C = g_1(W) \cdot D^2 + g_2(W) \cdot D + g_3(W). \tag{4}$$

Note that (3) and (4) are equivalent expressions. Since both equations represent capacitance, which must be a continuous function of both D and W, we can take the derivative of these two equations over W, which leads to the following expression:

$$f_1(D) = \frac{\partial}{\partial W} g_1(W) \cdot D^2 + \frac{\partial}{\partial W} g_2(W) \cdot D + \frac{\partial}{\partial W} g_3(W). \tag{5}$$

Thus, the model terms of $C(W, D)$ can be decided. Given the fact that the left-hand side (LHS) of (5) does not depend on W, the right-hand side (RHS) should also be independent of W. Then we can conclude that $g_1(W)$, $g_2(W)$, and $g_3(W)$ are linear functions of W, i.e.,

$$g_1(W) = k_1 W + k_2 \tag{6}$$
$$g_2(W) = k_3 W + k_4 \tag{7}$$
$$g_3(W) = k_5 W + k_6. \tag{8}$$

Here, $k_i (i = 1$ to $6)$ are constants. By substituting (6)–(8) into (4), the model terms can be easily identified and the equation can be rewritten as

$$C(W, D) = (k_1 W + k_2) \cdot D^2 + (k_3 W + k_4) \cdot D + (k_5 W + k_6). \tag{9}$$

To simplify the situation, the above illustration assumes that C is a linear function of W when D is fixed. If C is a second or higher order function of W, the above explanation still applies on taking higher order derivatives, which will lead to similar results.

In practice, the above technique is used to choose the terms of the model, while the coefficients of the terms are determined using least squares fitting.

Though only two variables are discussed in the above technique, the approach can be easily generalized to three and more variables. Also, note that even though the above discussion is not a strict mathematical proof, it does provide us with some insight and guidance on data fitting in order to get an accurate capacitance model.

D. Example

We apply this technique to model the C_{22} and C_{12} as depicted in Fig. 1. Table I summarizes the modeling results of C_{22}. It indicates that multiple R^2 is 0.9999, which means 99.99% of the variation can be explained by the model. F-ratio is the ratio of the mean square of the regression to the estimated variance, and the zero p-value means the ratio is very significant. However, one can not conclude that the model fits the data well just by looking at this table. Further analysis is necessary to assess the model.

The simplest and most informative method for assessing the fit is to plot the response against the fitted values, and also examine the residuals. Fig. 3 shows the predicted values versus the simulation data. The straight line indicates good fitting. Fig. 4 is the normal plot of the residual, and it gives no reason to doubt that the residuals are normally distributed. Since the minimum value of C_{22} is 0.33 (scaled by 1E-16), the ratio of the residual standard error over the minimum of simulation data C_{22} is just 0.5% (0.0017/0.33).

The above analysis shows that the model fits the data very well, the regression is significant, and the residuals appear normally distributed. This underscores the usefulness of the

TABLE I
STATISTICS OF MODELING RESULT OF C_{22} MODEL IN FIG. 1

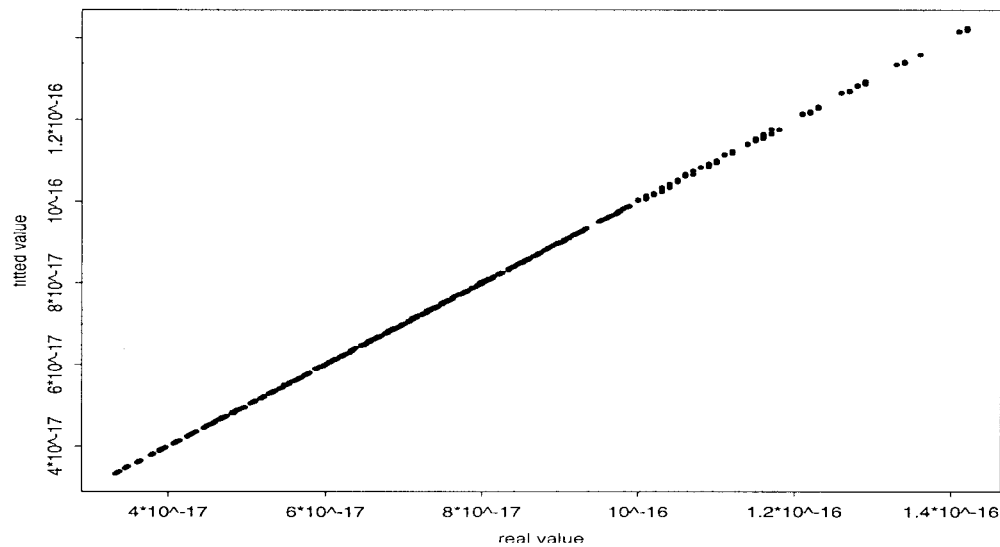| Source	Sum of Squares	Degree of Freedom	Mean Squares	F-ratio	Prob>F
Model	91.1037	47	1.938376	613700	0
Error	0.00542	1716	3.158eE-6	$R^2 = 0.9999$	
Total	91.109	1763		$\sigma = 0.00177$	

Fitted vs Real data

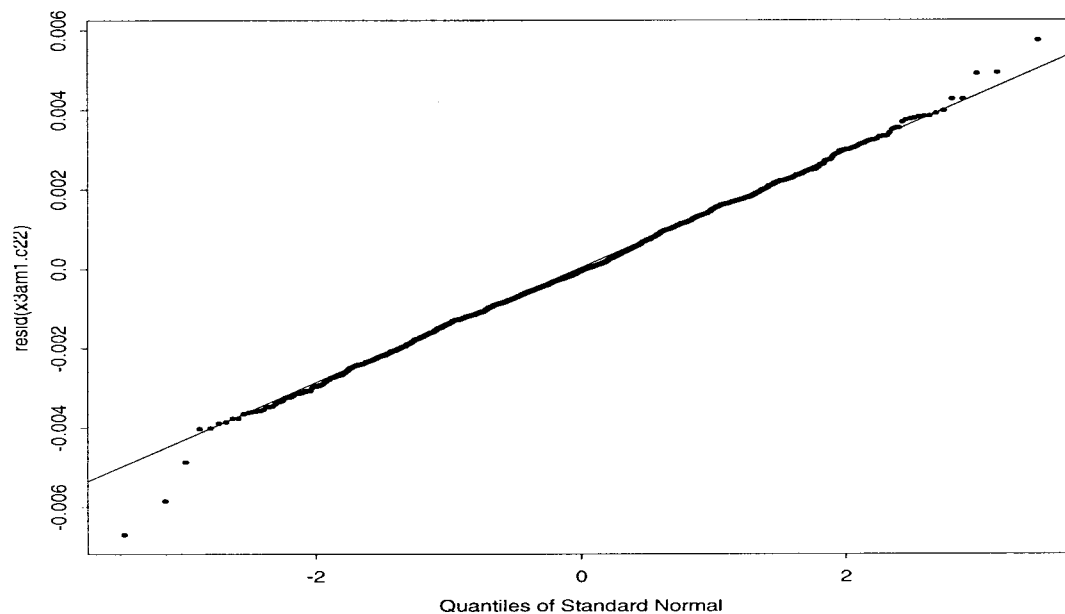Fig. 3. Fitted values against simulated data of C_{22} of Fig. 1.

Fig. 4. Normal plot for residuals of the fitting model of C_{22} of Fig. 1.

technique. The modeling of C_{12} using the same technique shows similar results.

To summarize this section, we discussed the issues of interconnect modeling for the purpose of the sensitivity study.

An efficient technique of curve fitting is discussed in detail, and a specific fitting problem is solved as an example. We also presented a methodology to build a parameterized interconnect model library.
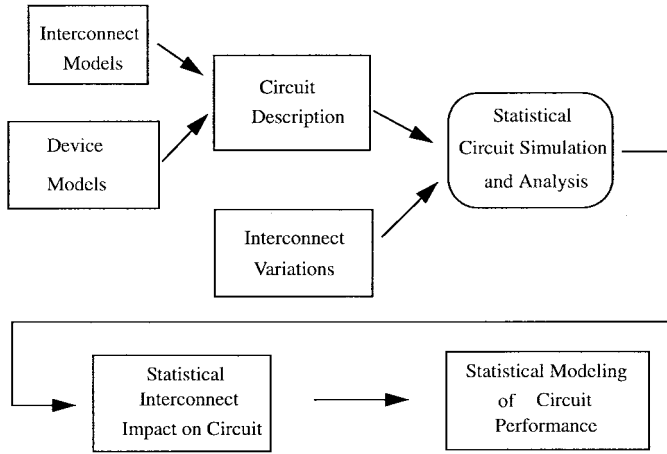
Fig. 5. Overview of sensitivity study based on interconnect model library.

Fig. 6. Circuit diagram of a ring oscillator.

Based on the interconnect model library built, we are ready to develop an approach to study the circuit sensitivity to interconnect variations. This is discussed in Section III.

III. SENSITIVITY STUDY

The models developed in last section, and the established range values for interconnect parameters are the essential ingredients for the evaluation of the impact on circuit performance. In this section, an approach to accomplish this evaluation will be explored, and the relationships between interconnect parameter variations and circuit performance will be developed.

The goal of statistical circuit design is to model and improve parametric yield [15]. The underlying concept is that variations in the manufacturing process change the performance of the integrated circuit and therefore cause the performance yield fluctuations seen in the final test. As stated in Section I, a new approach needs to be developed since active devices and interconnect wires are different in many aspects. To incorporate interconnections into the framework, the manufacturing line variations must be mapped into the variations of both devices and interconnect parameters, and then be mapped into the performance variations of circuits.

A. Methodology

An overview of the methodology to perform circuit sensitivity to interconnect variations is shown in Fig. 5. The basic idea is to model each interconnect wire of a circuit using the parameterized interconnect models developed in Section II, and then generate the circuit description based on a SPICE file. The generated circuit description contains closed-form analytical expressions for each interconnect capacitance and resistance elements, and it is the basis of the statistical circuit simulation.

To simulate the effect of process variations on a circuit, the connection between the process parameters and the input file to circuit simulator must be established. So the RC model for each interconnect wire should be expressed in terms of the interconnect parameters. With the help of the interconnect model library developed in the last section, the
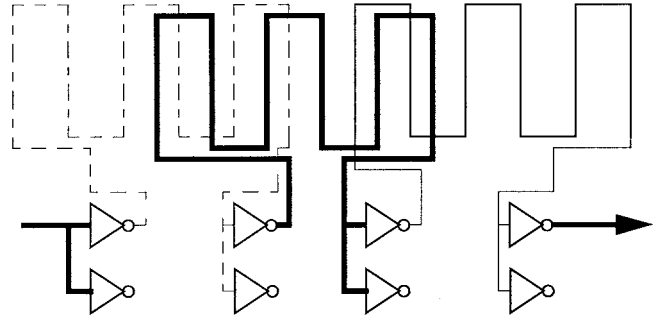
total capacitance and resistance of each interconnect wire can be easily described given the length of each wire, thus an RC model of each wire is built. The resulting description of the interconnect wires in a circuit usually takes the form of an RC mesh because of the coupling capacitance among neighboring wires.

We use the HSPICE circuit simulator to estimate circuit performance. Our work does not use formal optimization techniques to improve yield as the focus of this work is on the sensitivity analysis. More specifically, our goal is to determine the impact of interconnect related process parameters on performance.

The variation ranges of interconnect parameters form a multidimensional region which is referred to as a *parameter space*. This parameter space will be mapped to the variation ranges of the performance which is referred to as the *performance space*.

B. Case Study: Ring Oscillator Circuit

A ring oscillator was used to explore the sensitivity analysis approach. Fig. 6 shows part of the circuit diagram of the ring oscillator, which emphasizes the interconnect wires between stages. The loading of the circuit is dominated by interconnect wires, as indicated in Fig. 6. The interconnection length for each stage is 180 μm, and is divided into six fingers. Three of the fingers are next to previous stage fingers and the other three are next to next stage fingers, so there is a heavy capacitive coupling effect between neighboring stages.

The ring oscillator circuit used in this study has nine stages, with fan-out of 2. However, the design is such that significant loading is contributed by interconnect wires. In this way, the signal delay t_p between each stage is mainly determined by the interconnect capacitance and resistance.

First, the SPICE netlist is generated based on its layout using the extraction tool. Then, it is modified so that interconnect wires of the circuit are modeled in terms of the interconnect parameters. For example, coupling capacitance is modeled explicitly in terms of the length and distance of the wires. The regularity of this relatively simple ring oscillator circuit makes it easier to accomplish this modification. The fingers are parallel and have the same width and the same interwire space. By generating the circuit description in this way, a direct link between the circuit performance and interconnect parameters is established.
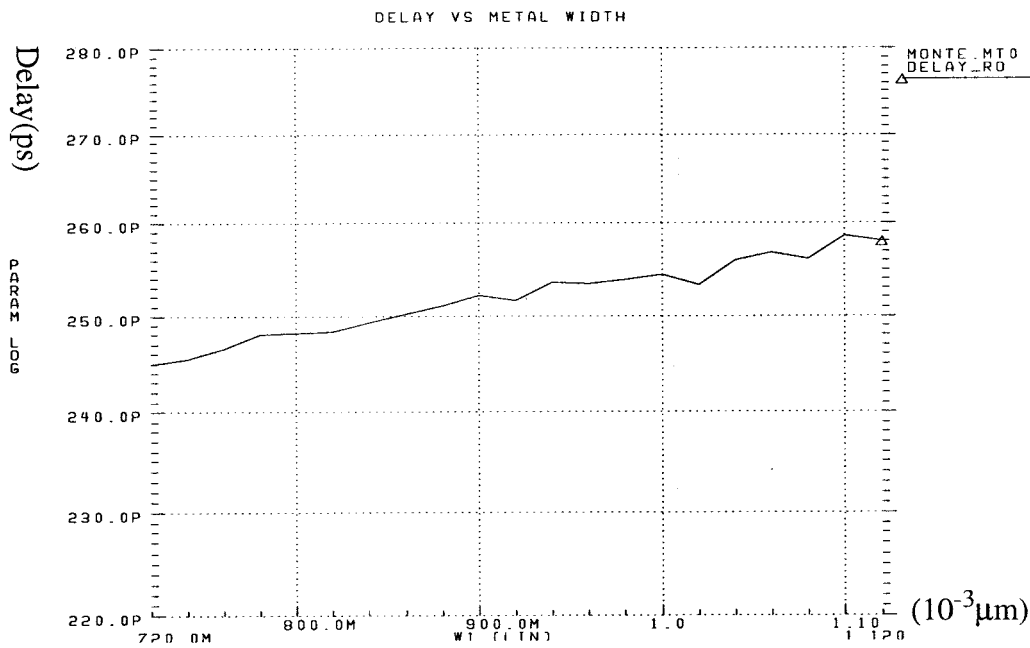
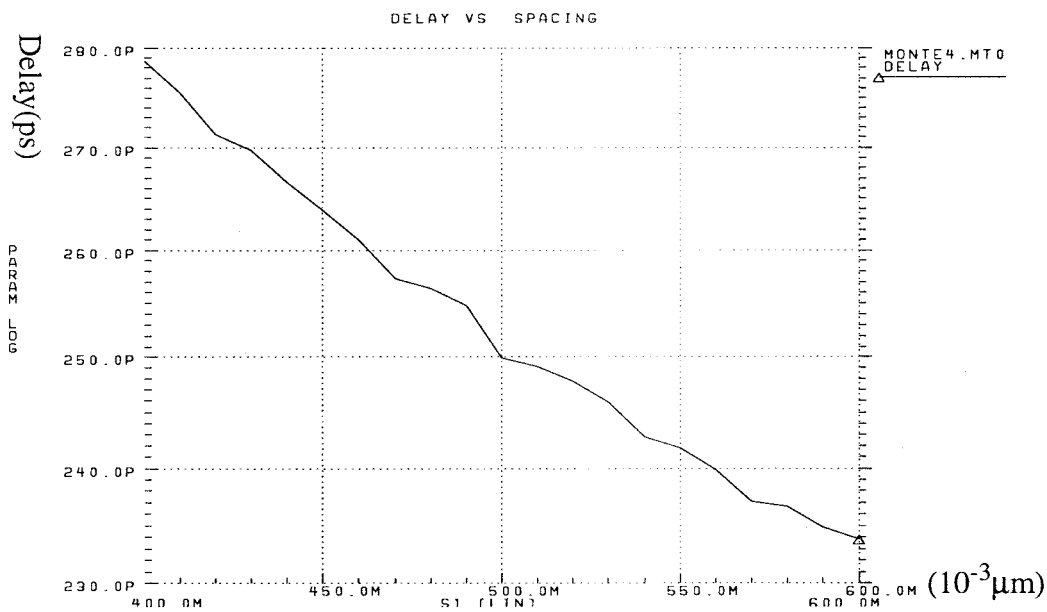Fig. 7. Ring oscillator delay versus metal width.

Fig. 8. Ring oscillator delay versus interwire spacing.

C. Results and Analysis

The ring oscillator circuit is simulated using HSPICE. The sensitivity of the delay to a particular parameter is evaluated by varying it over a reasonable range with the other parameters fixed. For example, the delay sensitivity to metal thickness is obtained by fixing the ILD thickness, metal width and metal spacing and varying the metal thickness over $\pm 20\%$ variation range.

Figs. 7–10 show the simulation results of the delay sensitivity to the wire width, interwire spacing, ILD thickness and metal thickness, respectively. The roughness of the curves is caused by numerical discretization within HSPICE. Table II

summarizes these results. It indicates that interwire spacing is the most sensitive parameter. Twenty percent variation of the interwire spacing from its nominal value will lead to 8.8% deviation of the delay. On the other hand, the circuit is not sensitive to the variation of the ILD thickness in the range of the simulation.

The lack of sensitivity to ILD thickness is because the delay is not sensitive to the plate capacitance. In fact, for this circuit, the delay is mostly sensitive to interwire coupling capacitance as can be seen in Fig. 12. Actually, this is original intention of the ring oscillator layout.

To get further insight and generalize the methodology, Monte Carlo simulations are also set up to perform statistical
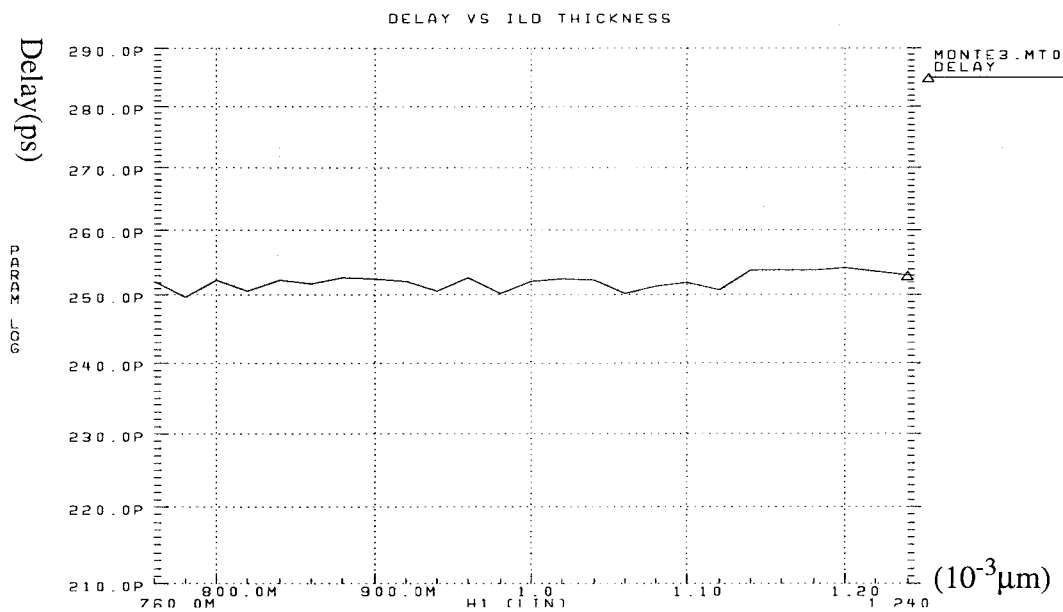
DELAY VS ILD THICKNESS

Fig. 9.   Ring oscillator delay versus ILD thickness. The layout of the ring oscillator is designed such that the delay is mainly determined by the coupling capacitance between neighboring wires instead of plate capacitance.
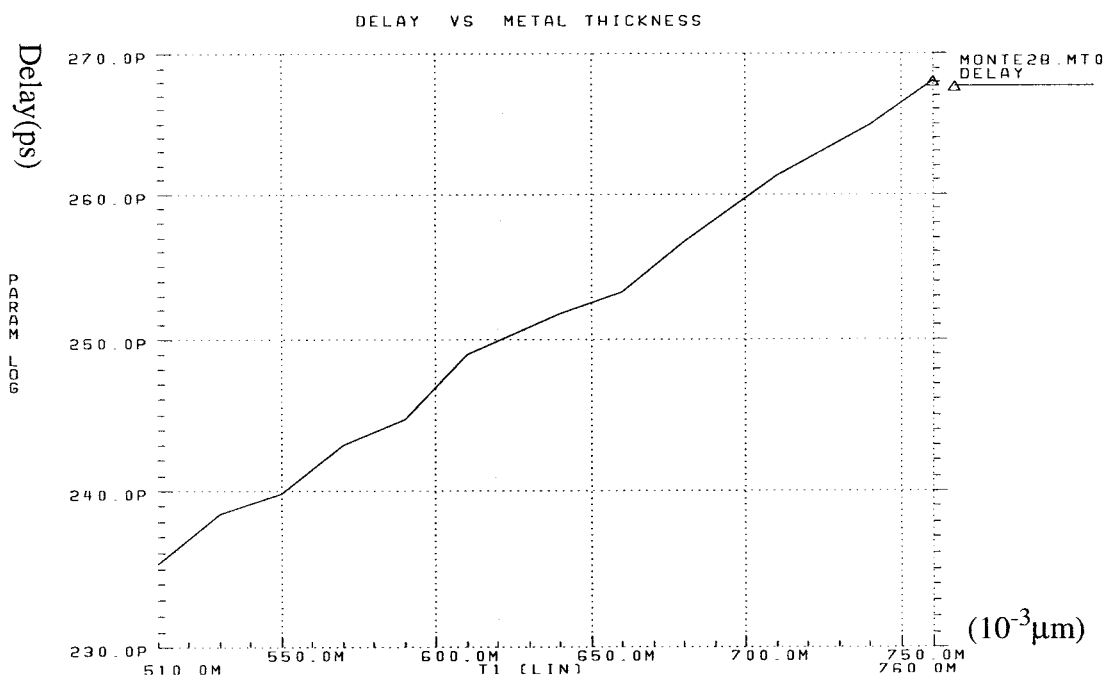
DELAY   VS   METAL THICKNESS

Fig. 10.   Ring oscillator delay versus metal thickness.

TABLE II
RESULTS OF SENSITIVITY STUDY OF RING OSCILLATOR

Parameter	Parameter range (μm) (20% variation)	Impact on Delay
Metal width	0.810-0.990	2.6%
ILD thickness	0.842-1.029	0.0%
Metal thickness	0.572-0.699	4.6%
Inter-wire spacing	0.450-0.550	8.8%

analysis. These statistical simulations closely reflect what happens in the real world. The simulation results establish a connection between performance spread and the variation of parameters.

The Monte Carlo simulation is performed based on the assumption that all interconnect parameters (there are four parameters in this study) are normally distributed with 3σ equal to 20% of their nominal values. These results are consistent with the previous deterministic analysis. Particularly, Fig. 11 shows the significant sensitivity of interwire spacing with respect to the delay.
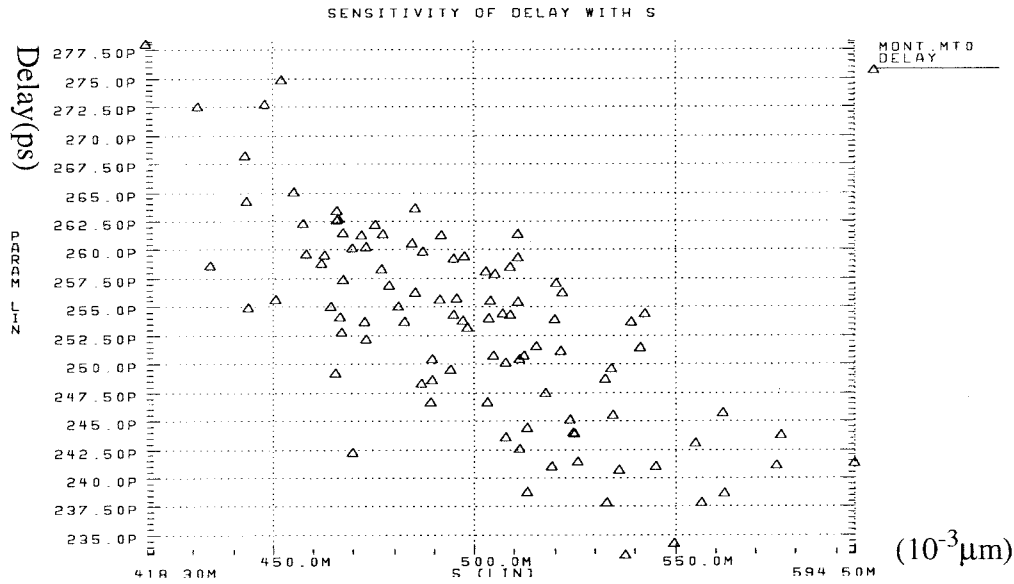
Fig. 11.   Monte Carlo simulation result: delay sensitivity to interwire spacing of ring oscillator.
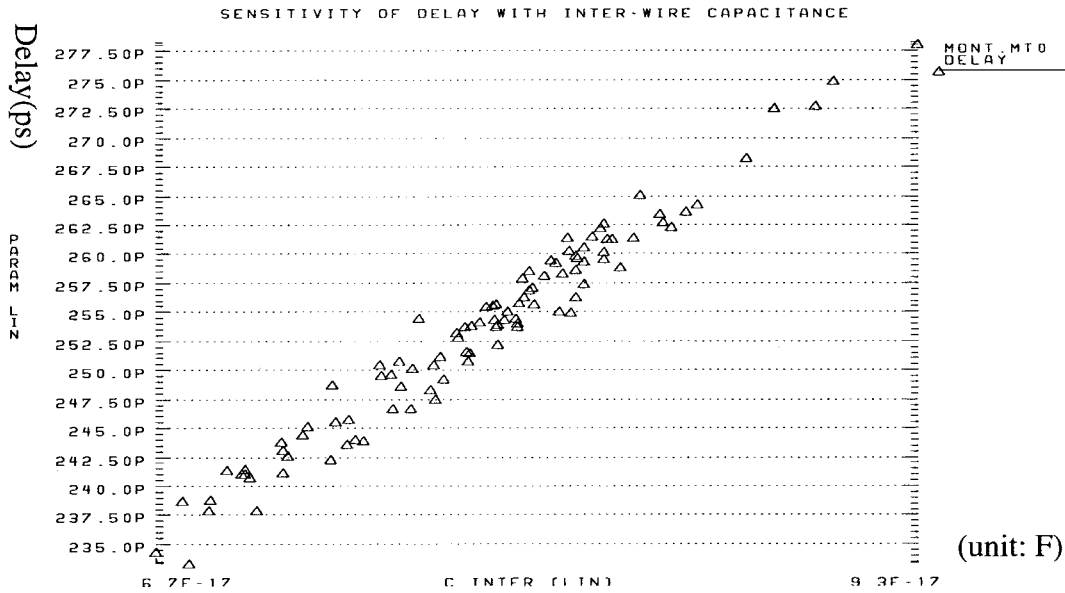

Fig. 12.   Monte Carlo simulation result: delay sensitivity to unit-length interwire coupling capacitance of ring oscillator.

Interconnect variations lead to the change of interconnect resistance and capacitance, including both plate capacitance and coupling capacitance, and affect the delay of the circuit. Particularly, Fig. 12 demonstrates the importance of the coupling capacitance with regard to the delay.

D. Summary and Discussion

In this section, the issues related to statistical circuit design are discussed, and an approach to study circuit sensitivity to interconnect parameter variations is developed using parameterized interconnect model library. The circuit netlist is modified to include explicit parameterized expressions of interconnect parasitics as a function of layout and technology parameters. The results from the study of a ring oscillator circuit reveal that the delay of this ring oscillator is the most sensitive to interwire spacing while least sensitive to ILD thickness.

There were several advantages to this approach. First, it made the sensitivity study much easier without going through the time-consuming and error-prone process of on-line whole chip circuit extraction. Second, when studying the effect of the spatially distributed variations, this approach will be a good candidate since interconnect wires can be modeled separately using different models at different positions. Third, the sensitivity to circuit design or layout parameters can be evaluated easily via this approach. Finally, when studying a complicated large circuit such as a microprocessor, some simple circuits that closely resemble the statistics of a microprocessor circuit can be analyzed using the above approach. In such a way, we
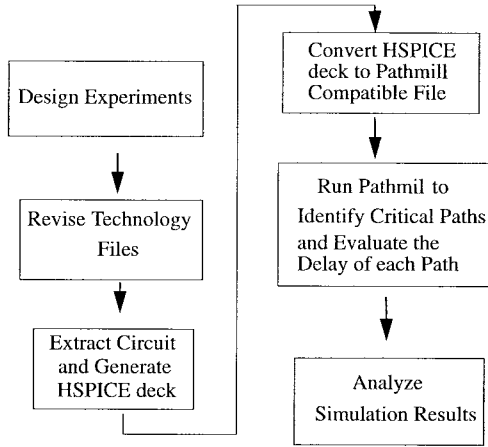
Fig. 13. The methodology of sensitivity study using statistical experiment design.

can evaluate and forecast the performance spread of the microprocessor resulting from interconnect parameter variations before the manufacturing of the product die.

However, there are some limitations to this approach. It requires manual construction of an RC model for each interconnect wire, so it is not very suitable for studying a complicated and irregular, circuit directly. It is inefficient to manually model the whole circuit. So, an alternative approach is developed in next section to study the impact of process variations of interconnect technology parameters on circuit performance.

IV. SENSITIVITY STUDY USING STATISTICAL EXPERIMENTAL DESIGN

In this section, we will show how a sensitivity analysis could be carried out for a complex circuit that does not have the regularity.

As technology advances, the number of interconnect layers increases, and the configuration of interconnect becomes more and more complicated. Since there are many parameters of interest in multilayer interconnect technology, and the cost of full-chip simulation is very high, statistical experiment design techniques become very useful in carrying out the computer simulations that explore the sensitivities of interest.

A. Methodology

The basic idea of this approach is that given the variation ranges of the technology parameters, the technology file which contains all the technology parameters is revised according to the experimental design. Then, different circuit description files are generated from each revised technology files. The circuit description files are HSPICE decks. They are fed into the circuit simulator to evaluate the performance of the circuit. Specifically, the flow of this approach is shown in Fig. 13 and is listed as follows.

1) Design experiments with interconnect parameter variables, and construct the design matrix.
2) Revise the technology file based on the design matrix for each designed experiment.

3) Extract the parasitics of the circuit from the layout given each revised technology file, and generate an HSPICE deck.
4) Convert the HSPICE deck to Epic compatible input file. Run Pathmill[2] to identify the critical paths and evaluate the delay of each critical path.
5) Perform statistical analysis based on the simulation results of the extracted critical paths. Model the delay of the critical path.

A 32-bit shift-and-add multiplier circuit is used as a study case. This circuit has three metal layers and one poly layer, as shown in Fig. 14. The variables of interest are listed as follows.

t_1, t_2, t_3, t_4 Thickness of poly, metal1, metal2, and metal3, respectively.
h_1 Field oxide thickness.
h_2 ILD thickness between poly and metal1
h_3 ILD thickness between metal1 and metal2.
h_4 ILD thickness between metal2 and metal3.

B. Screening Experiment

The purpose of the screening experiment is to investigate the most sensitive and important factors among the eight parameters listed above, with respect to the performance variation. The range of each parameter was chosen to effectively encompass its possible variation range during regular production. A full factorial experiment to determine all effects and interactions for the eight factors would require 2^8, or 256 experiments. In order to reduce the experimental budget and simulation cost, the effects of higher order interactions were neglected and a 2^{8-4} fractional factorial design requiring only 16 runs was performed.

The analysis of screening experiment results revealed that only two of the eight variables have large effects[3] on the circuit performance: ILD thickness between poly and metal 1 and ILD thickness between metal1 and metal2, i.e., h_2 and h_3.

The result also shows that interconnect wires play an important role in determining the critical path delay of this multiplier. This will be further analyzed in the subsequent subsections.

Since variation of circuit performance is mainly due to the variation of capacitance, the results show that h_2 and h_3 can explain most of the variations of the capacitance.

It should be noted that the above result is much circuit dependent, and even layout dependent to some extent. So different categories of circuits will exhibit different sensitivities to interconnect parameters. Even for the same circuit, the sensitivity analysis results may be different with different technologies, or with the same technology but different layouts. This is because the routing layers and length of each layer may be much different. So the results from the analysis

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[2] Pathmill is a CAD tool from Epic Inc., used to identify the critical paths of a circuit.

[3] Since this is a computer simulated experiment, lacking experimental error, it is meaningless to talk about *statistical* significance. We used traditional ANOVA techniques for the analysis with the understanding that the residuals are the result of under modeling. The ANOVA was used to help us identify the important factors.
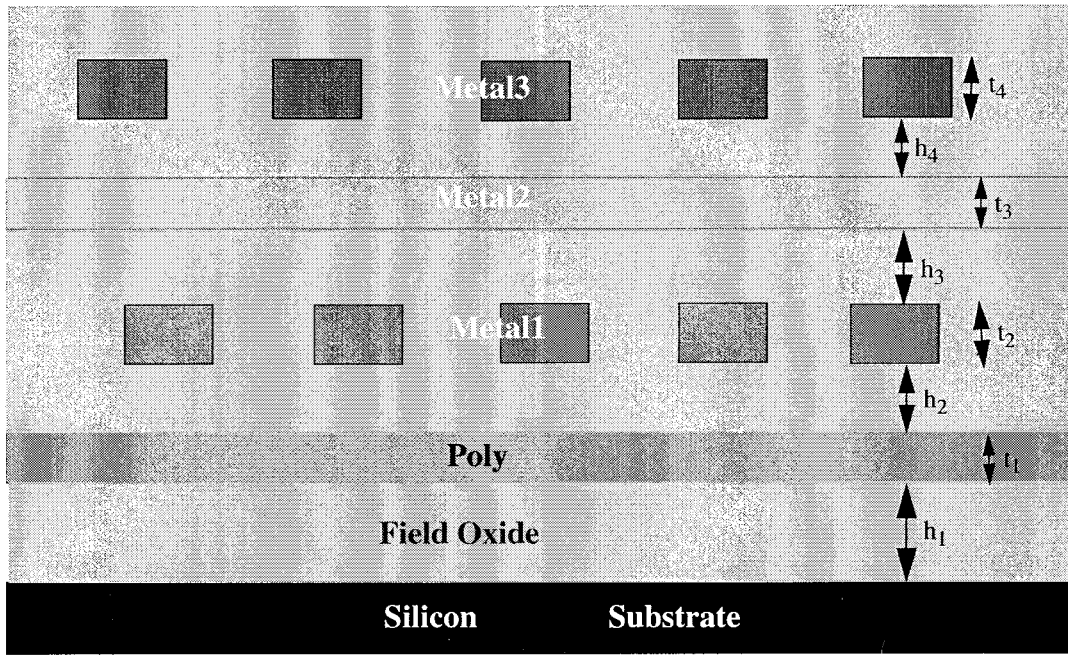
Fig. 14.   Illustration of multilayer interconnect structure of the multiplier circuit.

TABLE III
CAPACITANCE LOADING DISTRIBUTION OF THE MULTIPLIER CIRCUIT

	Percentage of Loading
Interconnect Capacitance	75%
Gate Capacitance	13%
Junction Capacitance	12%

TABLE IV
CRITICAL PATH DELAY SENSITIVITY OF
MULTIPLIER CIRCUIT TO THE MAIN FACTORS

Parameter	h_2 (μm)	h_3 (μm)	C_{gate} (F/m^2)
Variation range	0.54 - 0.66	0.72 - 0.88	4.8607 - 59401.43
Impact on delay	8.99%	5.24%	5.9%

of one circuit can not be simply generalized for even the same style of circuits without further analysis of the statistics of the circuit. The results of the sensitivity study will be more helpful and useful when linked to a detailed analysis of the circuit loading distribution, such as gate capacitance, diffusion capacitance, capacitance contributed by interconnect, and even the capacitance associated with different metal layers.

To compute the total gate capacitance, diffusion capacitance (includes junction capacitance and side-wall capacitance) and interconnect capacitance, we started from the HSPICE deck, evaluated the relevant geometry to calculate the various loading capacitances. Table III shows the loading distribution of this circuit in the nominal case, and it indicates that interconnect wires dominates the loading of the circuit. This is in agreement with the screening experimental results.

C. Second-Phase Experiment Design

Based on the results of the screening experiment, a second experiment is designed which takes both device and interconnect variations into consideration. There are four variables in the design: C_{gate}, $C_{\text{diffusion}}$, h_2, and h_3. $C_{\text{diffusion}}$ is the summation of unit area bottom junction capacitance and side-wall capacitance and C_{gate} is the unit area gate capacitance. The junction capacitance and side-wall capacitance were treated as a single factor since they are highly correlated. A full factorial

design would need 16 runs, so a 2^{4-1} fractional factorial design with only eight runs was used.

The experiment result reveals the significant effect of h_2, h_3, and C_{gate} on circuit performance, among which the effect of h_2 is the most prominent.

D. Central Composite Design and Model Building

Recall that the goal is to understand the impact of the variations of interconnect related technology parameters on circuit performance. We are interested to investigate how these parameters will affect the interconnect capacitance, and how the interconnect capacitance relates to circuit performance. So in the next section, we will build models to link the parameter variations with circuit performance.

In order to obtain the model, it is necessary to augment the data gathered with seven additional runs which employed a central composite design. In this design, the two-level factorial "box" was enhanced by further experiments at the center as well as symmetrically located "star" points [24].

Combining the results of 15 runs (second phase experiment and central composite design), the regression model is fitted:

$$\text{Delay} = 1.686975/h_2 + 1.309948/h_3$$
$$+ 5400.86 C_{\text{gate}}(h2, h3: \text{micron}, C_{\text{gate}}: \text{F/M}^2).$$

$$(10)$$

TABLE V
ANOVA TABLE OF THE CRITICAL PATH DELAY REGRESSION MODEL OF THE MULTIPLIER CIRCUIT

Source	Sum of Squares	Degree of Freedom	Mean Squares	F-ratio	Prob>F
Model	699.3331	3	1.938376	549.2	0
Error	0.0054	12	3.158eE-6	$R^2 = 0.9928$	
Total	91.109	15			

Based on the above regression model, the sensitivity of delay to each parameter is calculated and listed in Table IV.

The data transformation of h_2 and h_3 in the above model is suggested by physical intuition. The ANOVA table for the model is shown in Table V, which reveals the goodness of fit of the model. It also shows that the model can explain up to 99% of the variations of the delay.

E. Conclusion

In this section, we developed an approach using statistical design techniques to study the effects of interconnect parameter variations on the performance of a large, complicated circuit. With two experiments, the most significant factors are isolated, and the model is fitted via a central composite design. The results from the case study of a shift-and-add multiplier revealed the significance of ILD thickness. The loading distribution of the circuit was also analyzed and correlated with the results.

V. SUMMARY AND CONCLUSION

A. Summary

The main goal of this work is to present interconnect modeling techniques and develop approaches to study the circuit sensitivity to interconnect parameter variations. In this work, two different approaches are developed and are explored with a ring oscillator and a multiplier circuit, respectively.

In Section II, we discussed interconnect modeling issues in detail and presented a methodology to build an interconnect model library.

The first approach presented in Section III is based on the parameterized interconnect model library. This approach can capture the effects of both layout and technology parameter variations. This approach is suitable for studying spatially distributed variation effects. A ring oscillator circuit was studied using this approach. The limitation of this approach is its inefficiency to study a complicated real circuit unless an automated method can be found to pick up the right model for each interconnect wire.

In Section IV, we developed another approach which uses statistical design techniques. This approach is suitable for the sensitivity study of a large and complicated circuit. A multiplier circuit is studied using this approach. The disadvantage of this approach is that it requires multiple time-consuming circuit extraction steps.

An important point is that in order to make a general conclusion for one category of circuits, a reasonably large number of circuits must be studied. Since these circuits must have similar characteristics, one must attempt a meaningful taxonomy of like circuits. The conclusion from the result of one circuit will be meaningful for the same family of circuits only if one is able to define such a family.

B. Future Work

A possible direction of future work would be to make the process of sensitivity study automatic without much manual work. This can be extended from the first approach discussed in Section III. The main challenge is to generate the circuit description more efficiently, or even automatically, and describe the interconnect in a way suitable for sensitivity study.

Also, integration with variation models in the study will make the sensitivity study results more convincing.

Another direction of this work would be to study the problem from a higher level of the design flow, such as the logic level.

REFERENCES

[1] G. Anderson and P. Anderson, *The UNIX[TM] C Shell Field Guide.* Englewood Cliffs, NJ: Prentice-Hall, 1986.
[2] C. Yu, "Integrated circuit process for manufacturability using enhanced metrology," Ph.D. dissertation, Univ. California, Berkeley, 1995.
[3] G. Coatache, "Finite element method applied to skin-effect problems of instrip transmission lines," *IEEE Trans. Microwave Theory Technol.,* vol. MTT-35, Nov. 1987.
[4] A. Zemanian, "A finite-difference procedure for the exterior problem inherent in capacitance computations for VLSI interconnections," *IEEE Trans. Electron Devices,* vol. 35, July 1988.
[5] A. Zemanian and R. Tewarson, "Three-dimensional capacitance computations for VLSI/ULSI interconnections," *IEEE Trans. Computer-Aided Design,* vol. 8, pp. 1319–1326, Dec. 1989.
[6] W. H. Press, S. A. Teukolsky, W. T. Vetterling, and B. P. Flannery, *Numerical Recipes in C,* 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 1992.
[7] S. Y. Oh, *Interconnect Modeling and Design in High-Speed VLSI/ULSI Systems.*
[8] C. Mead and L. Conway, *Introduction to VLSI Systems.* Norwell, MA: Addison-Wesley, 1980.
[9] P. Yang, D. Hocever, P. Cox, C. Machala, and P. Chatterjee, "An integrated and efficient approach for MOS VLSI statistical circuit design," *IEEE Trans. Computer-Aided Design,* vol. CAD-5, pp. 5–14, Jan. 1986.
[10] A. E. Ruehli, *Circuit Analysis, Simulation and Design.* Amsterdam, The Netherlands: Elsevier, 1987.
[11] W. Maly, A. J. Strojwas, and S. W. Director, "VLSI yield prediction and estimation: A unified framework," *IEEE Trans. Computer-Aided Design* vol. CAD-5, Jan. 1986.
[12] Selected papers on *Statistical Design of Integrated Circuits.* New York: IEEE Press, 1987.
[13] E. D. Boskin, "A methodology for modeling the manufacturability of integrated circuits," Ph.D. dissertation, Univ. California, Berkeley, 1995.
[14] D. E. Hocevar, P. F. Cox, and P. Yang, "Computing parametric yield accurately and efficiently," in *Proc. ICCAD,* 1990, pp. 116–119.

[15] J. C. Zhang and M. A. Styblinski, "Design of experiments approach to gradient estimation and its application to CMOS circuit stochastic optimization," in *Proc. ISCAS,* Singapore, 1991, pp. 3098–3101.
[16] Z. Daoud, "DORIC: Design of optimized and robust integrated circuit," M.S. thesis, Univ. California, Berkeley, Dec. 1993.
[17] R. Spence and R. S. Soin, *Tolerance Design of Electronic Circuits.* Norwell, MA: Addison-Wesley, 1988.
[18] H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI.* Norwell, MA: Addison-Wesley, 1990.
[19] R. H. Dennard *et al.,* "Design of ion implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits,* vol. SC-9, Oct. 1974.
[20] K. Nabors, "FastCap: A multiple accelerated 3-D capacitance extraction program," *IEEE Trans. Computer-Aided Design,* vol. 10, pp. 1447–1459, Nov. 1991.
[21] U. Choudhury *et al.,* "An analytical-model generator for interconnect capacitances," in *Proc. IEEE CICC,* 1991.
[22] K. J. Chang, S. Y. Oh, and K. Lee, "HIVE: An efficient interconnect capacitance extractor to support submicron multilevel interconnect designs," in *Proc. ICCAD,* 1991.
[23] TMA, Inc., *Raphael User's Manual,* 1996.
[24] G. E. P. Box, W. B. Hunter, and J. S. Hunter, *Statistics of Experimenters.* New York: Wiley, 1978.

Zhihao Lin was born in China in 1969. He received the B.S. degree in electrical engineering and economics (minor) with honors from Tsinghua University, China, in 1992 and the M.S. degree from the University of California at Berkeley in 1997, where he was working on interconnect modeling and sensitivity study of C interconnect variations on circuit performance in the Berkeley Computer Aided Manufacturing (BCAM) group.

He is currently with NeoParadigm Labs, Inc., San Jose, CA, a system-level IC company. His research interests include the submicron interconnect modeling, mixed-signal circuit design, application-specific circuit design, and the application of statistical analysis in the design and manufacturing of integrated circuits.

Costas J. Spanos (S'77–M'85–SM'96) was born in Piraeus, Greece, in 1957. He received the Electrical Engineering Diploma with honors from the National Technical University of Athens, Athens, Greece, in 1980 and the M.S. and Ph.D. degrees in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, in 1981 and 1985, respectively, working on the development of statistical technology CAD systems.

From June 1985 to July 1988, he was with the Advanced CAD Development group, Digital Equipment Corporation, Hudson, MA, where he worked on the statistical characterization, simulation, and diagnosis of VLSI processes. In 1988, he joined the faculty of the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, where he is now a Professor. He has been the Director of the Berkeley Microfabrication Laboratory since 1993. He has taught and published (more than 50 refereed papers) extensively in the area of applied statistical techniques for the improvement of semiconductor manufacturing technologies. His research interests included the development of flexible manufacturing systems, the application of statistical analysis in the design and fabrication of integrated circuits, and the application of computer-aided techniques in semiconductor manufacturing.

Dr. Spanos has served on the technical committees of the IEEE Symposium on VLSI Technology, the International Semiconductor Manufacturing Science Symposium, and the Advanced Semiconductor Manufacturing Symposium. He was the Editor of the IEEE Transactions on Semiconductor Manufacturing from 1991 to 1994. He received the Best Academic Paper Award from the International Semiconductor Manufacturing Science Symposium in 1992.

Linda S. Milor (S'86–M'90), for photograph and biography, see this issue, p. 545.

Y. T. Lin, photograph and biography not available at the time of publication.