# Fast Extraction of Defect Size Distribution Using a Single Layer Short Flow NEST Structure

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*Abstract*—Defect inspection is required for process control and to enhance chip yield. Electrical measurements of test structures are commonly used to detect faults. To improve accuracy of electrically based determination of defect densities and defect size distributions, we present a novel NEST structure. There, many nested serpentine lines will be placed within a single layer only. This mask will be used as a short flow to guarantee a short turn around time for fast process data extraction. Data analysis procedures will provide densities and size distributions of killer defects that will have an impact on product chip yield.

*Index Terms*—Semiconductor devices, test structures, yield estimation, yield optimization.

## I. INTRODUCTION

**D**EFECTS (e.g., particles) can cause electrically measurable faults (killer defects) dependent on the chip layout and the defect size. These faults are responsible for manufacturing related malfunction of chips. So, defect density and size distributions are important for yield enhancement and to control quality of process steps and product chips [5]. Test structures are used to detect faults and to identify and localize defects.

The double bridge test structure was proposed by [4] to extract size distributions based on electrical measurements. But this test structure design requires two conducting layer having different resistivity. Thus, this design is limited to one polysilicon layer and one metal layer. The Harp test structure was proposed by [3] which may be used for any kind of layers, but even here at least two layers are necessary to design it which may slow down the data extraction procedure.

To enable the shortest possible manufacturing time, we have developed a short loop test structure using just one mask step to enable a fast extraction of densities and size distributions of killer defects that have a detrimental impact on the yield of product chips. Section II describes the design principle of the NEST structure, which enables the extraction of the size of each detected defect. Section III introduces the algorithms to determine a defect size distribution. Section IV discusses the accuracy of these algorithms using Monte Carlo simulations. Finally, we present some experimental results and our conclusions.
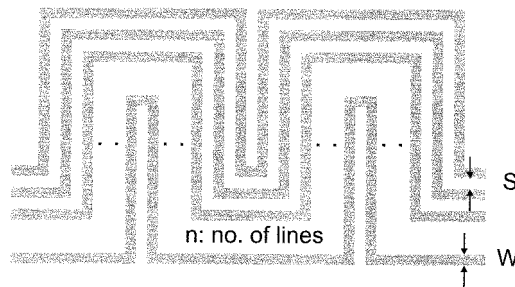
Fig. 1. Principle design of a single layer NEST structure.

## II. DESIGN PRINCIPLE OF THE NEST TEST STRUCTURE

Parallel lines—each connected to two pads—will be implemented inside a test structure to electrically determine a defect size distribution. If a defect occurs and causes an electrically measurable fault, either two or more test structure lines will be shorted or one or more test structure lines will be opened. The more test structure lines are involved, the larger the defect that caused this measured fault. In a 2-by-$N$ pad frame the number of pads is very limited. To enable the detection of opens and shorts, each test structure line has to be connected to two pads. So, only $N$ lines may be implemented that does not fill a large chip area that is needed to detect random defects. For this reason, the lines are designed as serpentines to fill the complete test chip area. Fig. 1 shows the principle design of such nested serpentine lines, which is based on a structure proposed by [1]. Compared to our approach using a high number of nested serpentine lines, [1] just used 5 serpentine lines within two combs. He implemented several structures having different dimensions to determine a defect size distribution by comparing the number of detected defects dependent on the dimension of the structures. Having a high number of nested serpentine lines enables the direct extraction of defect size distribution by comparing the number of detected defects dependent on the number of involved lines.

Each NEST structure will be connected to a 2-by-$N$ pad frame. Fig. 2 shows a complete NEST structure design, which was automatically generated in just a few seconds. To design a NEST structure there are three main constraints that have to be satisfied.

1) To prevent the problem of disentangling multiple defects within a NEST structure, there should not be more than one defect within a bundle of lines with a very high probability. Consequently, the area per NEST structure should be limited such that no more than one defect will be expected within a NEST structures. Since defect density is measured in number of defects per area, the maximal NEST structure area corresponds to the area in which one defect will occur. Initially the detailed defect density is
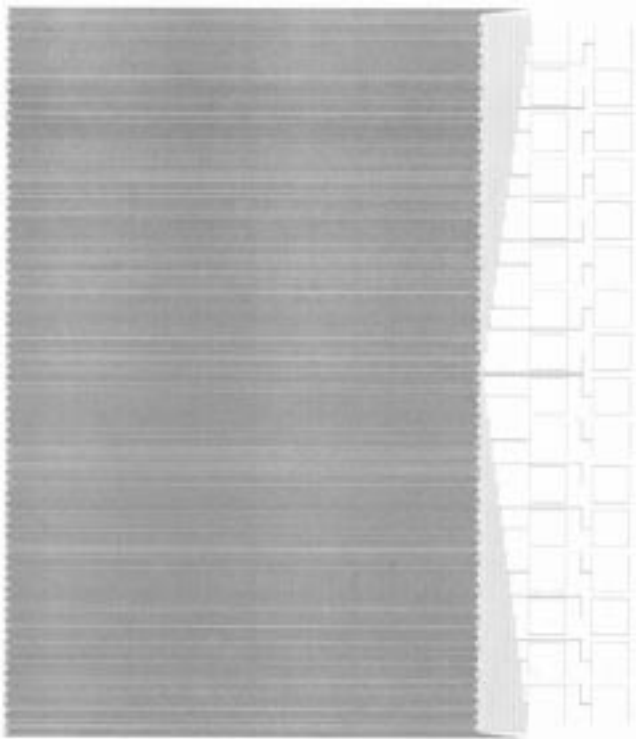
Fig. 2. Design of a NEST structure containing 3104 parallel lines in a single metal layer.
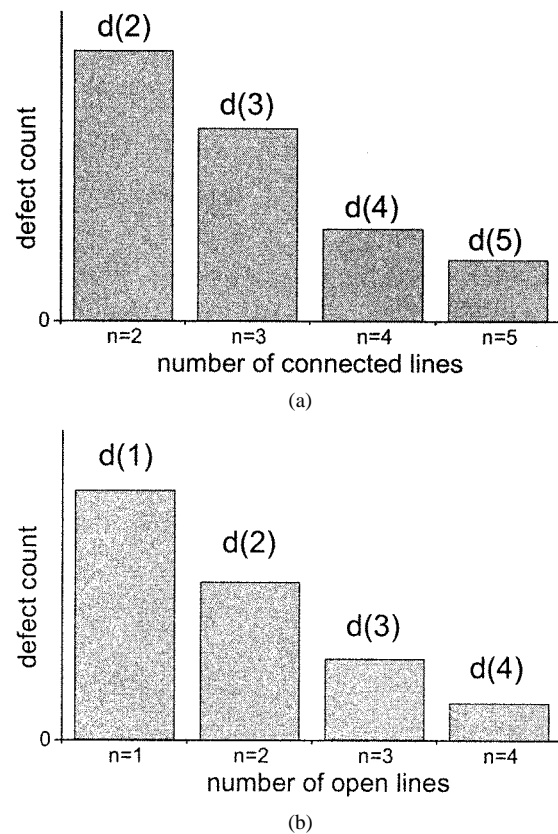


(a)



(b)

Fig. 3. (a) Number of defects that have caused short circuits and (b) number of defects that have caused open circuits, both dependent on the number of lines.

unknown, but usually an expected value can be obtained from previous technologies. To be on the safe side, it is recommended to use just half the maximal NEST structure area, if it is based on an estimated defect density and not on a measured defect density value.

2) To keep the NEST structure measurable, the resistance value per line should be within the limits given by the testing equipment.

3) Testing time should be within a given limit per wafer, which will give the maximum number of pad frames and NEST structures that may be implemented within a die.

Given today's low expected defect densities, testing time usually is the main limitation for analog DC measurements using a parametric tester. For digital testing as described at [2] the line resistance usually is the main limitation for the NEST structure design. To get reliable data for yield prediction for deep submicrometer processes where the average defect density is below 0.5 defects per $cm^2$, a large portion of the total area of a test chip has to be covered with NEST structures. Simulations with different defect size distributions as well as analyzing data from several fabs lead to the following: For a complete lot of at least 20 wafers no less than 30% of the test chip area should be filled with NEST structures. If smaller lots with only 10–12 wafers are used, up to 50% of the test chip area is required for NEST structures.

## III. DATA ANALYSIS PROCEDURES

After briefly discussing the testing procedure of the NEST structure, we will describe the algorithms to extract the size distribution of such defects that have caused electrically measurable faults within NEST structures.

### A. Testing of Opens and Shorts

Open circuits will be tested by measuring the resistance between the two pads connected to a single line of a NEST structure. A given NEST structure of m lines will result in a vector with m values each standing for a detected open line. The order of the values in the vector corresponds to the order of the lines within the NEST structure. For instance, the vector {0,0,1,1,0,0,0,0,0,1,1,1,0,0,0,0} of a NEST structure containing $m = 16$ lines indicates that there are two open circuits. One open circuit is caused by a defect interrupting the lines 3 and 4. The second open circuit is caused by a defect interrupting the lines 10, 11, and 12.

Short circuits will be tested by measuring the resistance between two pads connected to adjacent lines. A given NEST structure of $m$ lines will result in a vector with $m$ values each standing for a line being involved in a short circuit. The order of the values in the vector corresponds to the order of the lines within the NEST structure. For instance, the vector {0,0,0,0,0,1,1,1,0,0,0,0,0,1,1,0} of a NEST structure containing $m = 16$ lines indicates that there are two short circuits. One short circuit is caused by a defect connecting the lines 6, 7, and 8. The second short circuit is caused by a defect connecting the lines 14 and 15. Based on this we can generate a histogram for open circuits as well as for short circuits as can be seen in Fig. 3.
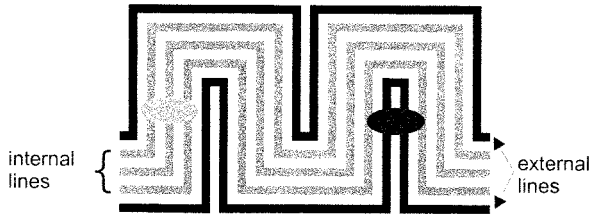
Fig. 4.    Defects shorting internal and external lines of a NEST structure.

### B. Defect Size Extraction of Shorts

In this section, we will describe in detail the procedure to extract a size distribution of such defects that have caused short circuits.

*1) Internal and External Lines:*  At [3] an algorithm was presented to extract a size distribution of defects causing short circuits within many electrically distinguishable parallel lines. A Harp test structure was used to provide such an environment. Within the NEST structure the electrically distinguishable lines are implemented as serpentines which will not always provide electrically distinguishable neighbored lines. In Fig. 4 these so called external lines are drawn as black lines. It can be seen that these lines only have an electrically "different" neighbor on one side while they are neighbored to themselves at the other side. Only the so called internal lines (gray lines in Fig. 4) have electrically distinguishable neighbored lines at all times.

The possible size of a defect will be different if external lines are involved or not. For instance a defect of a given size as can be seen on the left side of Fig. 4 may short three internal lines. If the same defect will hit an external line as can be seen on the right side of this Fig. 4, only two lines are shorted. So, only for those faults exclusively connecting internal lines we can use an algorithm based on [3], which will described in Section III-B2. To determine the defect size of those faults also including external lines, we will present a second algorithm in Section III-B3. Finally, both size distributions will be summarized in a total defect size distribution. To do so, we actually have to generate two histograms as shown in Fig. 3, one just containing the shorts of internal lines and a second one containing the shorts that also include external lines.

The external lines that are placed at the outer border of the entire NEST structure would theoretically require a third analysis method since they are only neighbored to one line. However, due to the size of the NEST structure the fraction of these lines versus all other lines is so small that this effect can be neglected.

*2) Algorithm for Internal Lines:*  The number of connected adjacent lines has to be transferred to a size distribution dependent on the design rules of the lines. For a given line width $w$ and space $s$, a defect that connects e.g., 2 lines may have a size in-between $s$ and $s + 2(w + s)$. In general, a defect connecting $n \geq 2$ lines may have a size in-between $[s + (n - 2) \cdot p, \ s + n \cdot p]$ where $p$ is defined as the line pitch.

$$p = w + s. \tag{1}$$

Fig. 5 gives the range of possible defect sizes for each number $n$ of connected lines. It can be seen, that there is an overlap between the different intervals, because dependent on the position of a defect within the lines the defect can belong to one of the two possible adjacent intervals. So, for instance in Fig. 5 the defects "$C$" and "$D$" can short either 3 or 4 lines although they have the same size. We have to summarize these overlapping intervals to get a size distribution. For that, it is useful to define the following size-intervals $SI(x)$ where $x \in N_0$ and $x \geq 0$:

$$SI(x) := [s + x \cdot p, \ s + (x + 1) \cdot p]. \tag{2}$$

The frequency $d(n)$ of all detected defects that connect exactly $n$ lines (ref. left side of Fig. 6) has to be distributed among two size intervals. For that, $\alpha(n)$ defects have to be transferred to the size interval $SI(x)$ representing the smaller feature sizes and $\beta(n)$ defects have to be transferred to the size interval $SI(x + 1)$ representing the larger feature sizes, where:

$$\alpha(n) + \beta(n) = d(n). \tag{3}$$

So, for $x = n - 2$ the number $D(x)$ of defects inside each size-interval $SI(x)$ will be:

$$D(x) = \begin{cases} \alpha(2), & \text{if } x = 0 \\ \alpha(x + 2) + \beta(x + 1), & \text{if } x > 0. \end{cases} \tag{4}$$

All these defect frequencies $D(x)$ result in a size distribution illustrated on the right side of Fig. 6, where the fraction of $\alpha$ and $\beta$ can be seen again.

Within the test chips, differently sized defects result in different numbers of connected lines. So, the occurrence of defects dependent on the number of connected lines always implicitly contains the defect size distribution which occurs within the measured test chips. So, we will use the ratio of adjacent defect occurrence value—as shown in charts like Fig. 3—to individually calculate the ratio of $\alpha(n)/\beta(n)$ per size interval. Using a design dependent weight factor $\gamma$, which will be described in detail in Section IV, $\alpha(n)$ will be calculated as

$$\alpha(n) = \begin{cases} 0, & \text{if } d(n) + d(n + 1) = 0 \\ \dfrac{d(n)^2}{d(n) + \gamma \cdot d(n + 1)}, & \text{if } d(n) + d(n + 1) > 0 \end{cases} \tag{5}$$

and $\beta(n)$ will be calculated as

$$\beta(n) = d(n) - \alpha(n). \tag{6}$$

*3) Algorithm for External Lines:*  If external lines are involved, the possible range of defect sizes is much larger than for the internal lines. So, for instance in Fig. 7 the defects "$A$" and "$B$" can just short either 2 or 3 lines although they have the same size than the defects "$C$" and "$D$" of Fig. 5 that have connected 3 or 4 lines. In other words, a two line short circuit can be caused by a defect which size is in-between $s$ and $s + 4p$.

In general, a defect connecting $n \geq 2$ lines may have a size in-between $[s + (n - 2) \cdot p, \ s + 2 \cdot n \cdot p]$. This interval is getting larger the more lines are involved compared to the constant internal range for the internal line algorithm. For that, all defects connecting n lines have to be distributed not just between two defect size intervals but between an
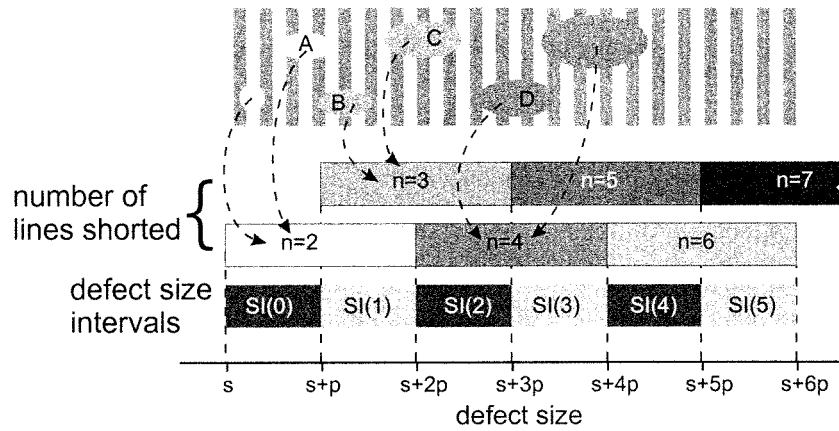
Fig. 5. Link between the size intervals $SI(X)$ and the possible size of a defect causing a short circuit over $n$ lines.
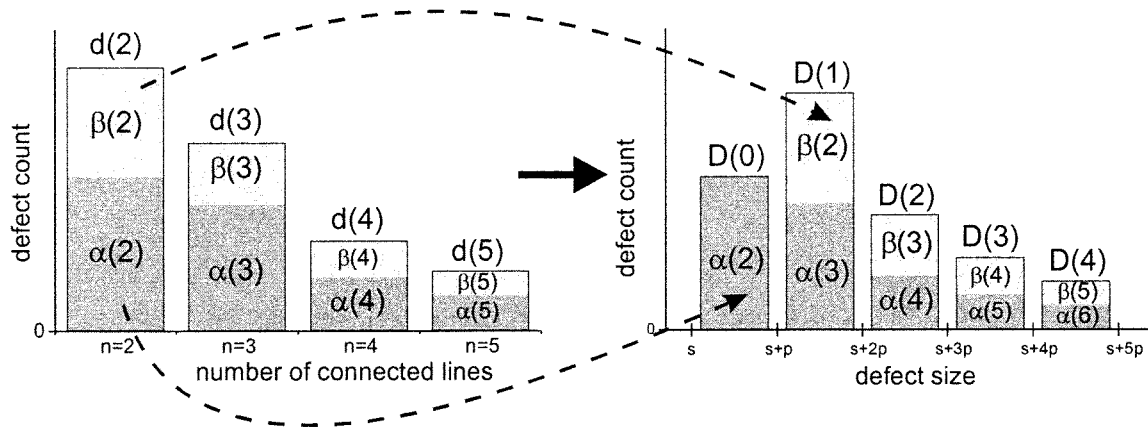


Fig. 6. Transition from the number of defects dependent on the number of involved lines to the defect size distribution.
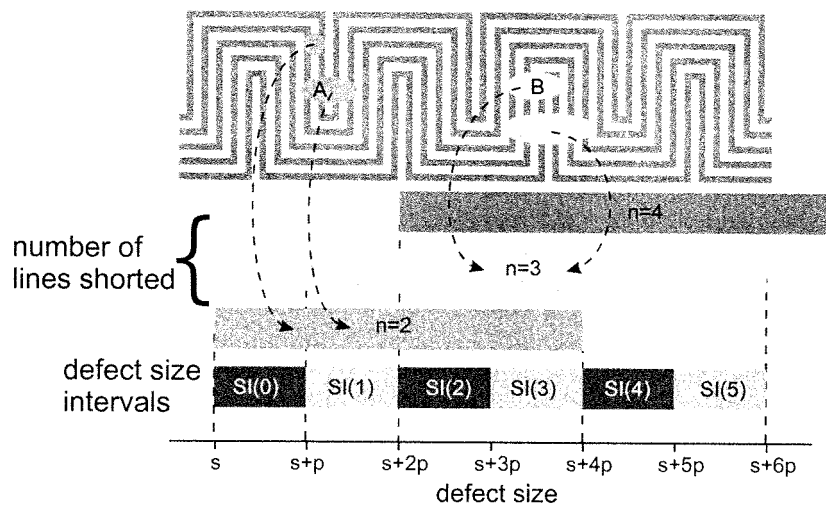


Fig. 7. Link between the size intervals $SI(X)$ and the possible size of a defect causing a short circuit over $n$ internal and external lines.

increasing number of defect size intervals. Furthermore, we usually observe much more faults just connecting internal lines because there are much more internal lines than external lines designed within a NEST structure. So, the sample size

of defects involving external lines is too small to give a reasonable defect size distribution on its own.

Instead, we will use the size distribution already determined for such defects just connecting internal lines to distribute the

defects that connect also external lines among the different defect size intervals. So, based on the number $d_{\text{ext}}(n)$ of faults that have shorted n lines, the following equation will determine the number $D_{\text{ext}}(x)$ of defects per size interval $SI(x)$

$$D_{\text{ext}}(x) := $$

$$\begin{cases} D_{\text{int}}(x) \cdot \sum_{i=2}^{i=x+2} \dfrac{d_{\text{ext}}(i)}{\sum_{k=i-2}^{k=2\cdot i-1} D_{\text{int}}(k)}, & \text{if } x < 2 \\[2em] D_{\text{int}}(x) \cdot \sum_{i=\text{integer}(x/2)+1}^{i=x+2} \dfrac{d_{\text{ext}}(i)}{\sum_{k=i-2}^{k=2\cdot i-1} D_{\text{int}}(k)}, & \text{if } x \geq 2 \end{cases}$$

$$(7)$$

where $D_{\text{int}}$ is the number of defects per size interval $SI(x)$ of the defect size distribution determined in Section III-B2 for the defects involving internal lines only.

*4) Total Defect Size Distribution:* Finally, per size interval we summarize the two defect count values $D_{\text{int}}(x)$ of the internal and $D_{\text{ext}}(x)$ external defect size distribution charts. The resulting histogram will give a size distribution of all defects that have caused electrically measurable faults within NEST structures.

The ratio of faults including an external line versus faults just including internal lines should be about $2 : (m - 2)$, where $m$ is the number of electrically distinguishable lines within a NEST structure. This may be used as a sanity check regarding possible systematic process problems.

## C. Defect Size Extraction for Opens

The same procedure described for short circuits can be used to extract a size distribution of defects that have caused electrically measurable open circuits. To do so, the following transformations have to be applied to the algorithms described in Sections III-B2 and III-B3:

1) The smallest number $n$ of open lines start at $n = 1$ compared to $n = 2$ in case of short circuits. So, due to $x = n - 1$ equation (4) will change to:

$$D(x) = \begin{cases} \alpha(1,) & \text{if } x = 0 \\ \alpha(x+1) + \beta(x), & \text{if } x > 0. \end{cases} \quad (8)$$

2) The width $w$ and space $s$ of the lines within the NEST structure have to be exchanged regarding the defect size intervals. So, a defect opening $n \geq 1$ internal lines may have a size in-between $[w + (n-1) \cdot p, \, w + (n+1) \cdot p]$. Consequently, the size-intervals $SI(x)$ will be defined as:

$$SI(x) := [w + x \cdot p, \, w + (x+1) \cdot p]. \quad (9)$$

3) Defects that open $n \geq 1$ internal and external lines may have a size inbetween $[w + (n - 1) \cdot p, \, w + (2 \cdot n + 1) \cdot p]$. Based on this, the following equation will replace equation (7) to determine the number $D_{\text{ext}}(x)$ of defects
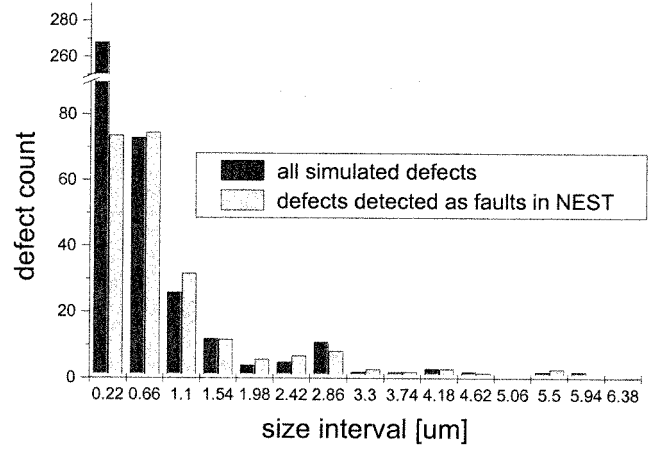


Fig. 8. Comparison of the size distribution of 412 simulated defects and the size distribution of those defects that where detected as faults within a NEST structure.

per size interval $SI(x)$

$$D_{\text{ext}}(x) := $$

$$\begin{cases} D_{\text{int}}(0) \cdot \dfrac{d_{\text{ext}}(1)}{\sum_{k=0}^{k=2} D_{\text{int}}(k)}, & \text{if } x = 0 \\[2em] D_{\text{int}}(x) \cdot \sum_{i=\text{integer}(x+1)/2}^{i=x+1} \dfrac{d_{\text{ext}}(i)}{\sum_{k=i-1}^{k=2\cdot i} D_{\text{int}}(k)}, & \text{if } x > 0. \end{cases}$$

$$(10)$$

## IV. SIMULATION OF DEFECT SIZE DISTRIBUTIONS

To determine the factor $\gamma$ we set up various Monte Carlo simulations for different sets of defects. Per experiment we generated 500 defects on average and throw them on NEST structures having different dimensions. Based on the number of shorted lines we used the algorithms described in Section III to determine a defect size distribution. We then compared such a NEST based defect size distribution to the defect size distribution based on the actual defects that were thrown on the NEST structures. One example for a defect distribution proportional to $1/x^2$ can be seen in the Fig. 8. Another example for a defect distribution proportional to $1/x^3$ can be seen in Fig. 9.

Except for the smallest size interval, we obtained the best fits for $\gamma = 2$ regardless of the defect size distributions we choose and the dimensions we choose for the NEST structures. For the smallest size interval we always observe a much smaller number of defects within the NEST structure than there is according to the assumed defect size distribution, because not all defects that are smaller than the line width plus twice the line space of a NEST structure will actually result in electrically measurable short circuits. To evaluate whether such an error has a significant effect on yield prediction we studied the yield impact on product chips. For that, we determined the cumulative critical area for several typical product chips as one can be seen in Fig. 10. The different curves in this graph show the different cumulative critical area curves for 2 line shorts, 3-line shorts, 4-line shorts,
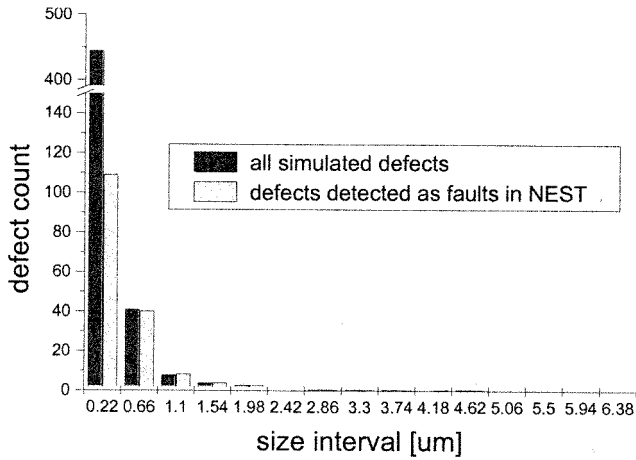
Fig. 9. Comparison of the size distribution of 505 simulated defects and the size distribution of those defects that where detected as faults within a NEST structure.
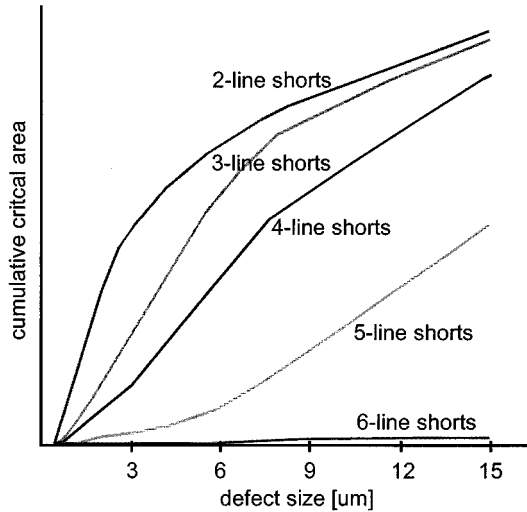


Fig. 10. Cumulative critical area curves of a typical product chip for 2-line shorts, 3-line shorts, 4-line shorts, 5-line shorts, and 6-line shorts.

5-line shorts, and 6-line shorts. Only the 2-line shorts and the 3-line shorts have some critical areas in the small size region we are interested in. The yield impact is proportional to the integral of the critical area multiplied by the defect size distribution as can be seen in Fig. 11 for different defect size distributions. It can be seen that the yield impact for the smallest defect size interval is less than 5%. So, even a relatively large error in this region is acceptable if it comes to yield prediction.

## V. EXPERIMENTAL RESULTS

At Toshiba Corporation in Yokohama, Japan, several NEST structures were manufactured to control defect appearance in a deep submicron backend environment. Table I summarizes the structures used to extract defect size distributions. Using differently dimensioned NEST structures enables the separation of systematic and random defects. So, for instance there will be no systematic yield issues only if the defect density values of differently dimensioned NEST structures follow a poisson distribution. If defects occur and cause a fault, either test structure
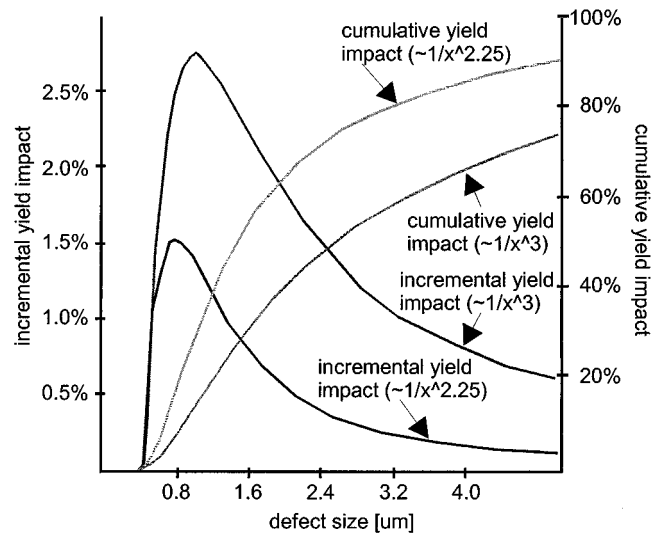


Fig. 11. Yield impact of different simulated defect size distributions on a product chip.

TABLE I
DIMENSIONS OF NEST STRUCTURES TO EVALUATE DEEP SUBMICROMETER INTERCONNECTION LAYER

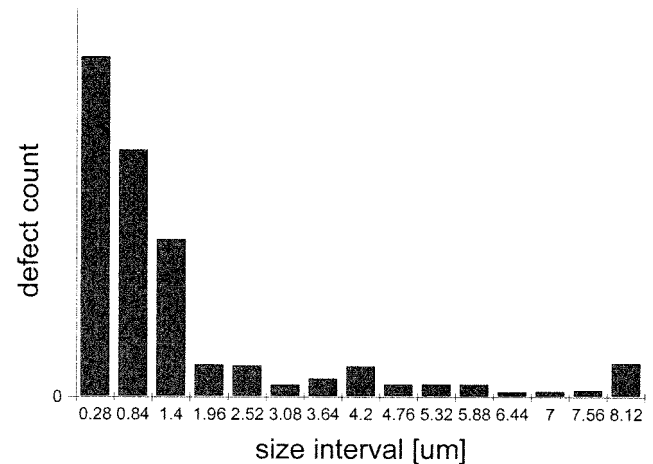| line pitch [um] | number of parallel lines per structure | area per structure [mm2] | pads per structure |
|---|---|---|---|
| 0.4 | 4992 | 2.4 | 2 by 16 |
| 0.44 | 4544 | 2.4 | 2 by 16 |
| 0.48 | 4160 | 2.4 | 2 by 16 |
| 0.56 | 3552 | 2.4 | 2 by 16 |
| 0.64 | 3104 | 2.4 | 2 by 16 |



Fig. 12. Size distribution of defects detected within a 0.56-$\mu$m line pitch (0.28-$\mu$m line width) NEST structure.

lines are connected to each other or test structure lines are interrupted. Since we know which test structure lines are implemented as neighbors, we can conclude to the number and size of the defects. Based on the number of shorted lines we apply the algorithms introduced in Section III to determine a defect size distribution as can be seen in Figs. 12 and 13. If for yield prediction purposes these measured defect size distributions should be modeled by an analytical function or calibrated to an analytical
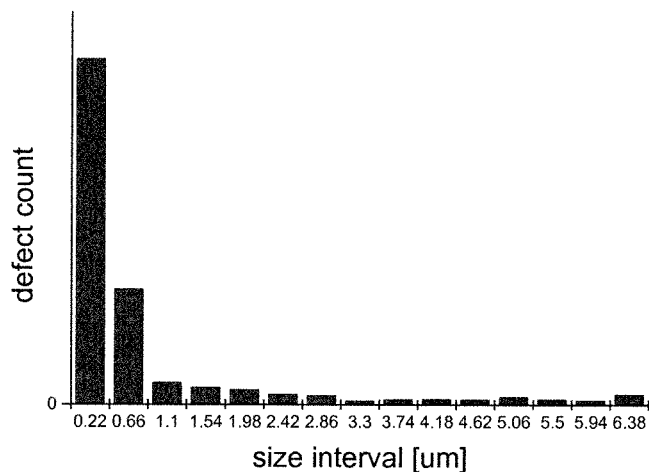
Fig. 13. Size distribution of defects detected within a 0.44-$\mu$m line pitch (0.22 -$\mu$m line width) NEST structure.
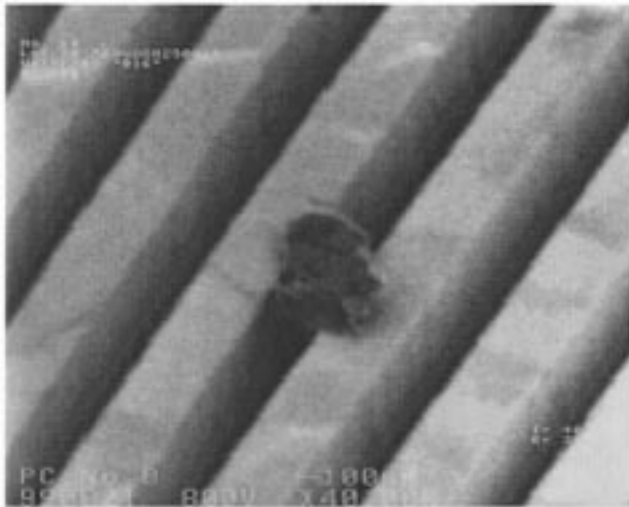


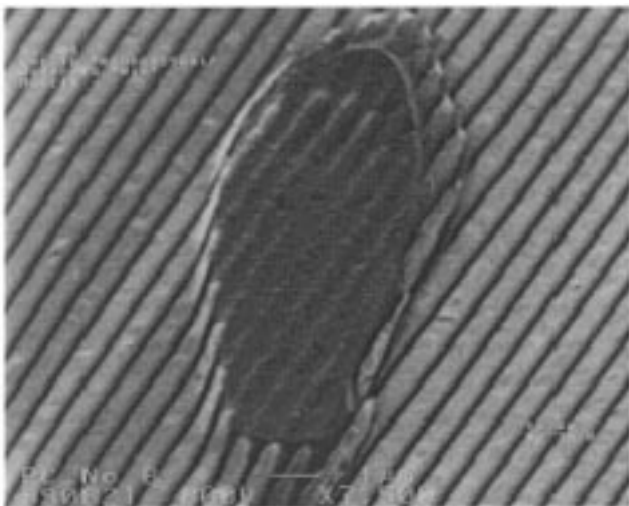Fig. 14. Detected defect that has caused an electrically measurable short circuit between 2 lines.



Fig. 15. Detected defect that has caused an electrically measurable short circuit between 11 lines.

function, it is possible to use the method describe at [4] since the NEST structure is fully compatible with the measurement and analysis requirements discussed in that paper. SEM pictures of two detected defects can be seen in Figs. 14 and 15. The same principle could be applied for opens, but the observed defect density was too small to actually generate a significant defect size histogram.

## VI. CONCLUSION

The described method to place test structure lines enables a fast and efficient inspection of defects that occur in a single layer. Just using a single short loop mask guarantees a short turn around time for fast process controlling. There is no limitation regarding layer specific properties such as sheet resistance and no requirement of any semiconductor devices to separate test structure lines or disentangle multiple faults, respectively. The NEST structure detects systematic problems as well as random defects to determine accurate defect densities and size distributions.

## ACKNOWLEDGMENT

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[5] C. H. Staper and R. J. Rosner, "Integrated circuit yield management and yield analysis: Development and implementation," *IEEE Trans. Semiconduct. Manufact.*, vol. 8, pp. 95–102, May 1995.

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