EE290H

Special Issues in Semiconductor Manufacturing

Costas J. Spanos
Department of Electrical Engineering
and Computer Sciences
el (510) 643 6776, fax (510) 642 2739
email spanos@eecs.berkeley.edu

Kameshwar Poolla
Department of Mechanical Engineering
el (510) 642 4642, fax (510) 643 5599
email poolla@me.berkeley.edu
University of California Berkeley, CA 94720, U.S.A.

http://www-inst.eecs.berkeley.edu/~ee290h/

Fall 2003

The purpose of this class

To integrate views, tools, data and methods towards a coherent view of the problem of *Efficient* Semiconductor Manufacturing.

The emphasis is on technical/engineering issues related to current state-of-the-art as well as future technology generations.

The Evolution of Manufacturing Science

1. Invention of machine tools. English system (1800).
   mechanical - accuracy
2. Interchangeable components. American system (1850).
   manufacturing - repeatability
3. Scientific management. Taylor system (1900).
   industrial - reproducibility
4. Statistical Process Control (1930).
   quality - stability
5. Information Processing and Numerical Control (1970).
   system - adaptability
6. Intelligent Systems and CIM (1980).
   knowledge – versatility
7. Physical and logical ("lights out") Automation (2000).
   integration – efficiency

Fall 2003 EE290H Tentative Weekly Schedule

1. Functional Yield of ICs and DFM. **2. Parametric Yield of ICs.** **3. Yield Learning and Equipment Utilization.**	IC Yield & Performance
4. Statistical Estimation and Hypothesis Testing. **5. Analysis of Variance.** **6. Two-level factorials and Fractional factorial Experiments.**	Process Modeling
7. System Identification. **8. Parameter Estimation.** **9. Statistical Process Control.** ***Distribution of projects. (week 9)*** **10. Run-to-run control.** **11. Real-time control.** ***Quiz on Yield, Modeling and Control (week 12)***	Process Control
12. Off-line metrology - CD-SEM, Ellipsometry, Scatterometry **13. In-situ metrology - temperature, reflectometry, spectroscopy**	Metrology
14. The Computer-Integrated Manufacturing Infrastructure	Manufacturing Enterprise

15. ***Presentations of project results.***

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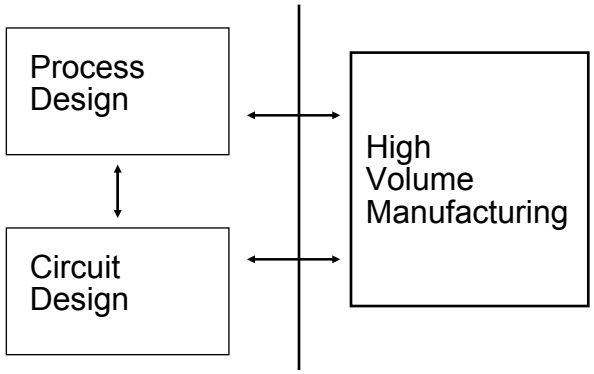
- Class Site http://www-inst.eecs.berkeley.edu/~ee290h/
- International Technology Road Map for Semiconductors, 2002 update http://public.itrs.net/
- Atlas of IC Technologies - An Introduction to VLSI Processes, W. Maly, The Benjamin/Cummins Publishing Company, Inc, 1987
- Semiconductor Manufacturing (Draft MS) by Gary May and Costas Spanos.

IC Yield and Performance

- Defect Limited Yield
  - Definition and Importance
  - Metrology
  - Modeling and Simulation
  - Design Rules and Redundancy
- Parametric Yield
  - Parametric Variance and Profit
  - Metrology and Test Patterns
  - Modeling and Simulation
  - Worst Case Files and DFM
- Equipment Utilization
  - Definition and NTRS Goals
  - Measurement and Modeling
  - Industrial Data
- General Yield Issues
  - Yield Learning
  - Short loop methods and the promise of in-situ metrology

What Determines IC Production Efficiency?



Solid interaction channels are needed between design and manufacturing.

Issues

- Understand and model random phenomena.
- Functional and parametric yield important, but only part of the picture.
- Production optimization belongs to three "spheres of influence":

  Process Engineer

  Process Designer

  IC Designer

- The interaction among the three spheres of influence is very important.

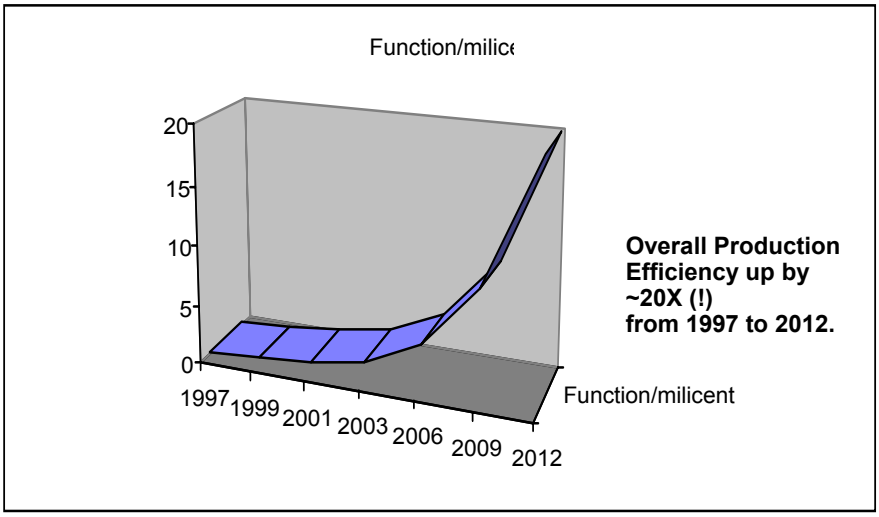
The 2002 Roadmap

Table 57a Lithography Technology Requirements—Near-term

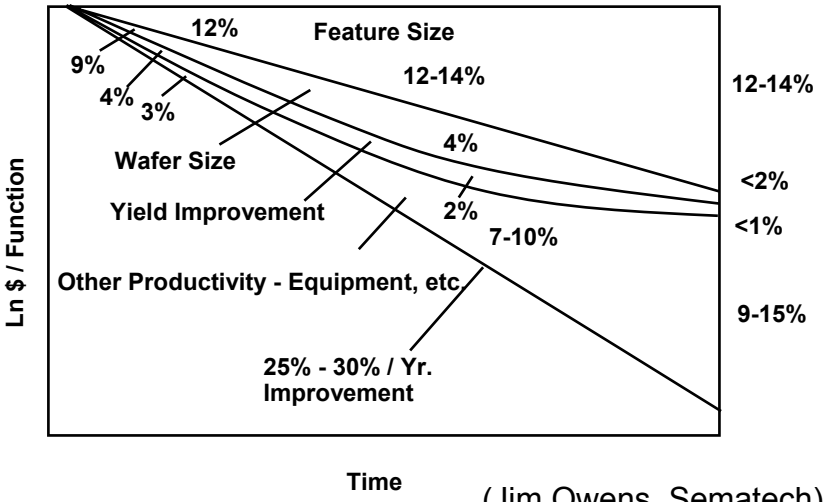
Year of Production	2001	2002	2003	2004	2005	2006	2007
DRAM							
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
Contact in resist (nm)	165	140	130	110	100	90	80
Contact after etch (nm)	150	130	115	100	90	80	70
Overlay	46	40	35	32	28	25	23
CD control (3 sigma) (nm)	15.9	14.1	12.2	11	9.8	8.6	8
MPU							
MPU ½ Pitch (nm)	150	130	107	90	80	70	65
MPU gate in resist (nm)	90	70	65	53	45	40	35
MPU gate length after etch (nm)	65	53	45	37	32	28	25
Contact in resist (nm)	165	140	122	100	90	80	75
Contact after etch (nm)	150	130	107	90	80	70	65
Gate CD control (3 sigma) (nm)	5.3	4.3	3.7	3	2.6	2.4	2
ASIC/LP							
ASIC/LP ½ Pitch (nm)	150	130	107	90	80	70	65
ASIC/LP gate in resist (nm)	130	107	90	75	65	53	45
ASIC/LP gate length after etch (nm)	90	80	65	53	45	37	32
Contact in resist (nm)	165	140	122	100	90	80	75
Contact after etch (nm)	150	130	107	90	80	70	65
CD control (3 sigma) (nm)	7.3	6.5	5.3	4.3	3.7	3	2.6
Chip size (mm^2)							
DRAM, introduction	390	308	364	287	454	359	568
DRAM, production	127	100	118	93	147	116	183
MPU, high volume at introduction	280	280	280	280	280	280	280
MPU, high volume at production	140	140	140	140	140	140	140
MPU, high performance	310	310	310	310	310	310	310
ASIC	800	800	572	572	572	572	572
Minimum field area	800	800	572	572	572	572	572
Wafer size (diameter, mm)	300	300	300	300	300	300	300

–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

The main metric is “Efficiency”



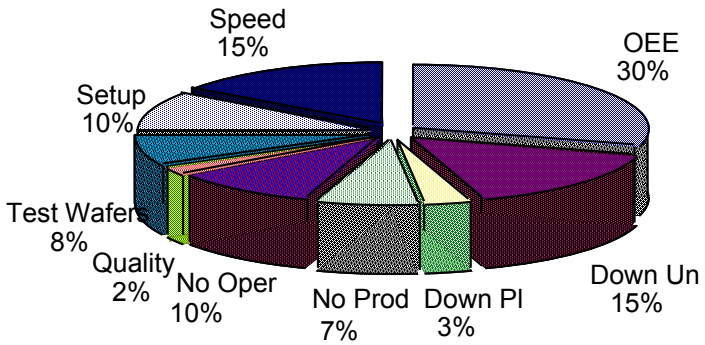
Where will the Extra Productivity Come from?



(Jim Owens, Sematech)

The Opportunities

Year	1997	1999	2001	2003	2006
Feature nm	250	180	150	100	70
Yield %	85	~90	~92	~93	?
Equipment utilization %	35	~50	~60	~70	
Test wafers %	5-15	5-15	5-15	5-15	



Yield Definitions

- Yield is simply the percentage of “good” product in a production batch.
- Yield has several components, each requiring a distinct set of tools to understand and improve.
- We will talk about the three main components:
  - Functional (defect driven)
  - Parametric (performance driven)
  - Production efficiency / equipment utilization

The Yield Problem

- Improving Yield quickly used to be a key competitive issue for all IC manufacturers.
- As the cost of installed equipment increases, one wants to amortize this cost over many ICs.
  - Even on 24hour operation, equipment utilization is low.
  - Limited yield is responsible for about 50% of equipment utilization loss.
  - Yield fluctuations cause terrible planning problems.
  - The problem is aggravated by frequent equipment, technology and design changes.
- One can say that Yield is limited by *Variability*

Routine vs. Assignable Variability

- Routine Variability is the result of a process that is under "Statistical Control":, i.e. follows some predetermined statistical distributions.

- Assignable Variability is the result of inadvertent "one of a kind" occurrences.

IC production suffers from routine and assignable variability

- Human errors, equipment failures
  - Processing instabilities
  - Material non-uniformities
  - Substrate non-homogeneities
  - Lithography spots
  - ...
- Planning and scheduling issues that limit equipment utilization

Process Variability Causes Deformations

- Geometrical
  - ° Lateral
  - ° Vertical
  - ° Spot defects
- Electrical
  - ° Global
  - ° Local

Deformations have *deterministic* and *random* components, are *global* and/or *local*, can be *independent* or can *interact*.

Deformations of Ideal Design

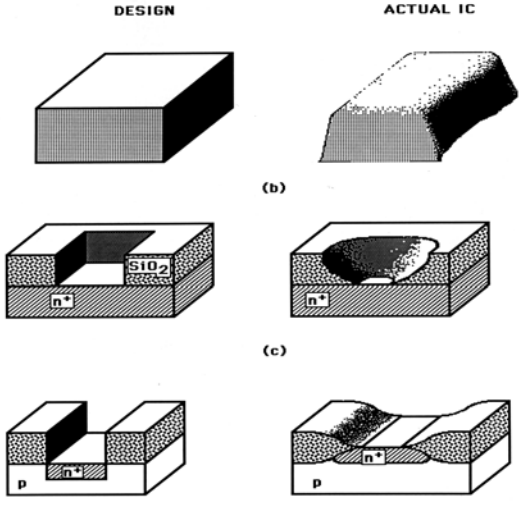
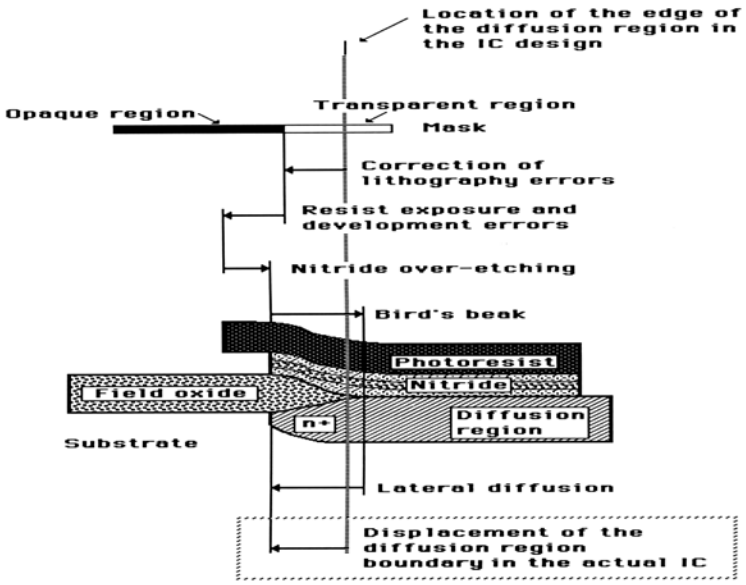


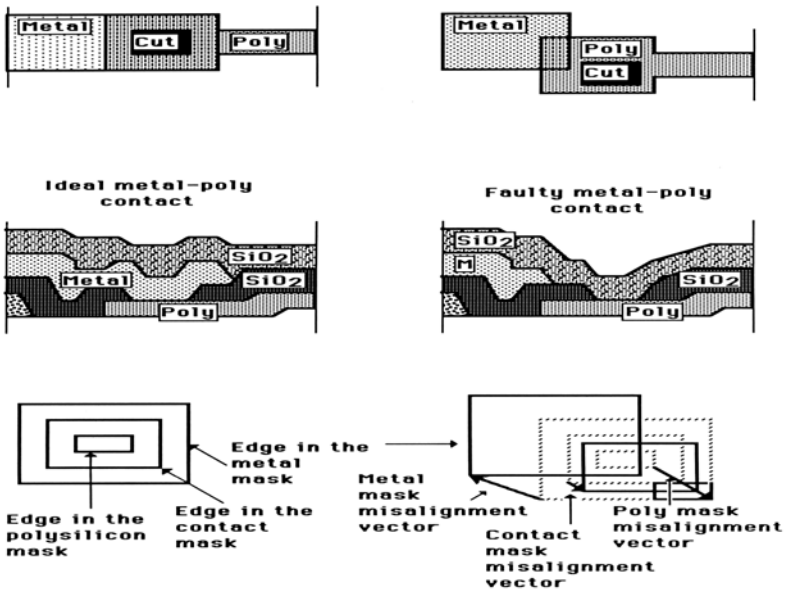
Figure 2-8: Discrepancies between concepts used in the design and actual elements of the IC, showing a metal line (a), contact cut (b), and diffusion region (c).

Atlas of IC Technologies - An Introduction to VLSI Processes, W. Maly, The Benjamin/Cummins Publishing Company, Inc, 1987

Lateral Displacement In Pattern Transfer.



Mask Misalignment



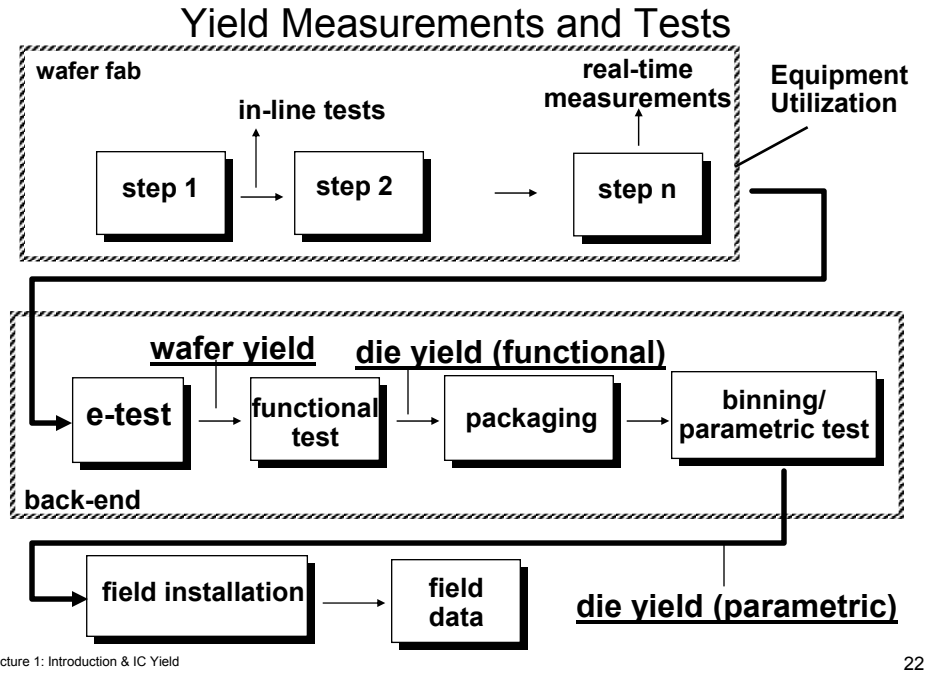
Deformations cause Faults

- Structural faults
- Performance faults
  - ° Soft performance faults
  - ° Hard performance faults

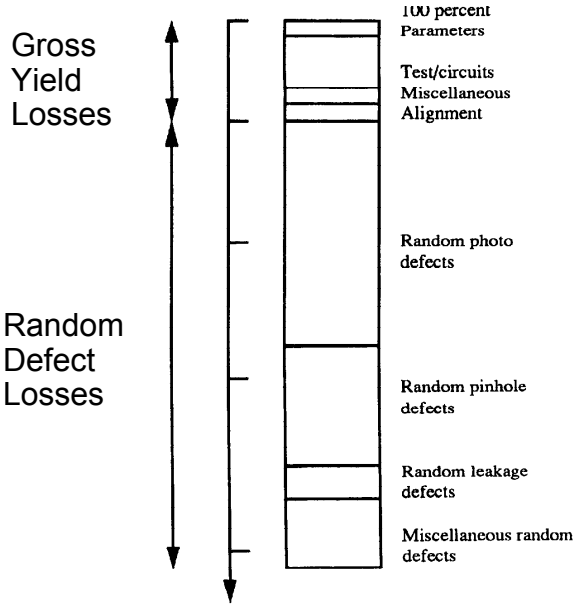
Faults have an impact on *Yield.*

Design Yield	Manufacturing Yield
• Functional • Parametric	• Wafer - Probe Testing - Final Testing • Equipment Utilization

Yield Measurements and Tests



Why do chips fail?



Yield sensitivity of CMOS Gate Array

Yield		Structural Fail.		Performance Failure			
		Geometrical				Electrical	
		Local	Global	Local	Global	Local	Global
Wafer	Manufacturing		Align & registration		Align & registration		Contamination
Probe					Interconnect delays		
Final							
Processing					Align & registration		Element parameter variation
Parametric	Design				Align & registration		Element parameter variation
Functional		Spot Defects					

Yield Sensitivity of Large DRAM

Yield		Structural Fail.		Performance Failure			
		Geometrical				Electrical	
		Local	Global	Local	Global	Local	Global
Wafer	Manufacturing		Wafer Deform		Etching		Contamination
Probe	Manufacturing	Spot Defects			Interconnect delays		
Final	Manufacturing	Spot Defects			Interconnect delays		
Processing	Manufacturing		Align & registration		Align & registration		Element parameter variation
Parametric	Design		Align & registration		Align & registration		Element parameter variation
Functional	Design	Spot Defects					

Yield Sensitivity of Bipolar Op Amp

Yield		Structural Fail.		Performance Failure			
		Geometrical				Electrical	
		Local	Global	Local	Global	Local	Global
Wafer	Manufacturing						DIP Effect
Probe	Manufacturing	Spikes, pipes, etc.		Align & registration		Spikes, pipes, etc.	Bar tr. parameters
Final	Manufacturing						
Processing	Manufacturing	Spikes, pipes, etc		Align & registration		Spikes, pipes, etc	Bar tr. parameters
Parametric	Design						Element parameter variation
Functional	Design	Spikes, pipes, etc		Align & registration		Spikes, pipes, etc	

What limits Functional Yield?

- Gross Misalignments
- Particles
- Mask Defects
- In general, the above are considered random events, and their assumed distribution plays a profound role in decisions having to do with:
  - Metrology (how often and what we measure)
  - Modeling (how one can predict the occurrence of these events)
  - Simulation (calculating how a specific IC layout will do)
  - Design rules/styles to “immunize” the IC to defects

Particles vs. Defects

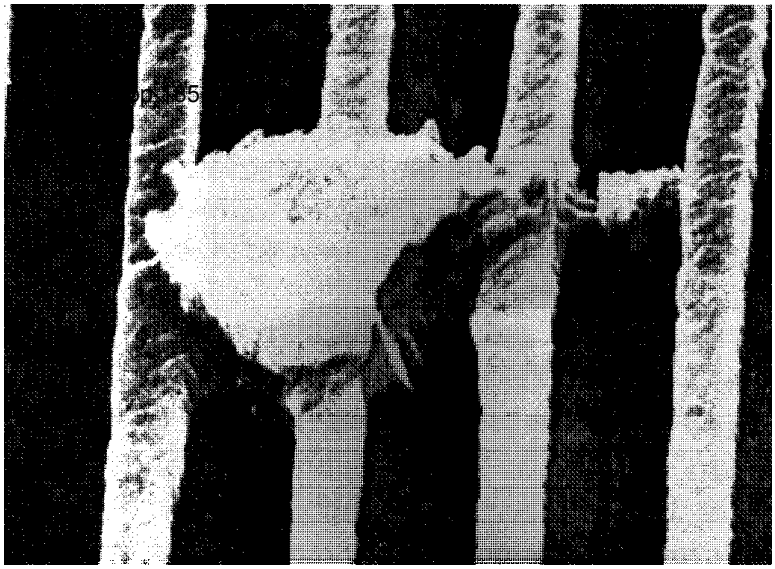
- Particles come from *outside* the device structure
- Defects are created *within* the device structure

  Aluminum spiking

  Interconnect patterning

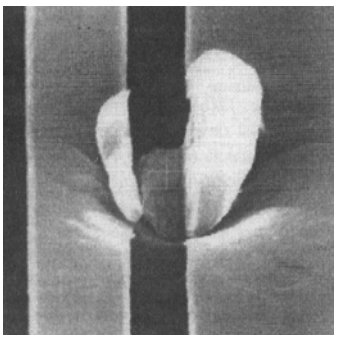
  etc.

Particles



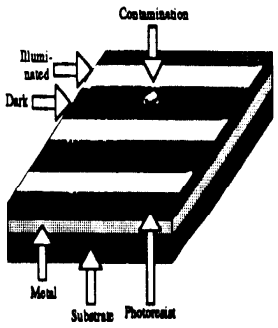
Where do particles come from?

- People
- Material Handling
- Processing chambers

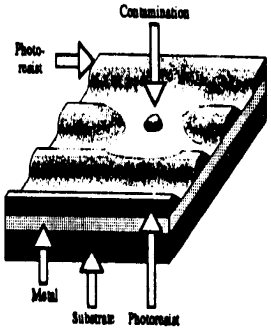


When does a particle matter?

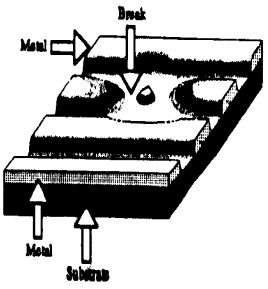
Exposure



Etching



Final Structure



Wafer scanning for particles

- Catastrophic failures are the result of “defects”.
- Not all defects are visible.
- Often, defects are caused by visible particles.
  - A great deal of effort is spent in testing process steps for particle generation.
- Equipment is used to scan patterned or un-patterned (blanket) wafers.
- Today’s sensitivity can be set to detect particles well under half a micron (typically as low as 0.1μm) on patterned wafers.
- Testing is expensive and time consuming.

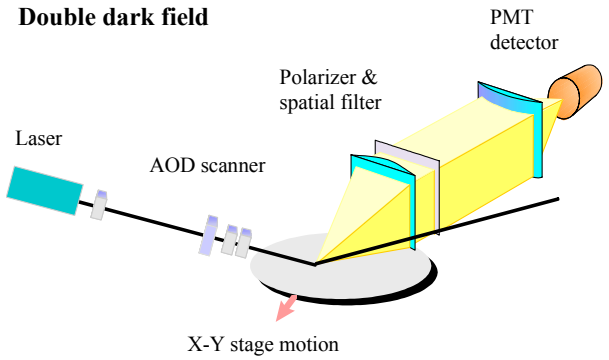
Wafer Inspection Technology Challenges for ULSI Manufacturing, S. Stokowski and M Vaez-Iravani, Characterization and Metrology for ULSI Technology, March 1998

In Line Particle Detection by Wafer Scanning

Inspection systems sell at about 700M/year, and the best can do 40nm detection, at about 150 wafers/hour.

Bright field systems take and analyze images (slow!)

Dark field systems detect scattered light (fast!)

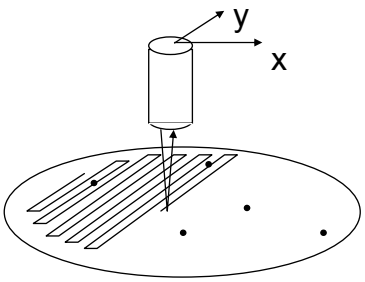


Counting particles

Scanning a “blanket” monitor wafer.

Diffracted light detects position and approximate size of particle.

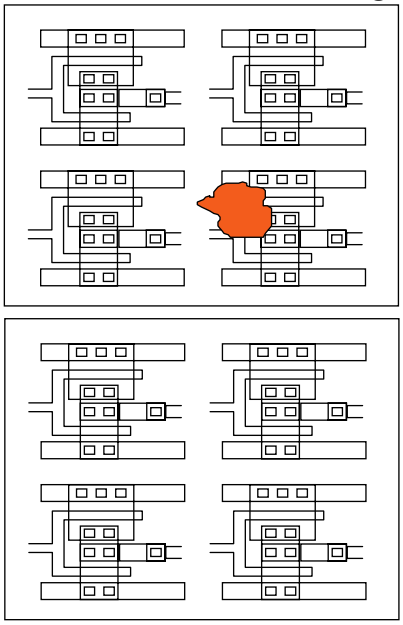
“Wafer Maps” with particle locations are then loaded to Optical or SEM imaging tools for further analysis.

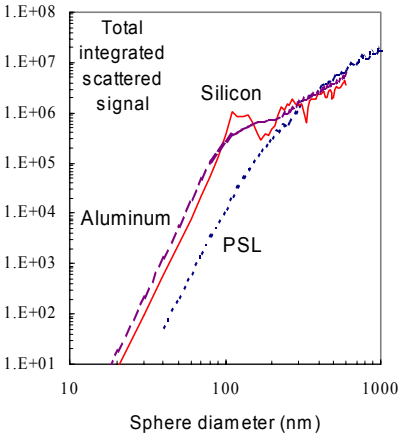


Lithography can print 10^{10} - 10^{11} resolution elements per sec.

The fastest systems can inspect 6×10^{8} pixels per sec.

Scanning a product wafer





Particle size is deduced by scattered intensity.

Imaging is only needed for detailed diagnostics.

The issue of measurement planning

- Typical “suspect” processes include plasma etching, RTP, CVD, PVD, PECVD, etc.
- There are dozens of such steps in a process, so there is great demand for particle scanning.
- State of the art scanners need several minutes per wafer.
  - One has to decide on a rational subset of wafers to scan.

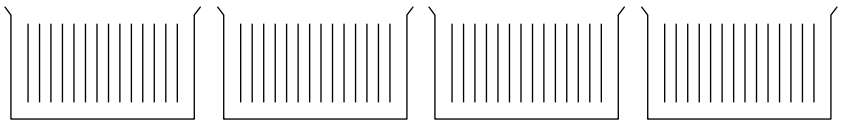
The Resource Allocation Problem

Since wafer scanning is expensive, we must create an “optimum” plan for testing a meaningful allocation.

Plans can be *adaptive*, so that dirty wafers receive more scrutiny.

Acceptance Sampling

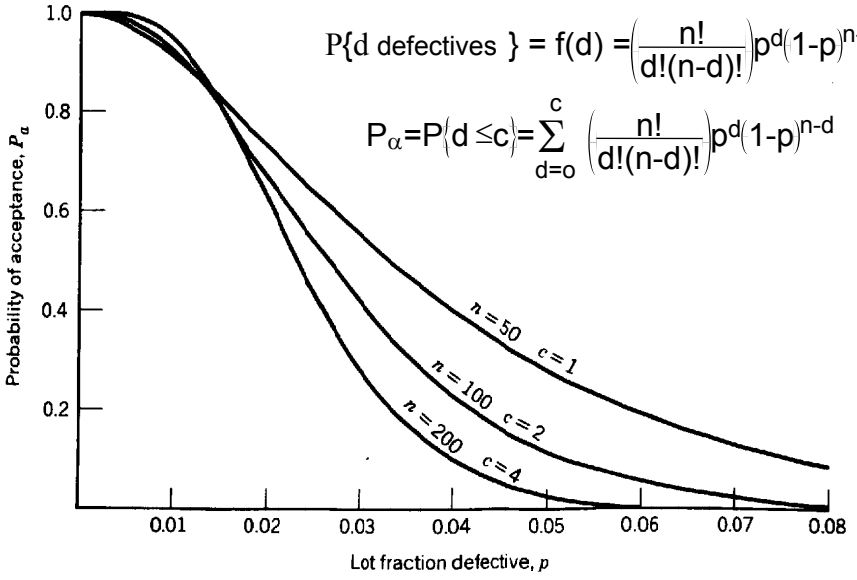
How many wafers do we sample per lot? How many points we measure per wafer?



Acceptance sampling is not a substitute for process control or good DFM practices.

Acceptance sampling is a general collection of methods designed to inspect the finished product.

Definition of a Single-Sampling Plan

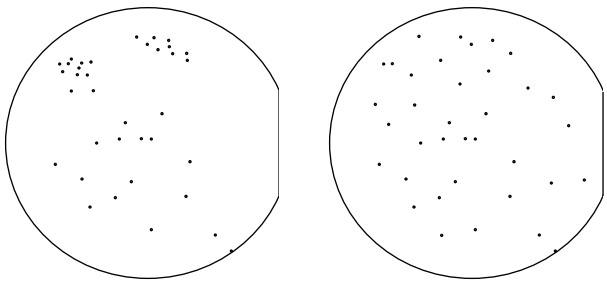


$$P\{\text{d defectives}\} = f(d) = \left(\frac{n!}{d!(n-d)!}\right)p^d(1-p)^{n-d}$$

$$P_\alpha = P(d \le c) = \sum_{d=o}^{c} \left(\frac{n!}{d!(n-d)!}\right)p^d(1-p)^{n-d}$$

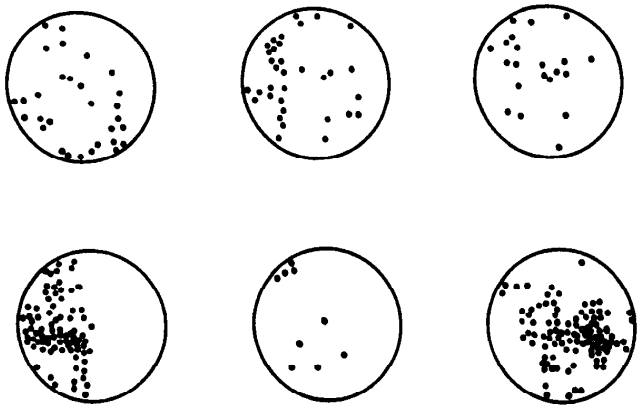
The Problem with Wafer Maps

Wafer maps contain information that is very difficult to enumerate

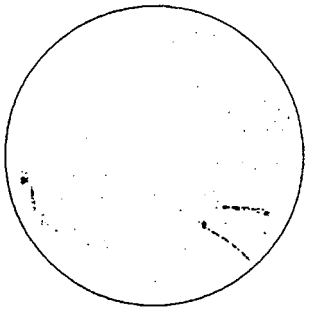


A simple particle count cannot convey what is happening.

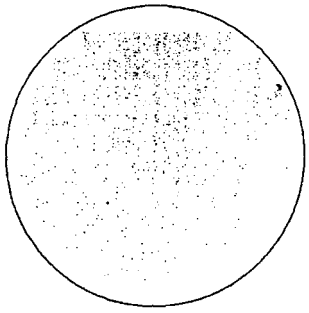
Typical Spatial Distributions



Two (extreme) Clustering Cases



This needs the modified Hough transformation to detect scratches, while ignoring background defects.



This is an example of a diffuse cluster. This is best detected after high density clusters have been removed from data.

The Development and Use of In-line Yield Estimates in Semiconductor Manufacturing, Ph.D. Dissertation, S. P. Cunningham, IEOR, UC Berkeley, 1995

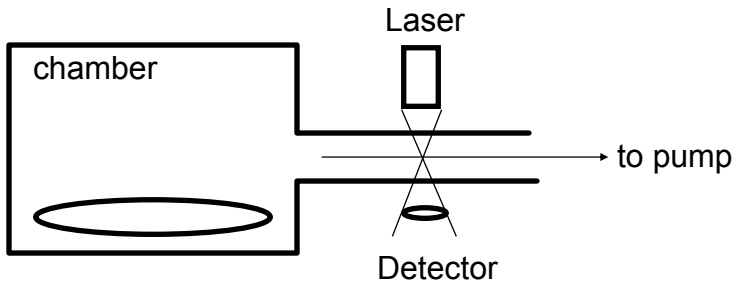
Spatial Wafer Scan Statistics for SPC applications

- Particle Count
- Particle Count by Size (histogram)
- Particle Density
- Particle Density variation by sub area (clustering)
- Cluster Count
- Cluster Classification
- Background Count

Whatever we use (and we might have to use more than one), must follow a known, usable distribution.

In Situ Particle Monitoring Technology

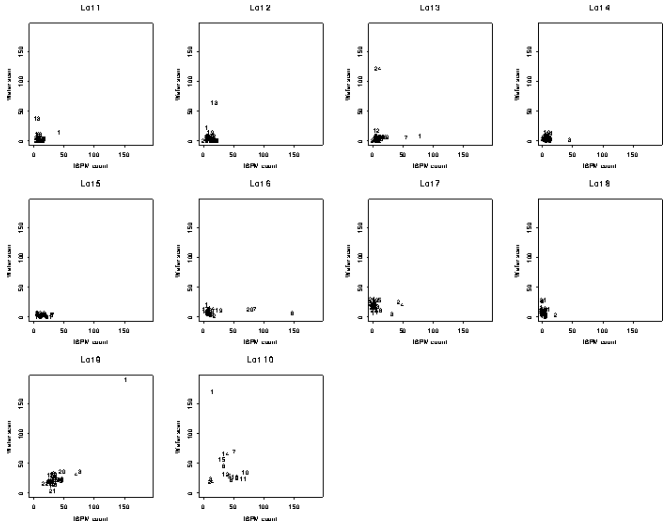
Laser light scattering system for detecting particles in exhaust flow. Sensor placed down stream from valves to prevent corrosion.



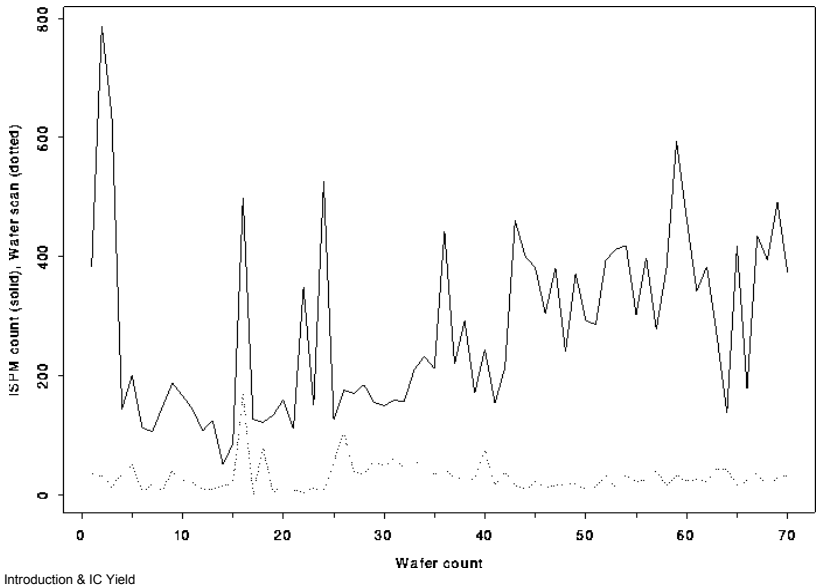
Assumed to measure the particle concentration in vacuum

Progression of scatterplots over time

The end-point detector failed during the ninth lot, and was detected during the tenth lot.



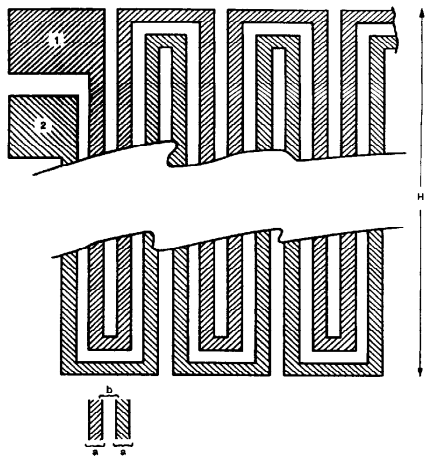
Time series of ISPM counts vs. Wafer Scans



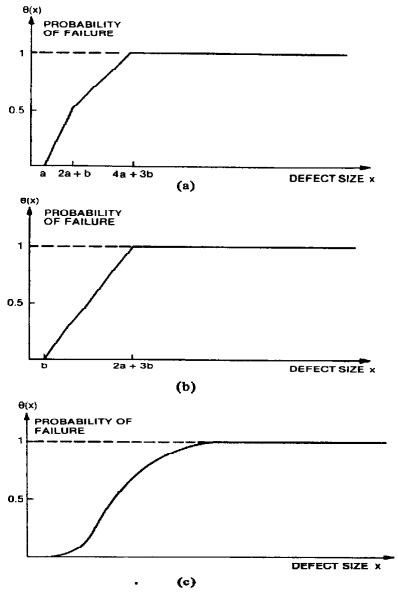
Drawing inferences from electrical test patterns

- Often one resorts to much faster (but less accurate) testing of electrical structures designed for particle detection.
- These can only be used on conductive layers, at the end of a process.
- Can detect shorts, opens in one layer, or shorts between layers.
- One must make assumptions about defect size and density in interpreting these results.

Electrically testable defect structure - Short/Open detection



Probability of Failure



Open
test structure

Short
test structure

Complex,
simulated
design

Electrically testable defect structures - defect size detection

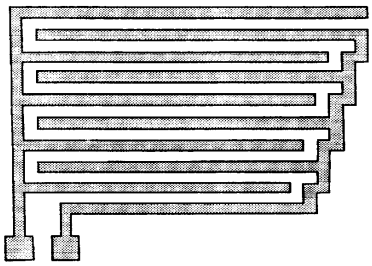
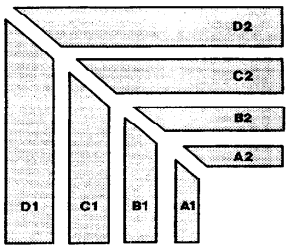


Fig. 1. Test pattern 1. Interdigitated combs.



Test Structure Performance

LINE WIDTHS AND SPACINGS OF TEST PATTERN 1

Line Pairs	A	B	C	D
Line width, w (μm)	0.5	0.7	1.0	1.4
Line spacing, s (μm)	0.5	0.7	1.0	1.4
Number of parallel lines, N	261	261	252	246
Average line length, L (μm)	880	1243	1726	2371
Area occupied by one half pair (10^{-3} cm^2)	2.29	4.53	8.68	16.30

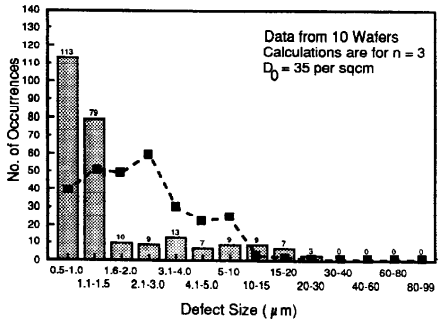


Fig. 6. Size distribution of defects that caused electrical shorts in parallel line pattern 1. Histogram shows microscopic observations. Black squares are calculated from model for defect-induced shorts.

Other Types of defect structures

Contact chains

Fallon Ladders

Charging structures

etc.

Use of in-line yield metrology

- Wafer screening
- Machine maintenance
- Yield learning
- Modeling (next time!)
- Design fault tolerant circuits

Functional Yield Modeling

Early Yield Models

Murhpy's

Modified Poisson

Negative Binomial

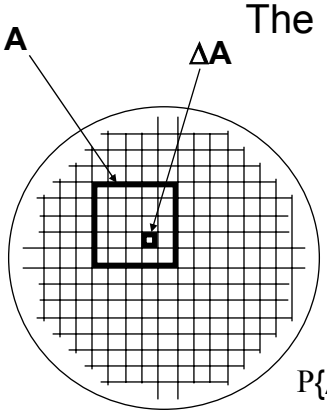
Component Models

Early Yield Models

$Y = \left(1 - \frac{S}{100}\right)^N$ Used for discrete components by Wallmark, 1960.
(S is failures in batch of 100)

$Y = e^{-NA_G D}$ Introduced by Hofstein and Heiman in 1963. Depends on gate area A_G.

The Basic Yield Model



Assume a constant defect density **D**

Assume that it takes one defect to kill a circuit.

Find the probability that a circuit will work, given **D** and the area **A** of a circuit.

$$P\{\Delta A \text{ is "bad"}\} = D\Delta A$$

$$A = n\Delta A$$

$$Y = P\{A \text{ is "good"}\} = \prod_{1}^{n} (1 - D\Delta A) = (1 - D\Delta A)^n$$

$$\ln(Y) = \frac{A}{\Delta A}\ln(1 - D\Delta A) \rightarrow - D A \text{ when } \Delta A \rightarrow 0$$

$$Y = e^{- D A}$$

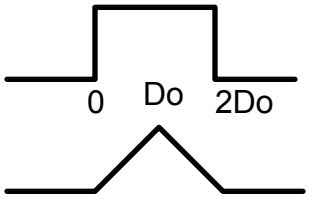
Poisson and Murphy's Yield Models

$$Y = \int_0^{\infty} e^{-AD} f(D)\,dD$$

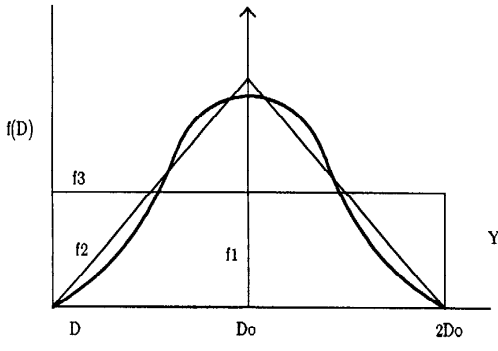
$$Y = \frac{1-e^{-2AD_o}}{2D_oA}$$

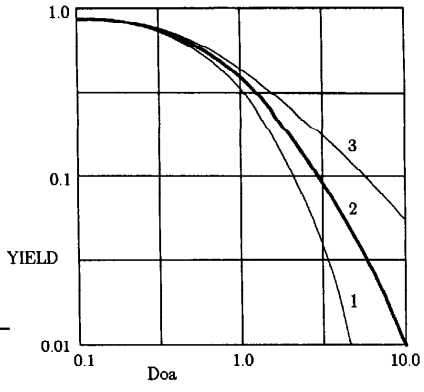
$$Y = \left(\frac{1-e^{-AD_o}}{D_oA}\right)$$

Murphy 1964



Poisson and Murphy's Yield Models (cont)





Modified Poisson Model

$$Y_{est}(A) = e^{-\lambda(A)} = e^{-\lambda(A_o)(A/A_o)}$$ From basic yield model.

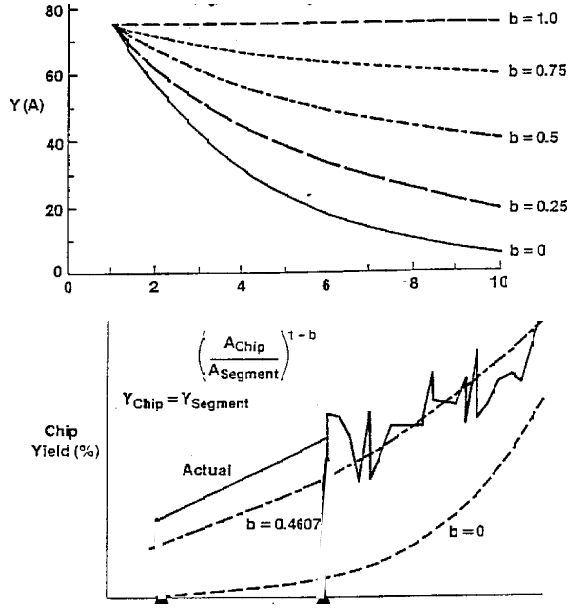
But basic yield model is too pessimistic, mainly because of defect clustering. So, the basic model can be modified:

$$Y_{est}(A) = e^{-\lambda(A_o)(A/A_o)^{1-b}} = Y_{meas}(A_o)^{(A/A_o)^{1-b}}$$

$$D_{est}(A) = D_{inf}(A_o)(A/A_o)^{1-b}$$

$$D_{inf}(A_o) = -[\ln Y_{meas}(A_o)]/A_o$$

Fitting the Modified Poisson Model



Negative Binomial

If f(D) follows a Gamma distribution, then:

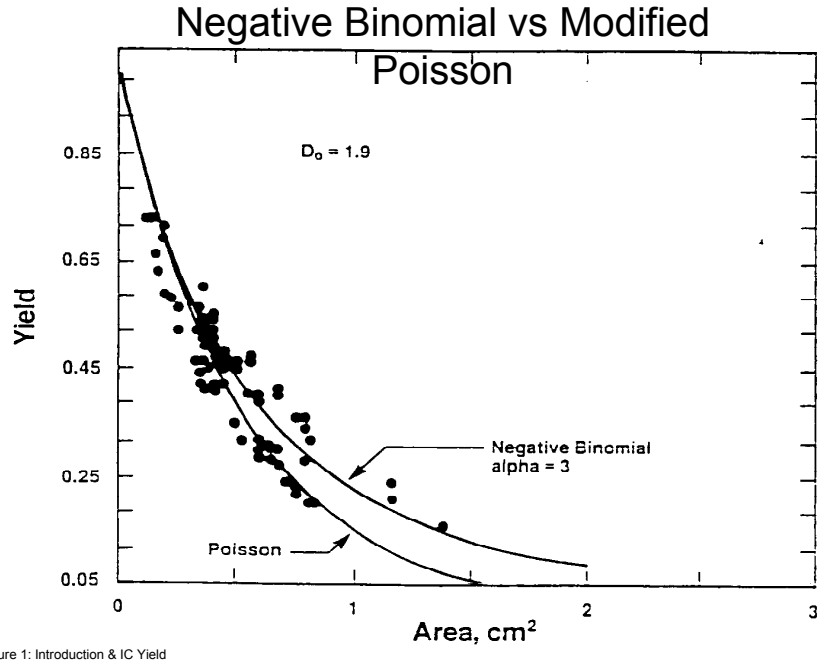
$$Y = \left[1 + \frac{A D}{\alpha} \right]^{-\alpha} \qquad (\alpha \sim 0.3 - 3)$$

And if clustering becomes an issue, then:

$$Y = Y_o \left[1 + \frac{A D}{\alpha} \right]^{-\alpha}$$

where Y_o is the "gross cluster yield".

Negative Binomial vs Modified Poisson



Component Yield Models

It is understood that as ICs are being processed in steps, yield losses also occur at *each layer*.

One can further assume that defect types are independent of each other.

$$Y = \prod_{i=1}^{M} \left[1 + \frac{A_i D_i}{\alpha_i} \right]^{-\alpha_i}$$

Or, to simplify model fitting, an approximation is made:

$$Y = \left\{ 1 + \frac{\left(\sum_{i=1}^{M} A_i D_i \right)}{\alpha_t} \right\}^{-\alpha_t}$$

Fitting Yield Models by Layer

Each layer (or defect type) is measured by a defect monitor made for that layer.

$$Y_{pi} = Y_{oi} \left\{ 1 + \frac{A_{pi}}{A_{mi}} \left[\alpha_i \left(\frac{Y_{oi}}{Y_{mi}} \right)^{1/2} - 1 \right] \right\}^{-\alpha_i}$$

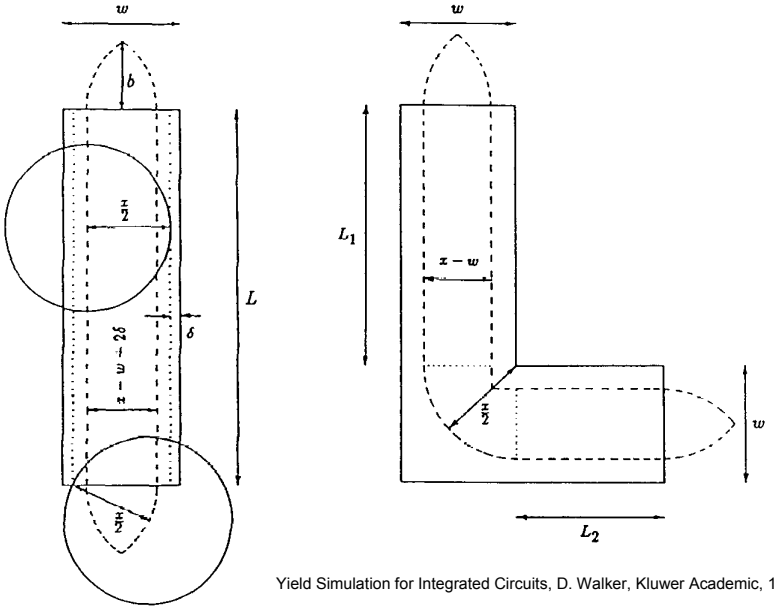
gross cluster — product — monitor

What is the “critical area”?

Yield simulation based on Critical Area

- Yield “Modeling” refers to aggregate models for a given technology and design rules (λ).
- The objective of yield “Simulation” is to predict the functional yield of a given, specific layout fabricated in a known line.
  - Need to know defect size and spatial distributions.
  - Must take into account the specific masks, one layer at a time.

The Concept of the Critical Area

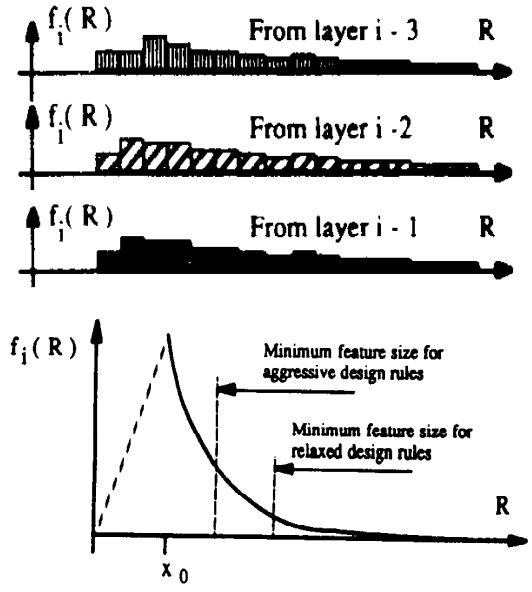


Yield Simulation for Integrated Circuits, D. Walker, Kluwer Academic, 1987

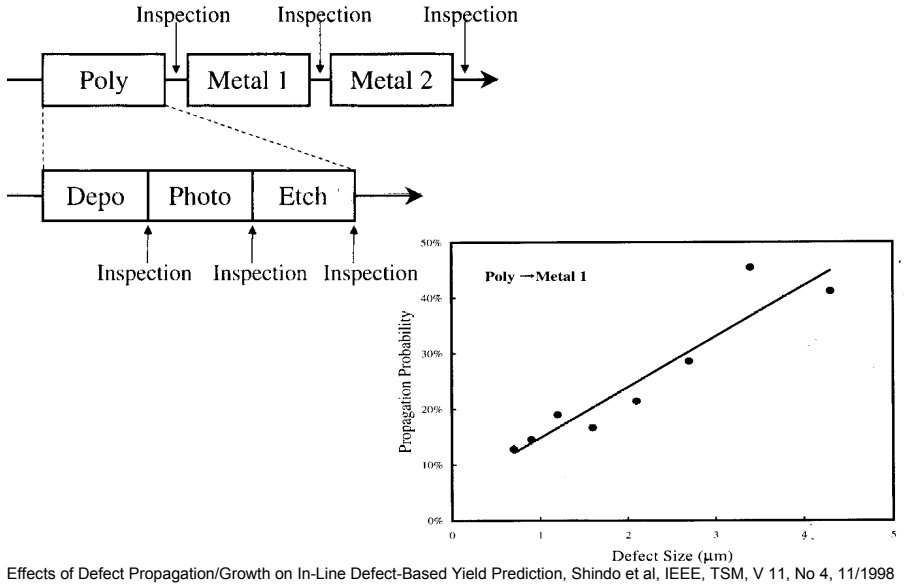
What do we need to know about particles

- Spatial distribution
- Size distribution
- Interaction of above with layout of circuit

Typical Defect Size Distribution

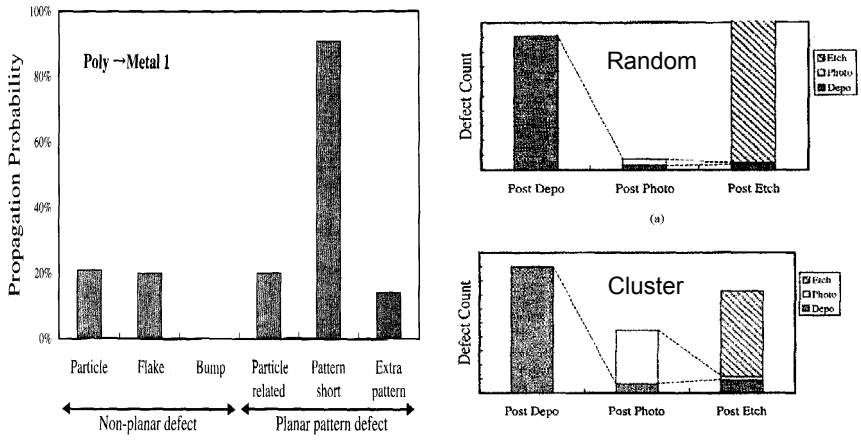


How do Defects Propagate in Process?



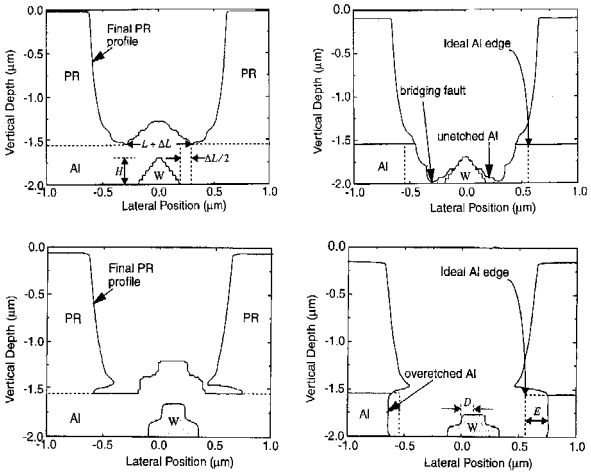
Effects of Defect Propagation/Growth on In-Line Defect-Based Yield Prediction, Shindo et al, IEEE, TSM, V 11, No 4, 11/1998

How do Defects Propagate in Process?



Defect impact simulation

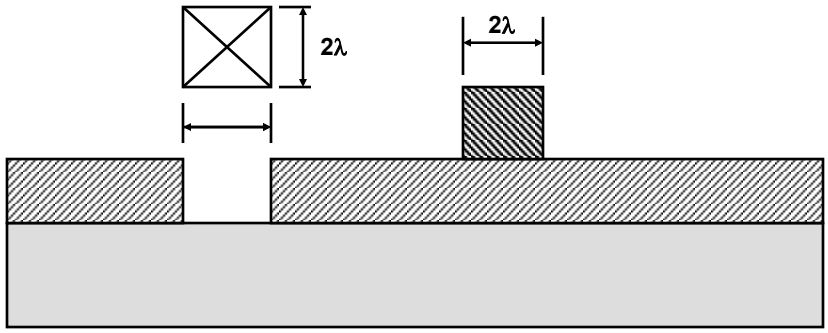
- One can now simulate the “evolution” of defects during processing.



Efficient Macromodeling of Defect Propagation/Growth Mechanisms in VLSI Fabrication, Li et al, IEEE TSM, Vol 11, No 4, 11/1998

Design Rules

- Design rules are developed to guide designers in matters of processing capability.
- Practical Design rules are a gross simplification of how an actual process behaves.



Design Rules (cont)

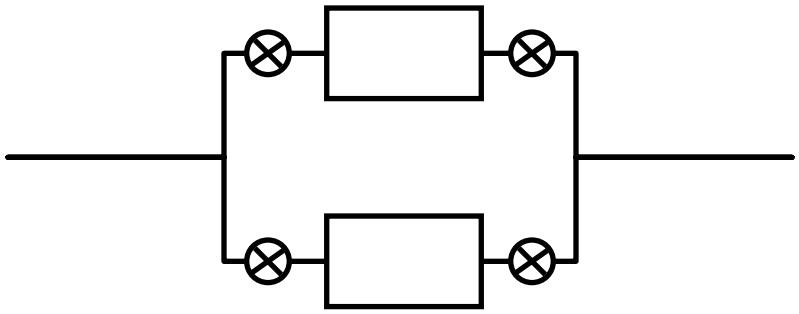
Lamda (λ) based design rules allow:

- The effective summary of process behavior for the benefit of the designer.
- That standardization of layout design.
- The automation of scaling, design checking, etc.
- The simplification of design transitions from one technology to the next.
- The effective “modularization” of IC design.

Redundancy and other DFM techniques

	Digital	Analog
Functional	Design rules Fault tolerance	Design rules
Parametric	Worst Case design	Statistical Design

Defect Tolerant Digital Designs



Defect Tolerance Implementation Requirements

- No or very limited impact on performance visible to the user.
- No additional manufacturing steps.
- Defective redundant elements replaceable by other redundant elements.

Typical Memory Faults

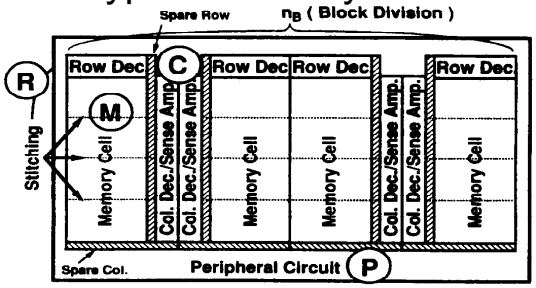


Fig. 1. Typical chip architecture.

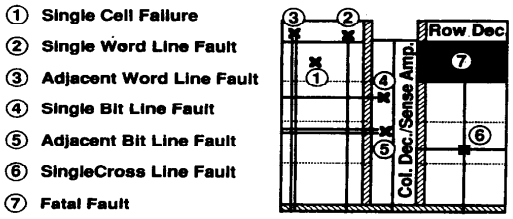
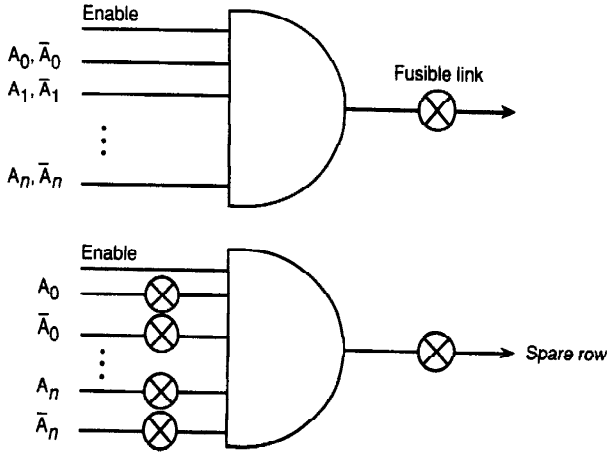


Fig. 2. Typical failure modes, caused by a single defect.

Redundancy in Memory ICs

Defective row / column replacement

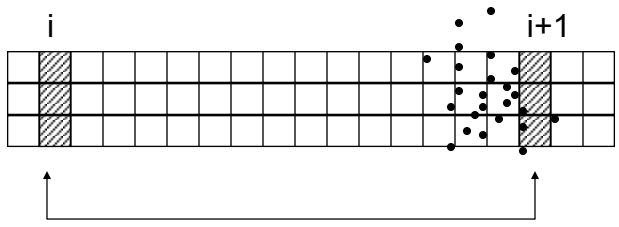


The problem with fuse links

- Electrical fuses are not very reliable.
- Laser trimming is expensive.
- Best techniques involve non-volatile memory programming.

Error Correcting Code Example

Parity allows correction of 16 kilobit failures out of 1 megabit.



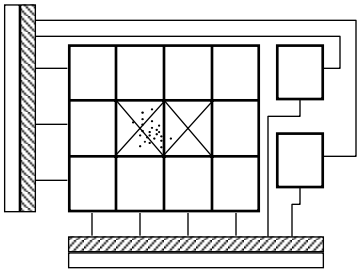
Consecutive bits in a word are stored at least 15 cells apart

Associative Approach

Sometimes, instead of replacing single rows or columns, one has to replace larger blocks destroyed due to wide fault clusters.

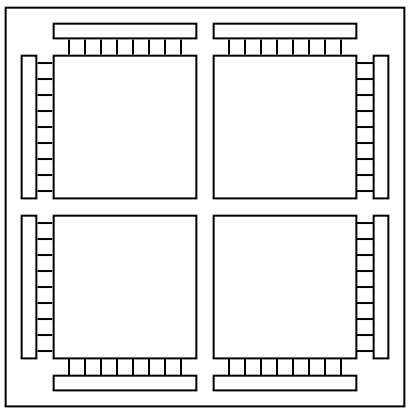
In this scheme the address of the block to be replaced is stored in a permanent memory.

Access time increase 2%. Power increase 0.6%, substantial area increase (27% for 1Mbit).



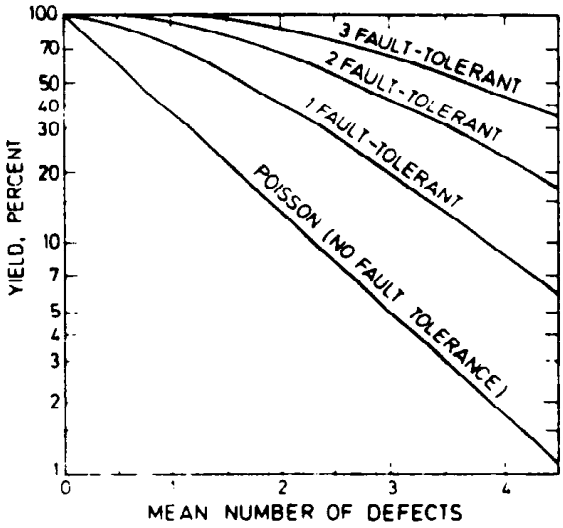
Partially Good Chips

A 1Mbit chip can be sold as a usable 0.5 Mbit, or even a usable 0.25Mbit chip.



Yield Modeling for Fault Tolerant Circuits

Assuming a simple Poison Model:



Yield Model for Fault Tolerant Circuits.

For non-fault tolerant designs:

$$Y = Y_o(1+D/\alpha)^{-\alpha}$$

For fault tolerant chips that have N modules with R spares:

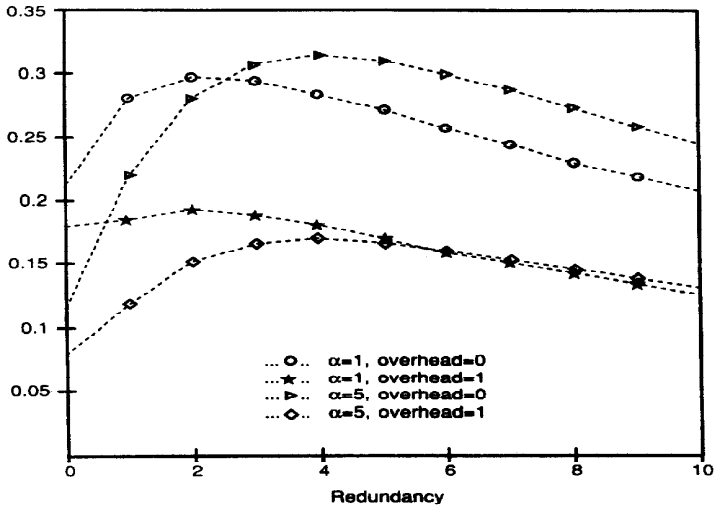
$$Y = Y_o \sum_{M=N-R}^{N} \alpha_{M,N}$$

$\alpha_{M,N}$ = *Prob* {Exactly M out of the N modules are fault-free}

$$\alpha_{M,N} = \sum_{k=0}^{N-M} (-1)^k \binom{N-M}{k} \binom{N}{M} \left[1+\frac{(M+k)D}{\alpha}\right]^{-\alpha}$$

Problem: what is the clustering parameter α of the module?

Effective Yield vs. Amount of Redundancy



"Effective" Yield takes into account Good die / wafer

Competitive Semiconductor Manufacturing Study

The Berkeley CSM survey is a comprehensive "field" study analyzing the elements of manufacturing competitiveness:

Technology, Integration, Automation, Process Control, Personnel Organization, Planning & Scheduling, Costing & Accounting.

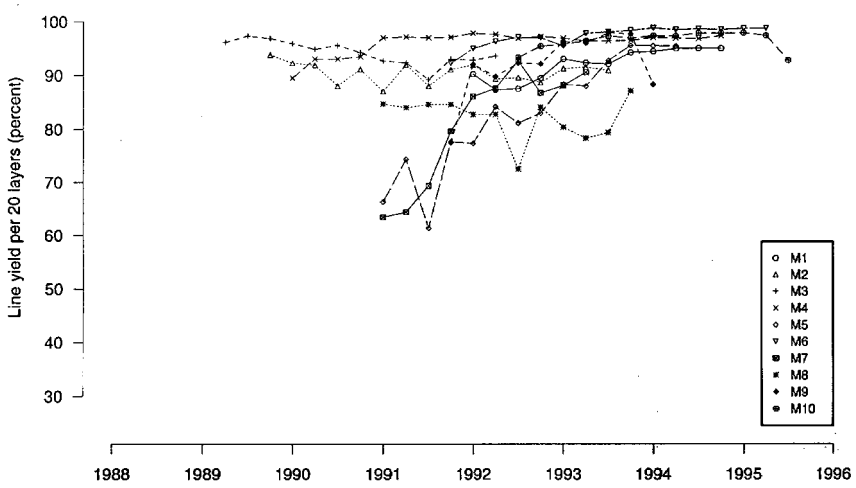
The focus is on "front end" production, digital ICs.

35 fabs around the world were targeted for 3-day visits by a multidisciplinary team of researchers.

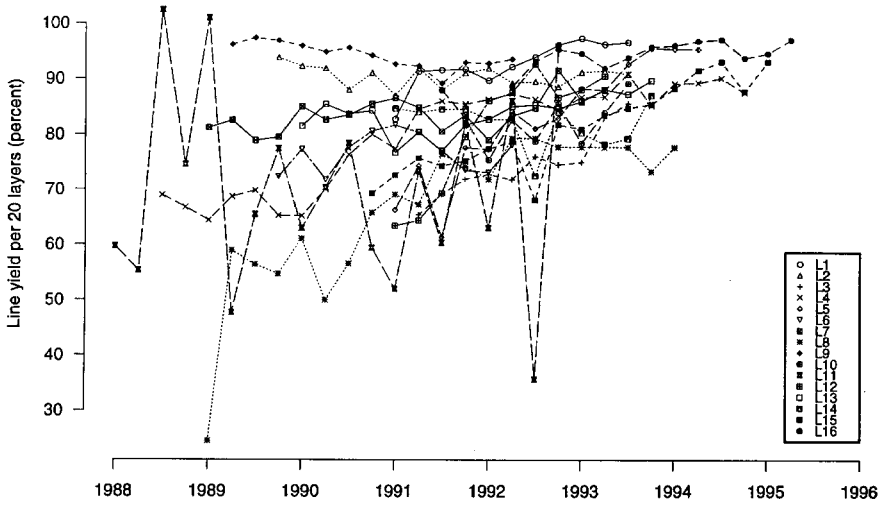
Information is shown for 16 fabs.

CSM, 3rd Report on the Results of the Main Phase, CSM-31, 8/1996

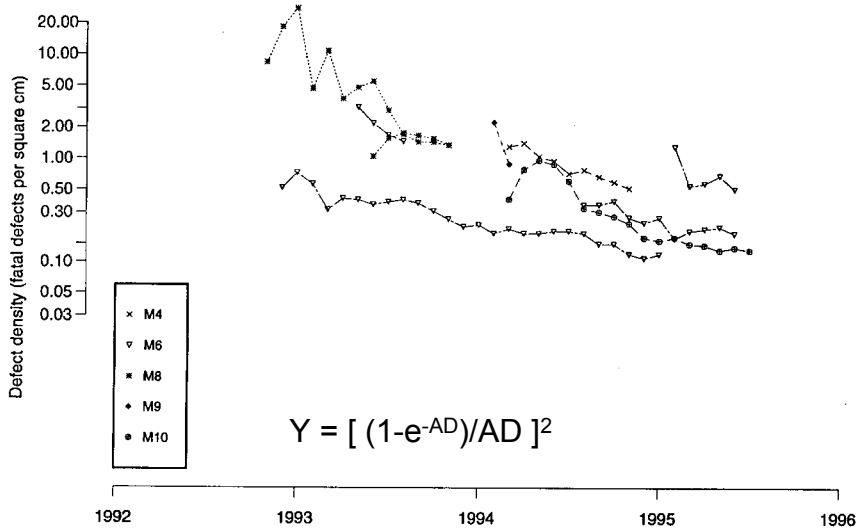
Line Yield, Memory



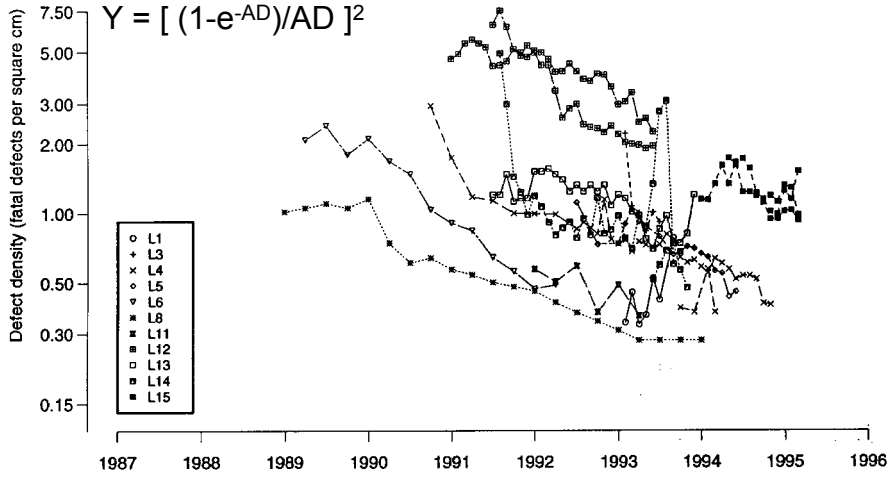
Line Yield, CMOS Logic



Memory Defect Density, 0.45-0.6μm

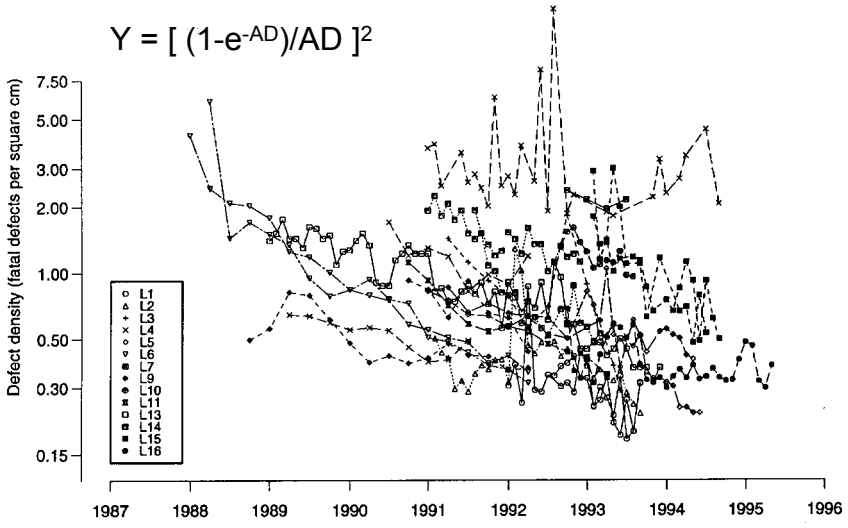


Logic Defect Density, 0.7-0.9μm CMOS



Logic Defect Density 1.0-1.25μm CMOS

$Y = [(1-e^{-AD})/AD]^2$



A More Dynamic View of Yield

- The Yield of each new process-product combination follows a trajectory called the yield learning curve.
- Time to yield for a new product can have huge implications.
- Also, field reliability is often related to yield.
- 1 Quarter sooner => 1 billion more sales over a 10 quarter lifetime.

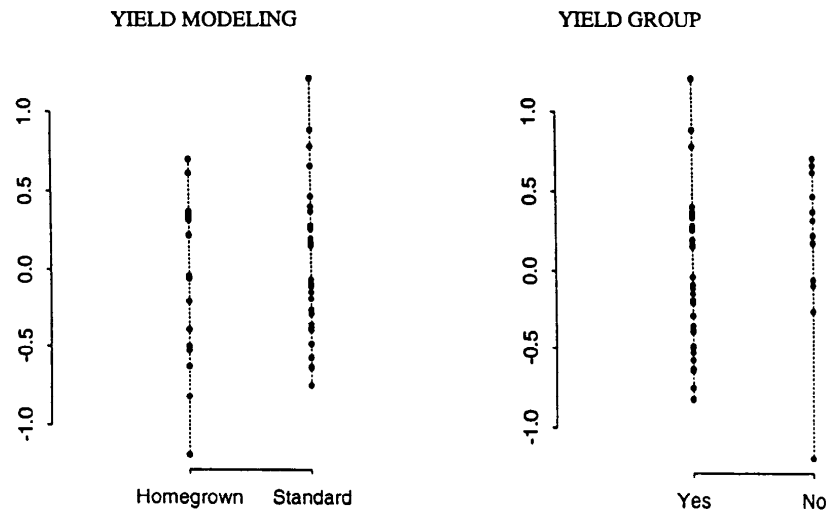
A Comprehensive Model from the Field Study

When all the factors were examined, an empirical model that predicted yield contained the following factors:

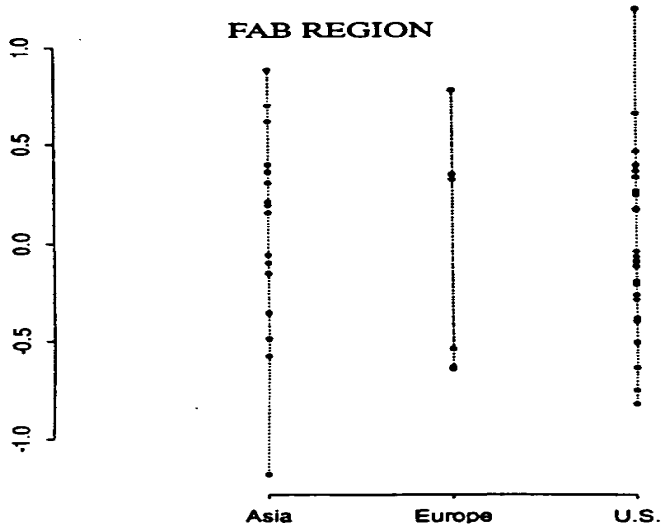
$$W=\log\left[\frac{Y}{1-Y}\right]=$$

$$.38 - (.96)(\text{dieSize}) + (.37)\log(\text{ProcessAge}) -(.28)(\text{PhotoLink})$$

Survey Residuals



Survey Residuals (cont)



What Drives Yield Learning Speed?

For each factory, this model was used to calibrate learning speed by the α_{2j} coefficient.

$$W_j = \alpha_{0j} + \alpha_{1j}\,(\text{dieSize}) + \alpha_{2j}\,\log(\text{ProcessAge})$$

Due to the small sample size, analysis was done with the help of contingency tables.

What Drives Yield Learning Speed? (cont)

RATING	SPC AUTOMATION		EXTENT OF SPC		
	Yes	No	High	Med	Low
High	2	0	0	2	0
Med	5	0	2	3	0
Low	2	3	1	1	3

RATING	PAPERLESS FAB		RECIPE DOWNLOAD		
	Yes	No	Full	Semi	Manua
High	0	2	0	2	0
Med	3	2	2	2	1
Low	1	4	1	0	4

RATING	YIELD MODEL		YIELD GR(
	Home	Away	Yes
High	1	1	2
Med	1	4	3
Low	2	3	3

RATING	FAB REGION		
	U. S.	Asia	Europe
High	2	0	0
Med	2	2	1
Low	3	2	0

In Summary

Yield modeling, measurement and control is vital in semiconductor manufacturing.

“Process Control” has interesting technical, as well as cultural aspects.

Yield learning is driven by competition and made even because of an ever improving equipment base.

Future advances will further decrease cycle time, increase wafer and die yield, and give more uniform performances for current geometries.

It will be a serious challenge to bring these improvements to the factory of 2010 with 0.03μm geometries and >>12 inch wafers.

Next frontier for yield improvement: Parametric Considerations and Equipment Utilization!