Sensors and Metrology

A Survey

Outline

- General Issues & the SIA Roadmap
- Post-Process Sensing (SEM/AFM, placement)
- In-Process (or *potential* in-process) Sensors
  - temperature (pyrometry, thermocouples, acoustic waves)
  - pressure and flow (manometers, momentum devices)
  - composition (OES, LIF, RGA, mass Spectroscopy Actinometry)
  - thickness (reflectometry, ellipsometry, scatterometry)
  - smart-dummy wafers and smart substrates

Introduction

- Sensors (and actuators) are key limiting factors in application of control techniques to semiconductor manufacturing
- sources of difficulty
  - implementation environment (vacuum, clean facilities, etc.)
  - perception that in-situ sensors affect process
  - ex-situ sensors can reduce throughput
  - cost of ownership
  - traditional resistance in industry

General Remarks on Sensors

- modeling is often key part of sensing
  - physical quantity of interest may not be directly measured (ex: OES indirectly contains info about etch process state)
  - thus, sensors are based on a model of the underlying physical process

  sensors = model + data

- signal processing
  - needed to reduce noise, improve bandwidth
  - difference between *data* and *information*
- problems
  - sensors require calibration
  - must account for drift
- other issues
  - sensor fusion
  - data compression

Key Issues in Sensors

- some key tradeoffs
  - non-invasive vs. invasive
  - non-destructive vs. destructive
  - in-situ vs. ex-situ
  - speed vs. accuracy
  - noise
- bias (accuracy) vs. precision (repeatability + reproducibility)
  - a sensor could be inaccurate, (thermocouple readings are off by 4º K)
  - but the sensor might have good precision, (it is *consistently* off)
  - precision is often more important for process control
- modern filtering and estimation methods can be of great use in improved sensing software.

2002 SIA Road Map Challenges

CD AND LEFF CONTROL [FRONT END PROCESSES AND LITHOGRAPHY]

The control of Critical Dimension (CD) etching especially at gate level has traditionally been one of the more difficult challenges. In recent years it has become common practice to use etch processes that result in a gate dimension (effective gate length: Leff) that is smaller than that printed in the resist. More complex etch processing must be executed while still maintaining the overall gate 3-sigma dimensional tolerance. In addition, the shape of the sidewall profile must be maintained in order to achieve acceptable sidewall oxide coverage and reliability. Another challenge is stopping the etch process at a very thin gate dielectric without cutting a trench into the underlying silicon.

MASK-MAKING [LITHOGRAPHY]

Mask-making capability and cost escalation will continue to be critical to future progress in lithography and will require continued attention. As a consequence of aggressive roadmap acceleration particularly in terms of MPU gate linewidth (post etch) and increased mask error factors (MEFs) associated with low k1 lithography, mask linewidth controllability fails to meet the requirements of the chipmakers. For example, in the 1997 Roadmap, the 70 nm node device required 4' masks to achieve 9 nm of CD control for isolated lines and 14 nm for contacts. The current CD control requirements are 3.4 nm for isolated lines and 4.3 nm for contact when MEF is assumed to be 1.4 and 3.0, respectively. Mask equipment and process capabilities for complex optical proximity correction (OPC) and phase shift masks (PSM) are currently available, while mask processes for post-193 nm technologies are still at a research and development stage. Mask damage caused by electrostatic discharge (ESD), which has long been a concern, is likely to be even more problematic as mask feature sizes will shrink further and masks for 157 nm lithography will be kept in atmospheres nearly free of water.

PROCESS CONTROL [LITHOGRAPHY] Process control, particularly for overlay and linewidths, also represents a major challenge. It is unclear whether metrology, which is fundamental for process control, will be upgraded adequately to meet future requirements. Resist line edge roughness (LER) becomes increasingly significant as gate linewidth control needs to become as precise as size of a polymer unit. Next -generation lithography will require exposure tool of totally new concept. The new tool must be developed and proven to meet reliability and utilization requirements to realize cost-effective production

INTEGRATION OF NEW PROCESSES AND STRUCTURES [INTERCONNECT]

Combinations of new materials, structures, and processes increase integration complexity. In the process of forming contact holes, a barrier metal that prevents interaction between wiring and insulation film, and a related new process technology need to be developed. Also, a technology that fills contact holes with metal so they have a high aspect ratio (A/R) is also required. As the feature size continues to shrink, it becomes more challenging to develop new insulating materials that prevent metal diffusing and a new process technology as well.

The 2002 update Metrology Road Map

Table 97a Metrology Technology Requirements—Near-term

	Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*Driver*
	DRAM ½ Pitch (nm)	*130*	*115*	*100*	*90*	*80*	*70*	*65*	
	MPU / ASIC ½ Pitch (nm)	*150*	*130*	*107*	*90*	*80*	*70*	*65*	
	MPU Printed Gate Length (nm)	*90*	*75*	*65*	*53*	*45*	*40*	*35*	
	MPU Physical Gate Length (nm)	*65*	*53*	*45*	*37*	*32*	*28*	*25*	
	Microscopy								
Was	Inline, nondestructive microscopy resolution (nm) for P/T=0.1	0.65	0.53	0.45	0.37	0.32	0.3	0.25	*MPU Gate*
Is	Inline, nondestructive microscopy resolution (nm) for P/T=0.1	0.5	0.4	0.4	0.3	0.3	0.2	0.2	*MPU Gate*
Was	Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	11.4	11.9	12.4	13	13.6	14.3	15.2	
Is	Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	11.4 150	11.9 130	12.4 110	13 90	13.6 80	14.3 70	15.2 65	*D1/2*
	Materials and Contamination Characterization								
	Real particle detection limit (nm) [B]	65	53	45	37	32	30	25	*D1/2*
	Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	43	35	30	24	21	20	17	*D1/2*
	Specification limit of total surface contamination for critical COI surface materials (atoms/cm^2) [C]	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	5.00E+09	*MPU Gate*
	Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	5.00E+08	*MPU Gate*

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

The 2002 update Metrology Road Map

Table 97b Metrology Technology Requirements—Long-term

	Year of Production	*2010*	*2013*	*2016*	*Driver*
	DRAM ½ Pitch (nm)	*45*	*32*	*22*	
	MPU / ASIC ½ Pitch (nm)	*45*	*32*	*22*	
	MPU Printed Gate Length (nm)	*25*	*18*	*13*	
	MPU Physical Gate Length (nm)	*18*	*13*	*9*	
	Microscopy				
Was	Inline, nondestructive microscopy resolution (nm) for P/T=0.1	0.18	0.13	0.09	*MPU*
Is	Inline, nondestructive microscopy resolution (nm) for P/T=0.1	0.15	0.11	0.07	*MPU*
Was	Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	16.1	19.3	23.2	*D1/2*
Is	Microscopy capable of measurement of patterned wafers having Maximum aspect ratio / diameter (nm) (DRAM contacts) [A]	16.1 45	19.3 32	23.2 22	D1/2
	Materials and Contamination Characterization				
	Real particle detection limit (nm) [B]	18	13	9	*D1/2*
	Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	12	9	6	*D1/2*
	Specification limit of total surface contamination for critical COI surface materials (atoms/cm^2) [C]	5.00E+09	5.00E+09	5.00E+09	*D1/2*
	Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	5.00E+08	5.00E+08	5.00E+08	*D1/2*

White–Manufacturable Solutions Exist, and Are Being Optimized
Yellow–Manufacturable Solutions are Known
Red–Manufacturable Solutions are NOT Known

Sensor-based Metrology

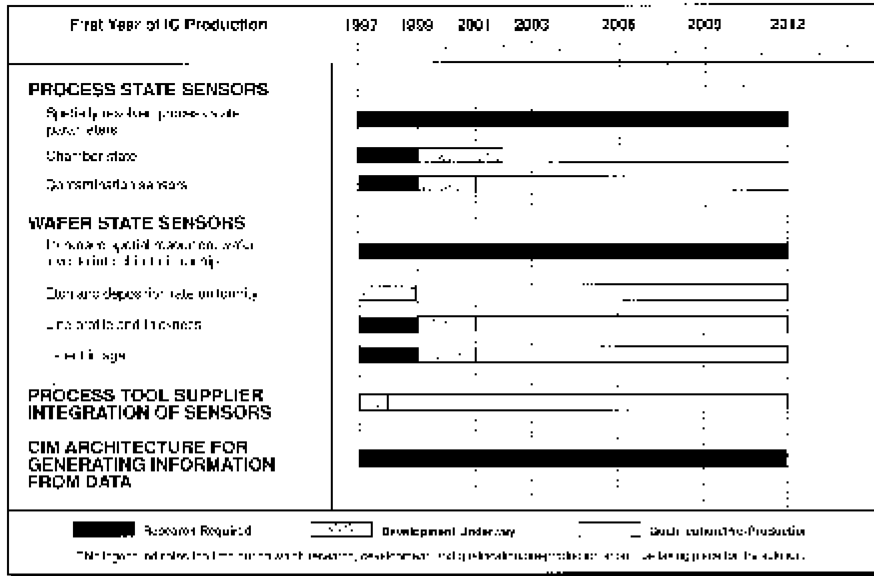


Figure 47 Sensor-based Metrology for Integrated Manufacturing Potential Solutions

Materials and Contamination

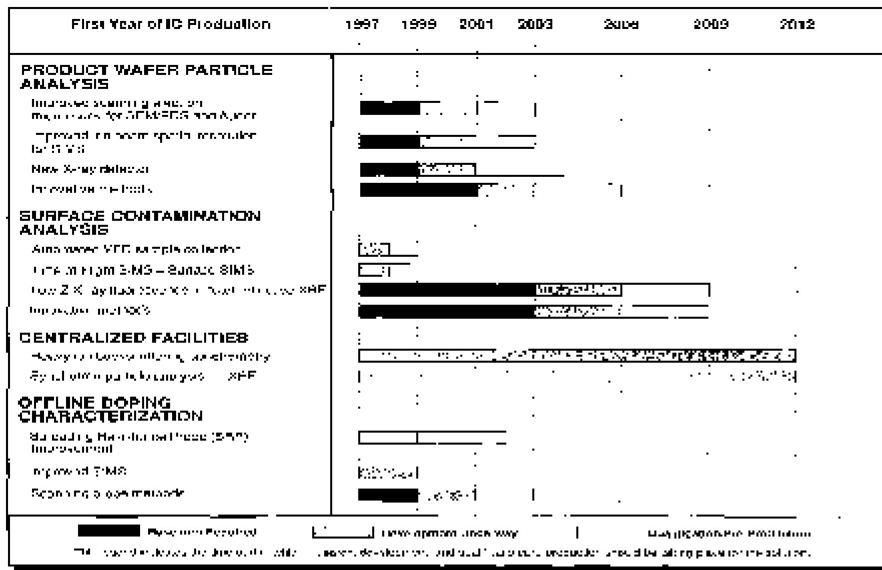
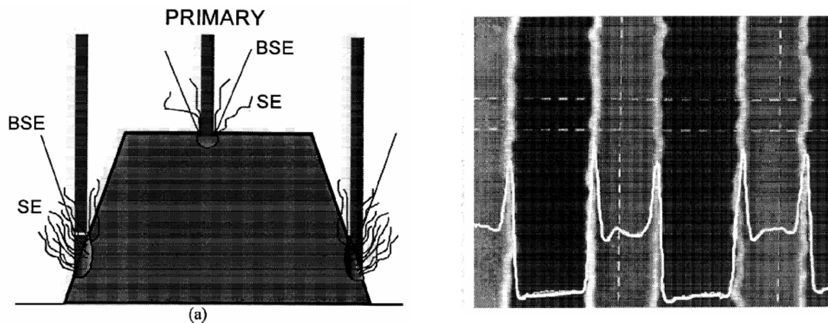


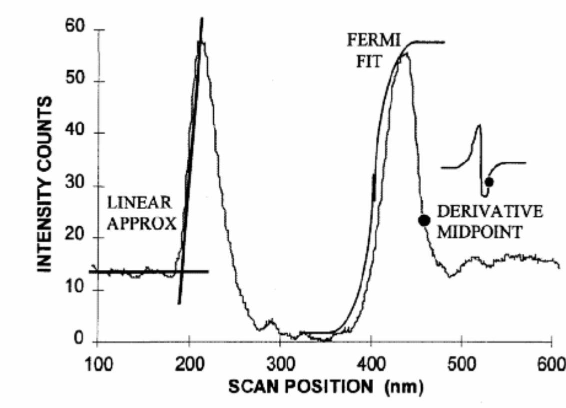
Figure 48 Materials and Contamination Characterization Potential Solutions

CD Metrology

- CD-SEM is today's pre-eminent technique…
- Electron yield in interaction volume is a function of surface topography (*Secant effect*) and atomic number.
- Extracting CD is not so simple...



Various Edge Detection Algorithms are in use...



CD-SEMs are often calibrated with AFMs

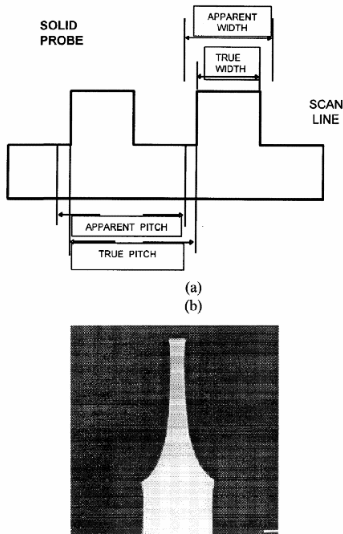


Figure 3 - (a) Effect of probe width on Pitch and Line Width measurements.(b) Image of flared CD AFM tip.

Atomic force Microscopy uses either repulsive forces (sub nm proximity), or weaker attractive forces (a few nm away).

Tip tracks surfaces using feedback control.

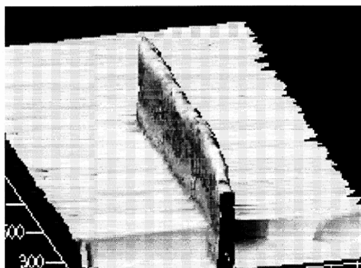
Shape and size of tip is the critical source of errors.

Standard features are use to calibrate and "de-convolve" the tip profile from the measurements.

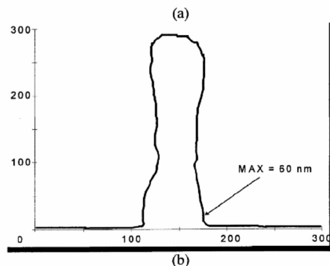
AFM is 100-1000 times slower than a CD-SEM.

AFM is sensitive to line-edge roughness.

CD-SEM vs AFM standards

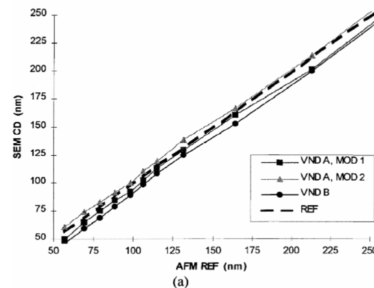


(a)

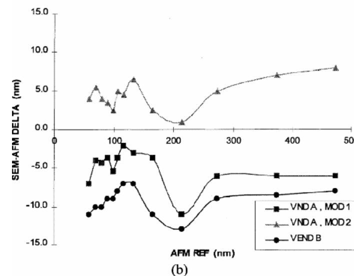


(b)

Figure 5 - Etched Poly-Si lines for nano-scale devices.



(a)



(b)

Figure 6 - SEM linearity for isolated poly-Silicon lines.

CD-SEM cannot "see" the actual profile...

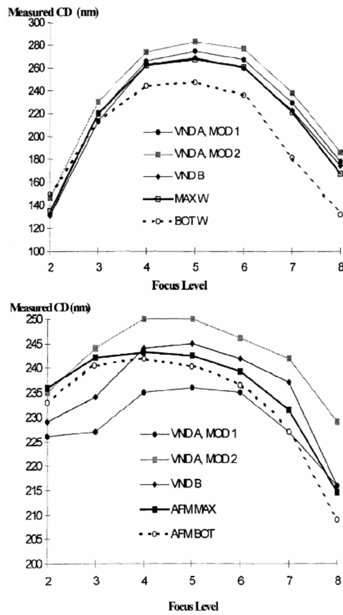
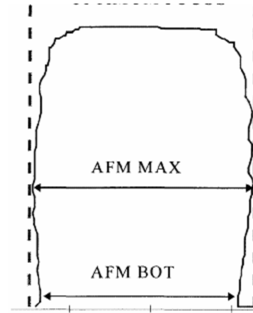
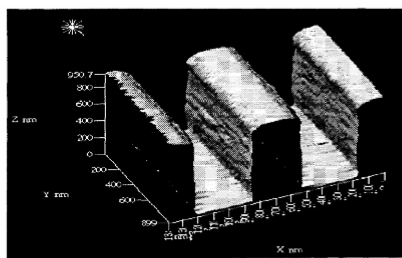


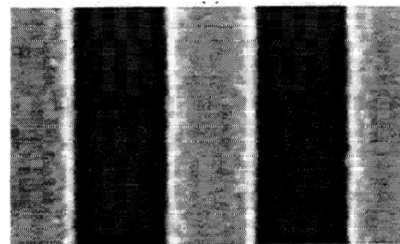
Figure 10 - SEM comparison for dense lines

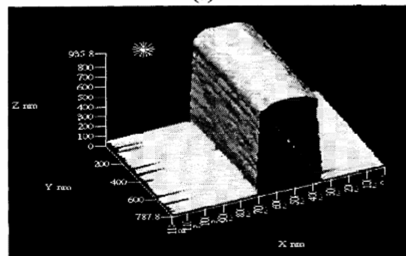


Dense vs. Isolated Lines

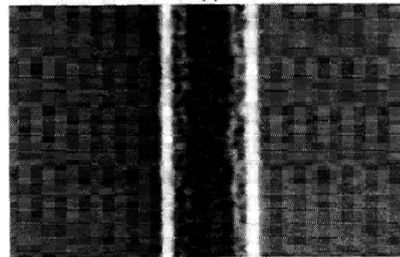

(a)

dense


(c)


(b)

iso


(d)

Comparison for Contact holes

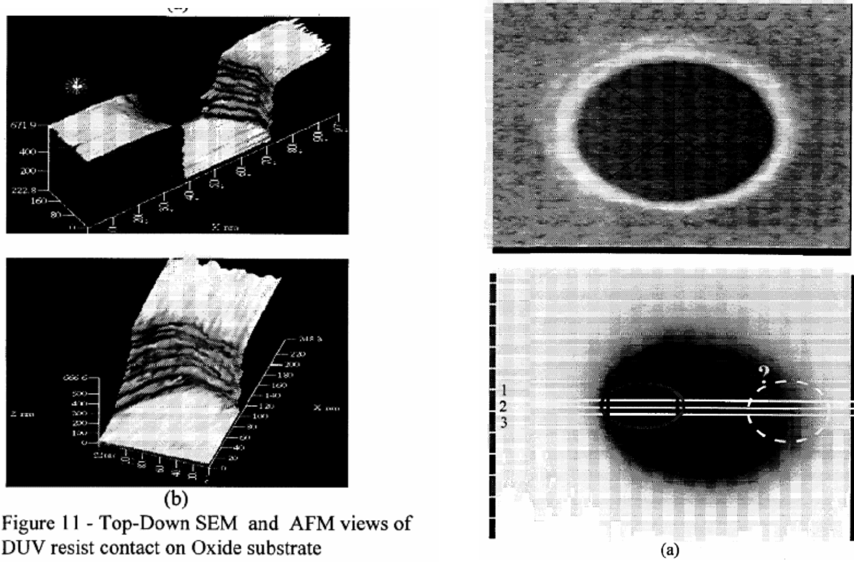


Figure 11 - Top-Down SEM and AFM views of DUV resist contact on Oxide substrate

More CD-SEM vs AFM comparisons

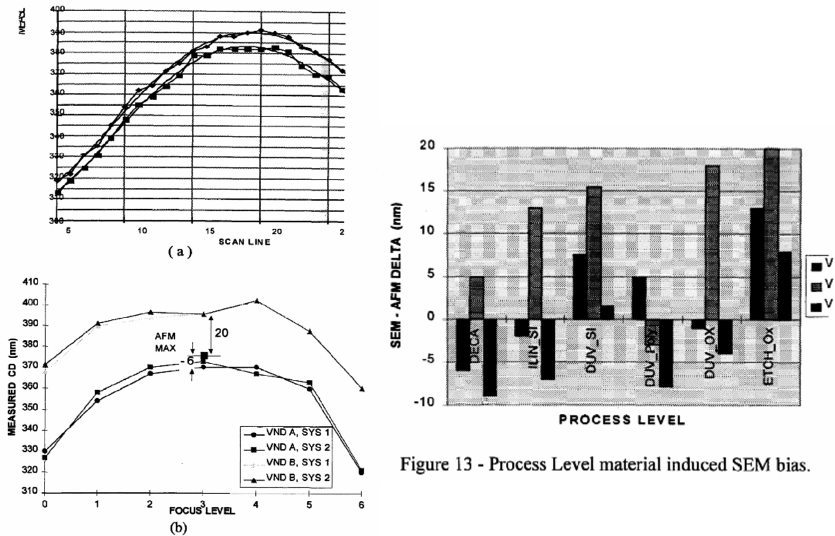
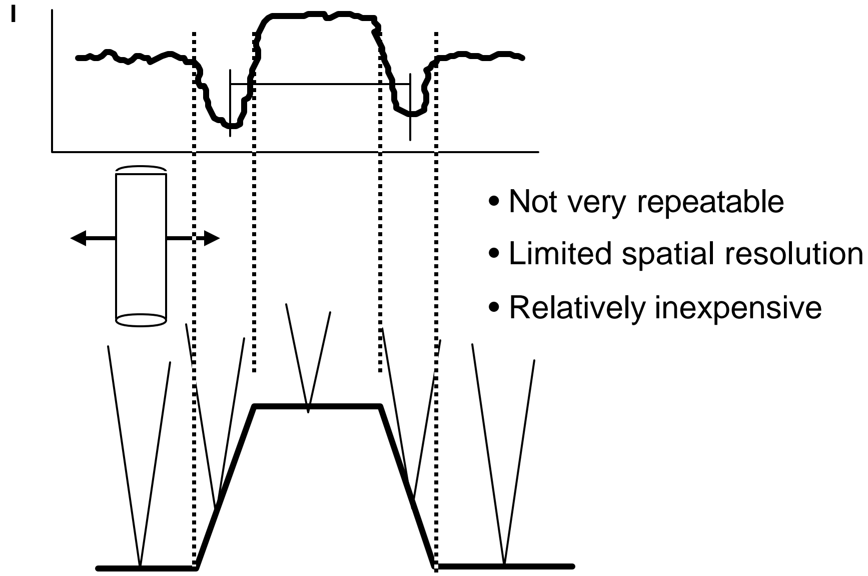


Figure 12 - (a) Polynomial fitting to determine the contact diameter (b) Matching data for tools of the same model.

Figure 13 - Process Level material induced SEM bias.

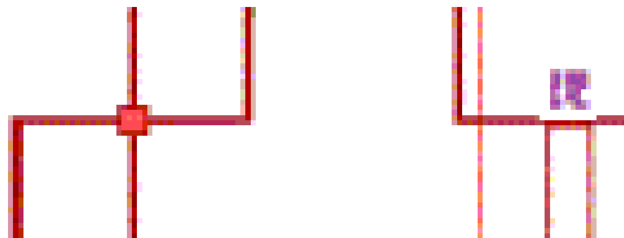
Optical CD Measurement



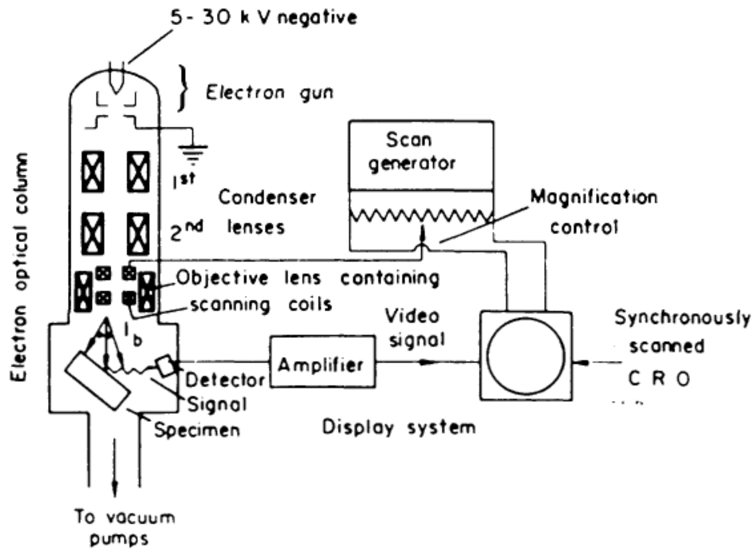
- Not very repeatable
- Limited spatial resolution
- Relatively inexpensive

Electrical CD Measurement

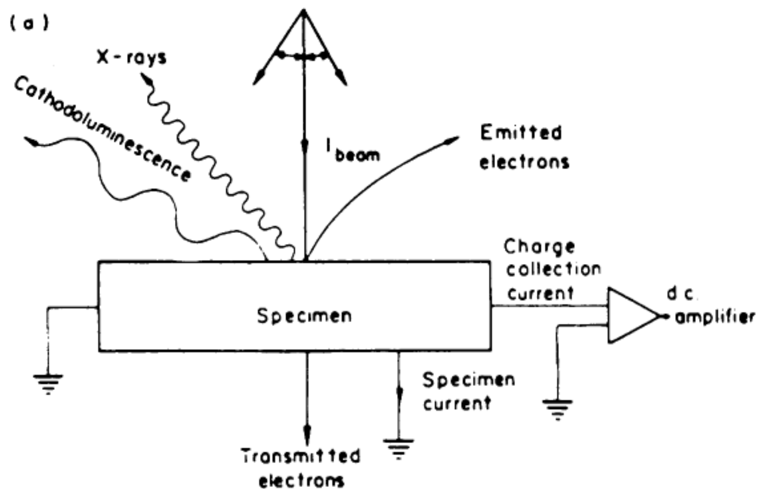
Measurement is very repeatable and fast.
Can only be used in conductive layers.
Need at least one conductive layer and one insulator.
Can be extended for misalignment measurements.



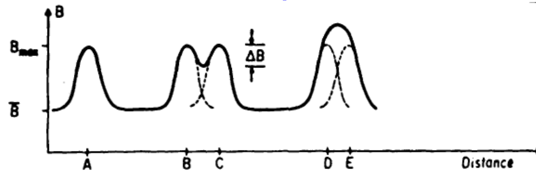
Basic SEM Structure



The Many Modes of SEM



The Issue of Spatial Resolution

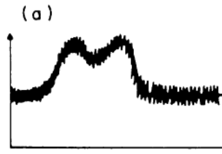


Two points are resolved when

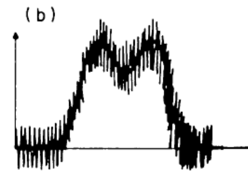
$B_{max} - \Delta B \leq 0.75 B_{max}$

or $\Delta B \geq 0.25 B_{max}$

(a)



(b)



$\overline{B} = 0.5\,B_{max}$
$\Delta B = 0.15\,B_{max}$
$C_t = 0.1$
gain = G

$\overline{B} = 0$
$\Delta B = 0.3\,B_{max}$
$C_t = 0.2$
gain = 2G

Chrome on Silicon Example

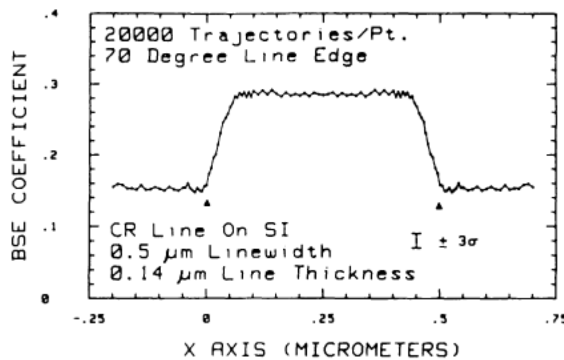


Fig. 2.9 Monte Carlo calculation of the backscattered electron signal response from a strip of chromium (thickness 0.14 μm, width 0.5 μm) on a silicon substrate scanned with a 10 nm diameter 20 keV beam. (From Hembree *et al.*, 1981.)

Signal Depends Stronlgy on Material

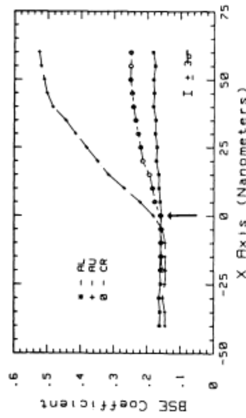


Fig. 2.10 Effect of atomic number on the backscattered electron signal resp from metallic strips on a silicon substrate (thickness 0.14 μm, width 0.5 μm; beam 1(diameter, 20 keV). (From Hembree et al., 1981.)

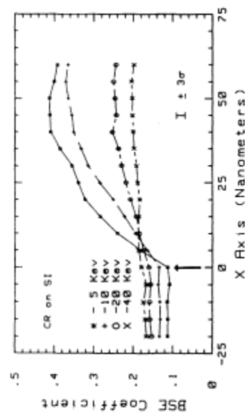
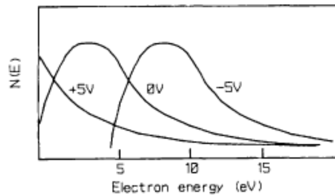
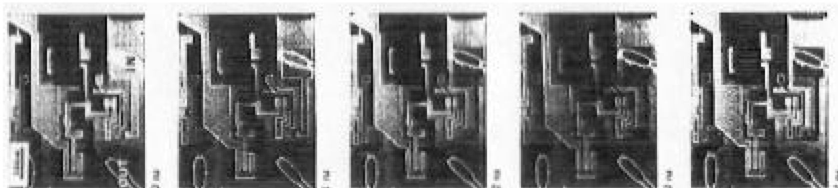


Fig. 2.11 Effect of beam energy on the backscattered electron signal response fro chromium strip on a silicon substrate (thickness 0.14 μm, width 0.5 μm; beam 10

Voltage Contrast SEM



5.5 Secondary electron energy spectrum versus specimen voltage.



CD Sem Resolution

Scanning Resolution shown to 1-5nm.

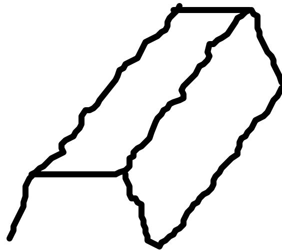
CD metrology on resist has 5-10nm precision.

Other solutions:

ATF, has (theoretically) atomic resolution.

Problem:

What *is* CD??



CD-SEM Conclusions

- Accuracy is several (many) nm.
- Precision (1-σ repeatability + reproducibility) is 2-5nm today.
- CD-SEM is stand-alone (I.e. expensive)
- CD-SEM measurements are available only after patterning, and data integration with control systems is difficult at best.
- AFM-based calibration will not be possible for trenches less than ~100nm wide.