Fall 2003 EE290H Tentative Weekly Schedule

1. Functional Yield of ICs and DFM.
2. Parametric Yield of ICs. ←
3. Yield Learning and Equipment Utilization.

IC Yield & Performance

4. Statistical Estimation and Hypothesis Testing.
5. Analysis of Variance.
6. Two-level factorials and Fractional factorial Experiments.

Process Modeling

7. System Identification.
8. Parameter Estimation.
9. Statistical Process Control. ***Distribution of projects. (week 9)***
10. Run-to-run control.
11. Real-time control. ***Quiz on Yield, Modeling and Control (week 12)***

Process Control

12. Off-line metrology - CD-SEM, Ellipsometry, Scatterometry
13. In-situ metrology - temperature, reflectometry, spectroscopy

Metrology

14. The Computer-Integrated Manufacturing Infrastructure

Manufacturing Enterprise

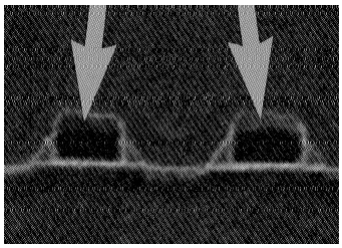
15. ***Presentations of project results.***

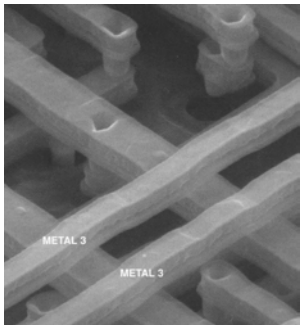
IC Yield and Performance (cont.)

- Defect Limited Yield
  - Definition and Importance
  - Metrology
  - Modeling and Simulation
  - Design Rules and Redundancy
- **Parametric Yield**
  - **Parametric Variance and Profit**
  - **Metrology and Test Patterns**
  - **Modeling and Simulation**
  - **Worst Case Files and DFM**
- Equipment Utilization
  - Definition and NTRS Goals
  - Measurement and Modeling
  - Industrial Data
- General Yield Issues
  - Yield Learning
  - Short loop methods and the promise of in-situ metrology

IC Structures can be highly Variable

Transistor





Interconnect

Variability will impact performance

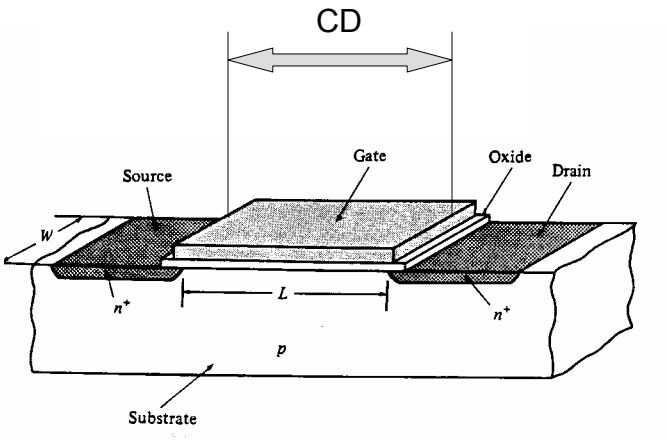
What *is* Parametric Yield?

- When devices (transistors) do not have the exact size they were designed for,
- when interconnect (wiring) does not have the exact values (Ohms/μm, Farads/μm2, etc.) that the designer expected,
- when various structures (diffused layers, contact holes and vias, etc.) are not exactly right,
- the circuit may work, but
- performance (speed, power consumption, gain, common mode rejection, etc.) will be subject to statistical behavior...

What are the Parametric Yield Issues?

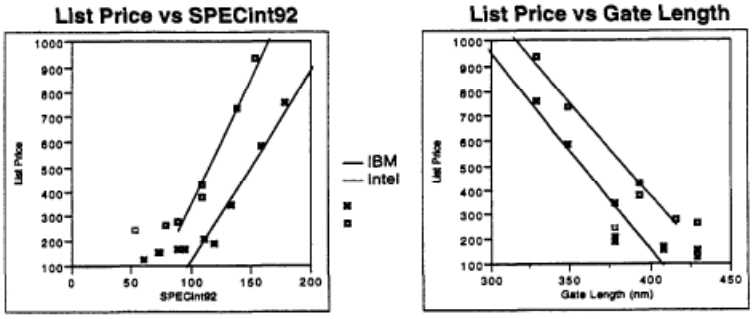
- Binning and Impact on Profitability
- The Process and Performance Domains
  - Characterizing the Process Domain
  - Identifying Critical Variables
  - Modeling Process Variability
  - Associated (Statistical) Metrology
- Process Variability and the Circuit Designer
- Design for Manufacturability Methods
- A Global (re)view of Yield

What is *the* Critical Dimension?



Gate is typically made out of Polysilicon

Basic CD Economics



Source: MicroDesign Resources

Leading Edge CD Control Revenue Leverage:

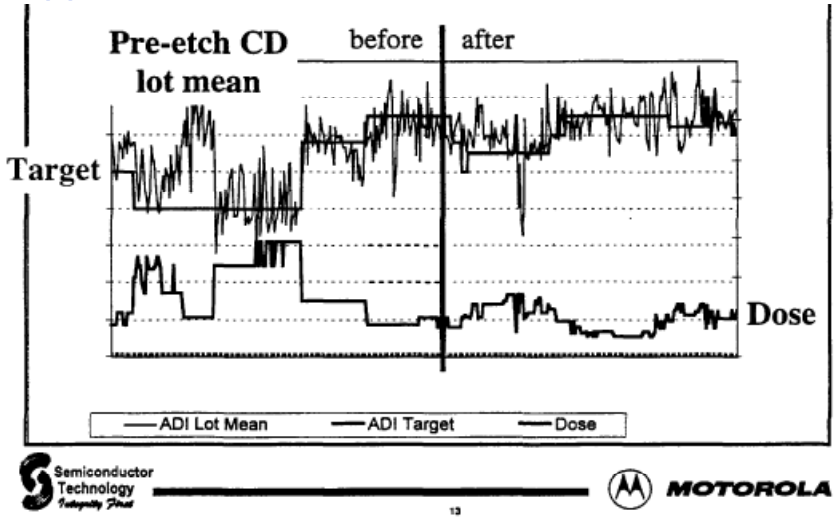
~ $7.5/nm

Semiconductor Technology

MOTOROLA

(D. Gerold et al, Sematech AEC/APC, Sept 97, Lake Tahoe, NV)

Application of Run-to-Run Control at Motorola



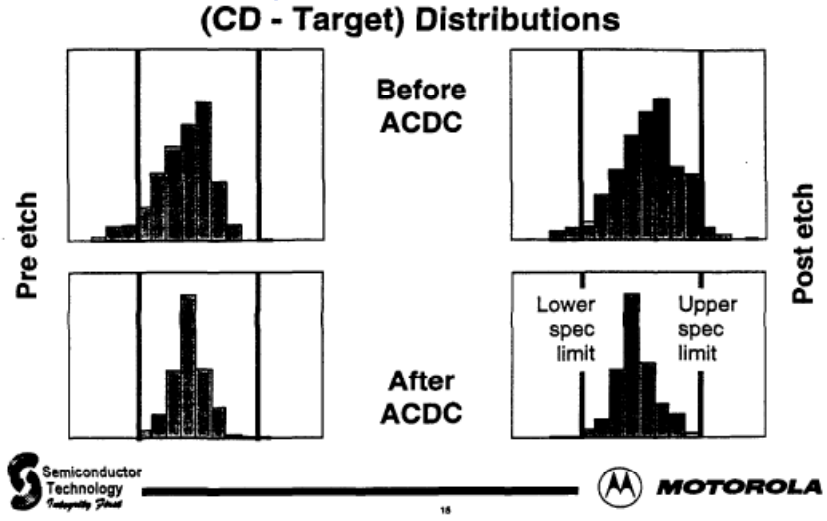
Semiconductor Technology

MOTOROLA

$$Dose_n = Dose_{n-1} - \beta\,(CD_{n-1} - CD_{target})$$

(D. Gerold et al, Sematech AEC/APC, Sept 97, Lake Tahoe, NV)

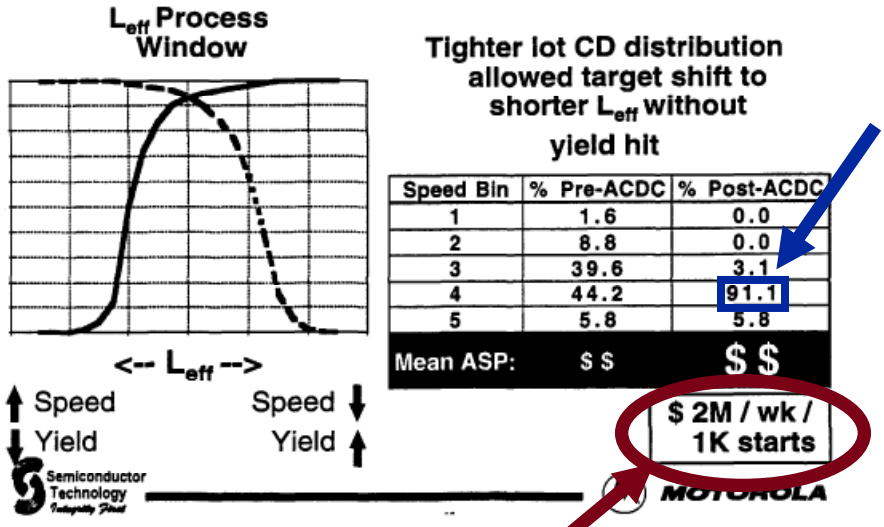
CD Improvement at Motorola



σ_{Leff} reduced by 60%

(D. Gerold et al, Sematech AEC/APC, Sept 97, Lake Tahoe, NV)

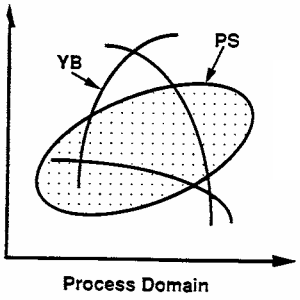
Why was this Improvement Important?



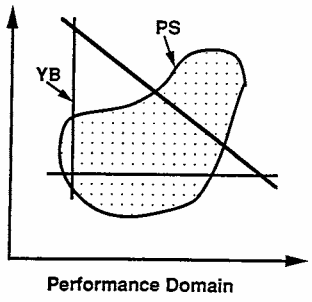
600k APC investment, recovered in two days...

Process and Performance Domains

- CD is not the only process variable of interest…
- Speed is not the only performance of interest…
- In general we have a mapping between two multi-dimensional spaces:

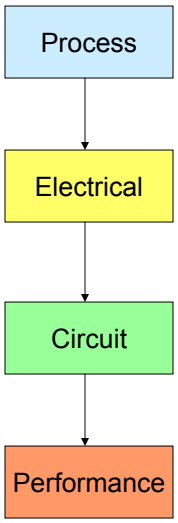


CD
Resistivities
Conductance of contacts and Vias
Dielectric capacitance per unit area...



Speed
Power
...

So, what to do?



What process parameters to measure?
How to reduce Process Variability?

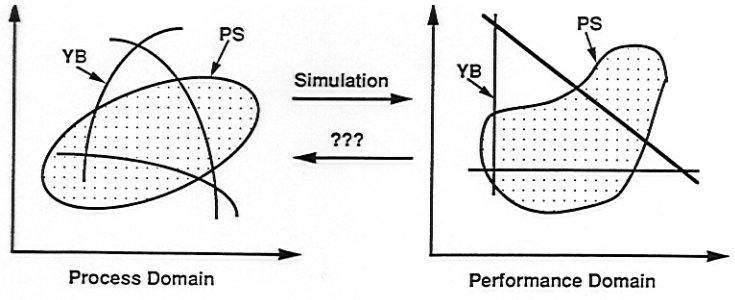
What electrical parameters matter?
How can we set reasonable specs on those?

How to simulate performance variation?
How to design a circuit that is immune to variation?

What performance is important?
What Process/Layout parameters can we change to satisfy critical performance specs?

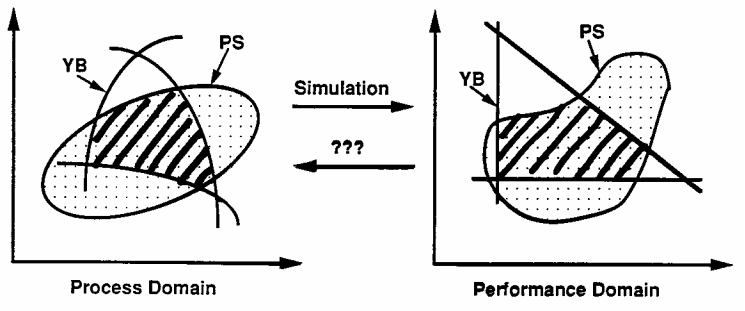
Translating Specifications between Domains

- Performance Specs, imposed by the market, translate to an “acceptability region” in the process domain.
- This “acceptability region” is also known as the Yield Body (YB).
- The Yield Body can be mapped into either domain.



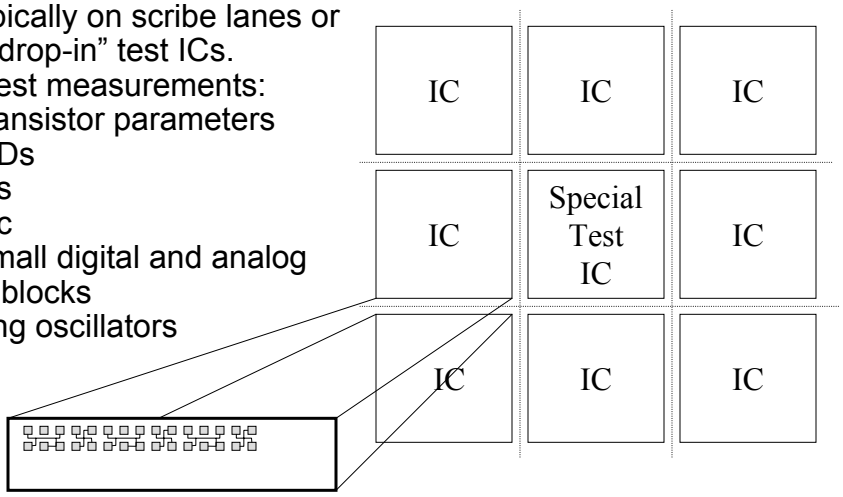
So what *is* Parametric Yield?

- One is interested in *mapping* and in *maximizing* the overlap between YB and PS.
- This can be accomplished in various ways.
  - first, we should be able to measure (characterize) the Process Spread (PS).
  - then, one has to figure the mapping from Process to Performance!
  - Finally, one needs design tools to manipulate the above.

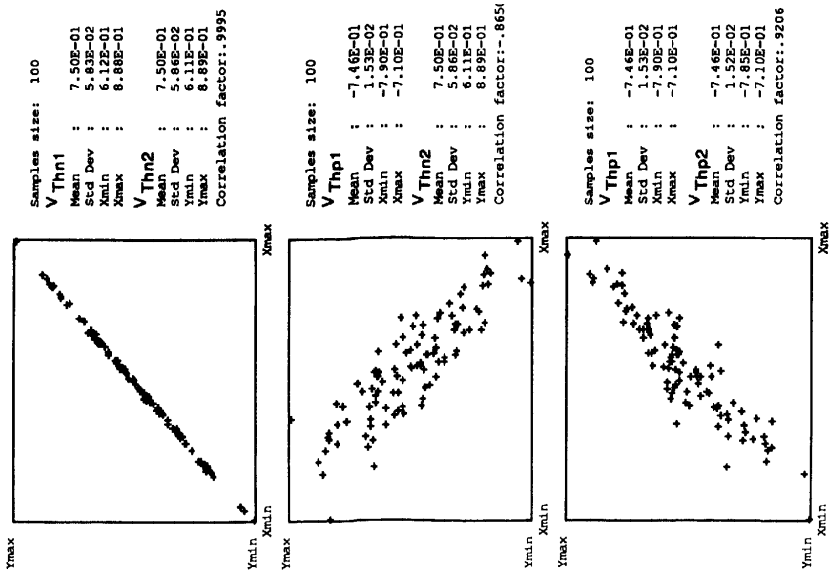


Parametric Test Patterns

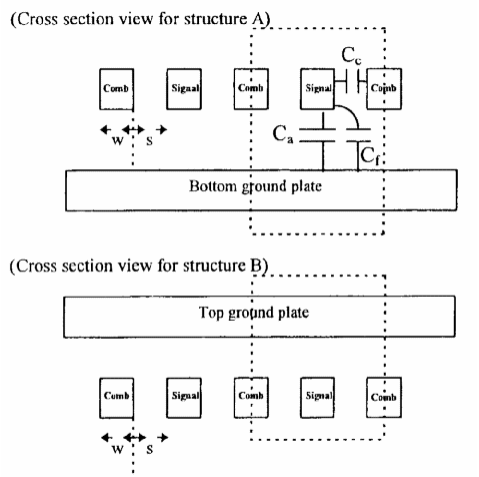
Typically on scribe lanes or in “drop-in” test ICs.
E-test measurements:
- transistor parameters
- CDs
- Rs
- Rc
- small digital and analog blocks
- ring oscillators



Parametric Transistor Measurements



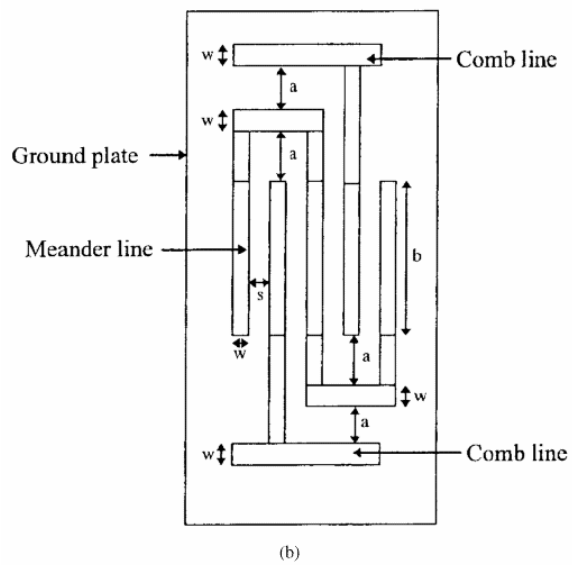
There is no agreement about Interconnect Parameters...



(a)

An Extraction Method to Determine Interconnect Parasitic Parameters, C-J Chao, S-C Wong, M-J Chen, B-K Liew, IEEE TSM, Vol 11, No 4. Nov 1998.

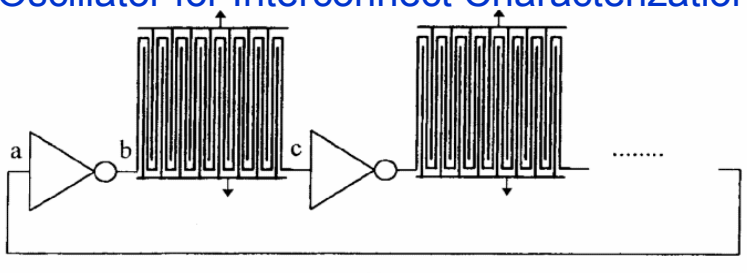
Interconnect Characterization Structures



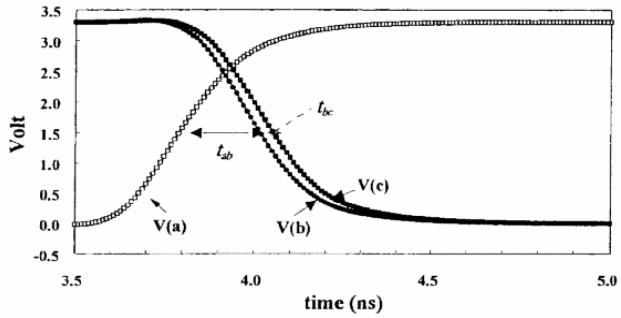
(b)

Fig. 1. Top view and cross section of interconnect parasitic test structure.

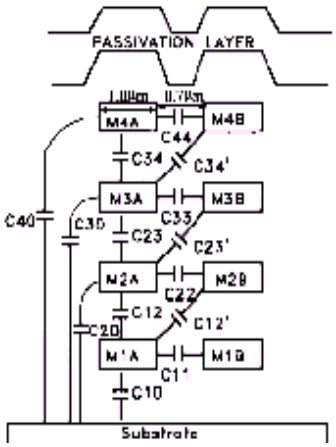
Ring Oscillator for Interconnect Characterization

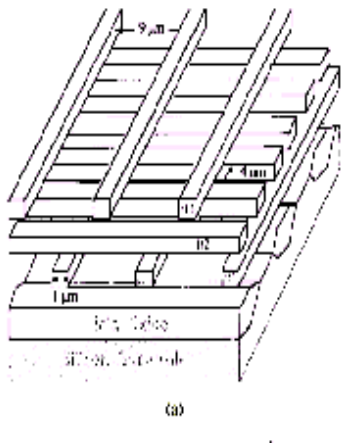


(a)



Interconnect Structures are very Complex...



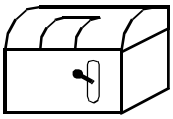


(a)

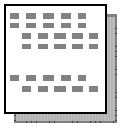
Statistical Metrology for CDs

Where does variability come from?
What are its *spatial* components?

Causal



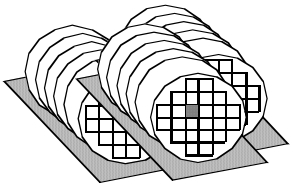
Equipment



Recipe

? Other

Spatial

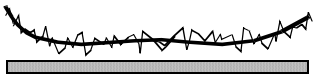


Within Die
Among Die
Among Wafers

Random/Deterministic

Response from Equipment A

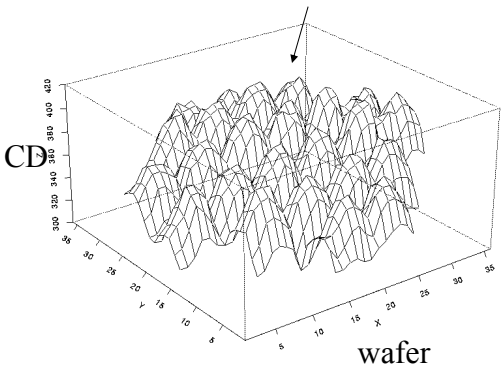
Random/Deterministic



Data Collection

- Electrical Measurements facilitate data collection.
- Raw data contains confounded variability components from the entire “short loop” process sequence.

You can “see” the boundaries of the stepper fields!



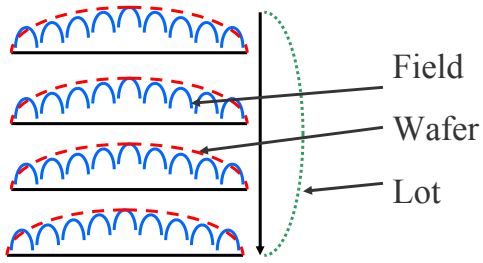
Nested Variance – A Simple Model

CD variation can be thought of as nested systematic variations about a true mean:

Spatial components

$$CD_{ijkl} = \mu + f_i + w_i + l_k + L_l + \sigma$$

μ: True mean; f_i: Across-field; w_i: Across-wafer; l_k: Across-lot; L_l: Lot-to-lot; σ: Random



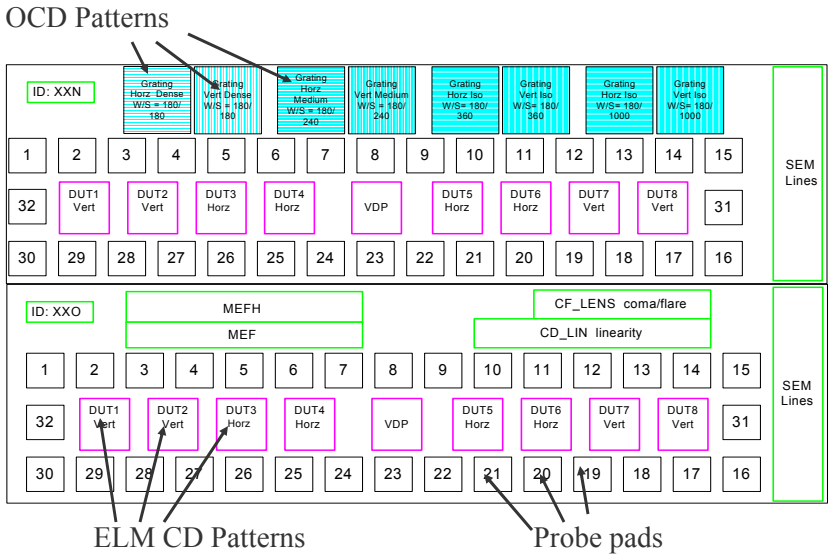
Experimental Design

- Use a mask with densely grouped test features to explore spatial variability.
- Electrical linewidth metrology (ELM) chosen as primary metrology due to its high speed.
- A fabrication process based on a standard 248 nm lithography process was used to print test wafers.

Test Mask Design

- Mask design consists of a 22x14 array of test modules
- Module has CD structures (ELM, CD-SEM, OCD) in varying pitch, orientation, and OPC use.
- Density of structures allows detailed variance maps using an “exhaustive” sampling plan.
- Three feature types measured for each module for every field on the wafer (all no-OPC).

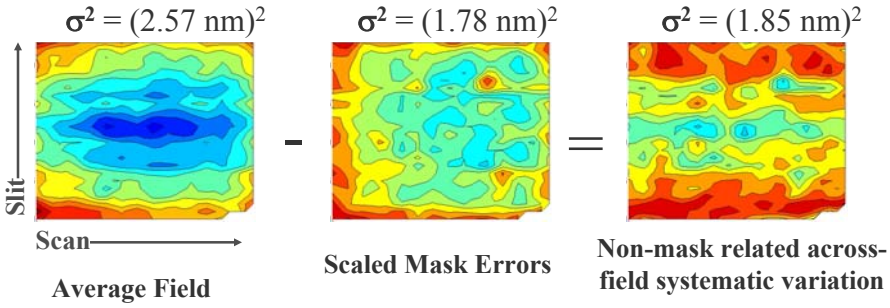
Test Mask Design (cont)



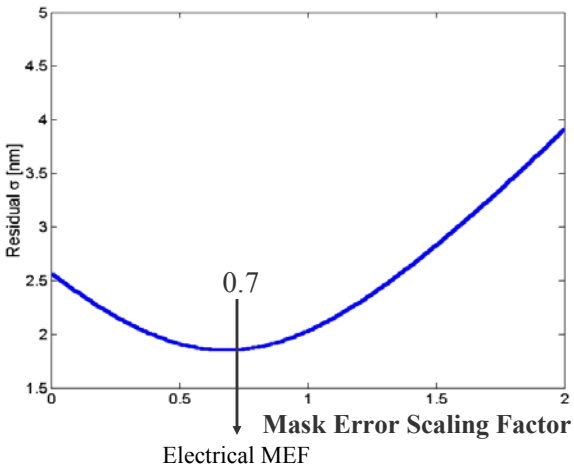
Across-Field Systematic Variation – Mask Errors

Calculate average field to see across-field systematic variation

Use mask measurements to decouple scaled mask errors from non-mask related systematic variation



Optimizing Mask Error Scaling Factor for ELM



Mask Errors
→ Aerial Image
→ Resist Pattern
→ Trim Etch
→ Poly Etch
→ Electrical Measurement

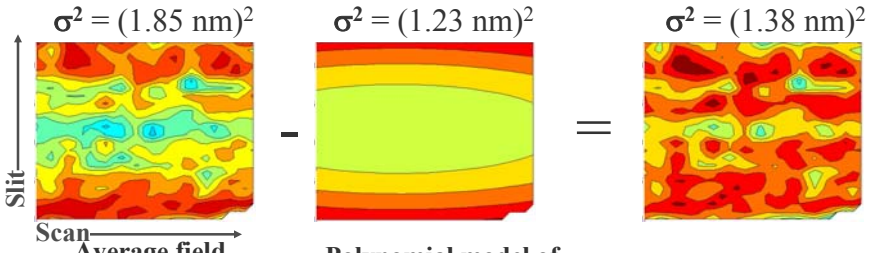
Optical MEF expected to be ~1.2

Mask error scaling factor optimized to minimize residuals when mask errors are removed from average field.

Across-Field Systematic Variation

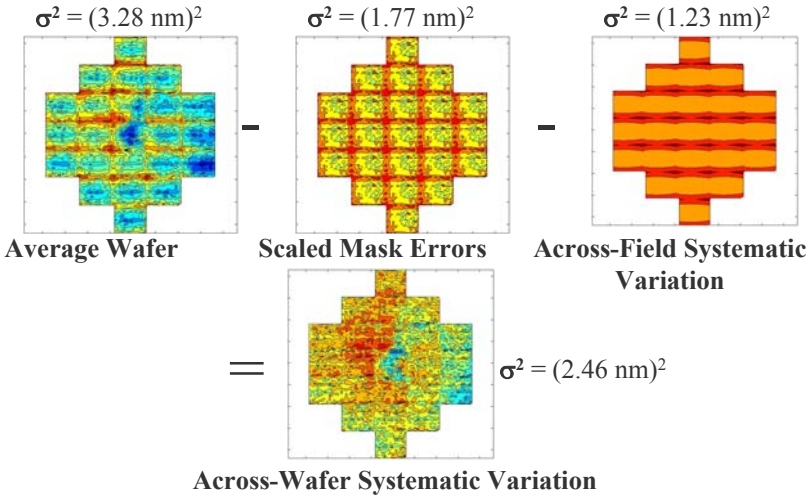
Polynomial model used to capture across-field systematic variation (inferred from examination of data):

$$CD(X_f, Y_f) = aX_f^2 + bY_f^2 + cX_f + dY_f$$



Across-Wafer Systematic Variation

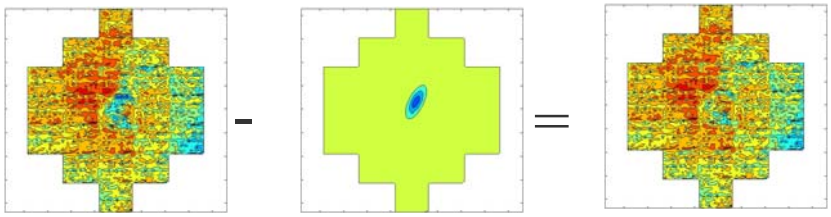
Separation of Across-Field and Across-Wafer Systematic Variation:



Across-Wafer Systematic Variation

- There is a distinct local drop in CD value in the wafer center, most likely linked to the way the develop fluid is dispensed.
- A bivariate Gaussian function was fitted to the data to remove this effect.

$\sigma^2 = (2.46\ \text{nm})^2$ $\sigma^2 = (0.52\ \text{nm})^2$ $\sigma^2 = (2.39\ \text{nm})^2$



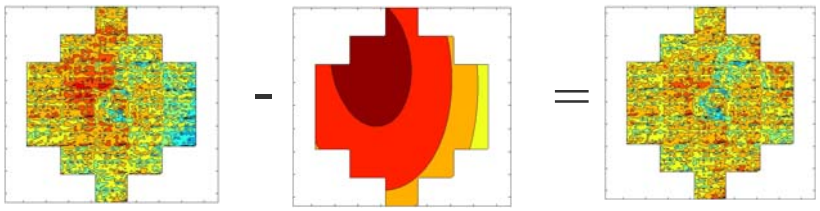
Across-Wafer Systematic Variation **Bivariate Gaussian Model** **Remaining Across-Wafer Systematic Variation**

Across-Wafer Systematic Variation

The remaining across-wafer systematic variation was removed using a polynomial model:

$$CD(X_w, Y_w) = aX_w^2 + bY_w^2 + cX_w + dY_w + eX_wY_w$$

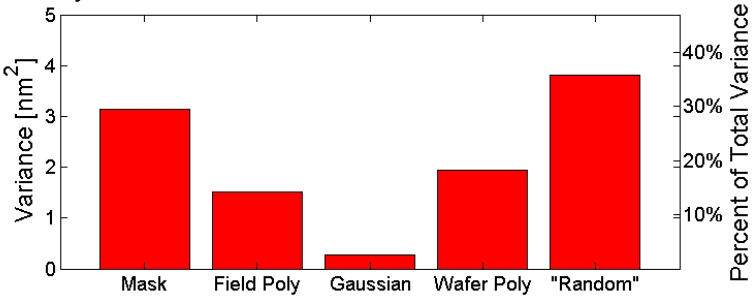
$\sigma^2 = (2.39\ \text{nm})^2$ $\sigma^2 = (1.39\ \text{nm})^2$ $\sigma^2 = (1.95\ \text{nm})^2$



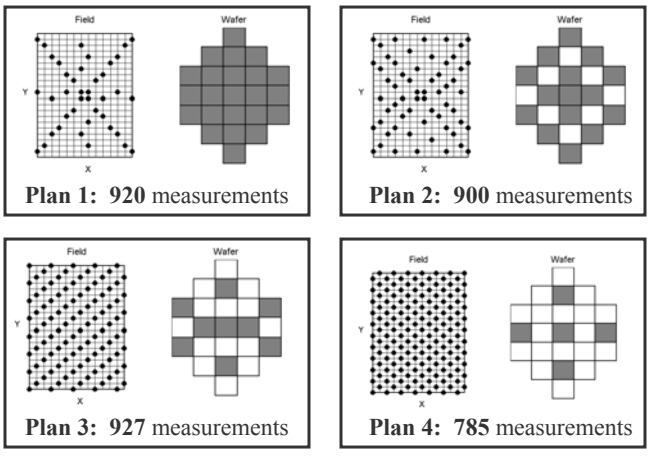
Across-Wafer Systematic Variation with bivariate Gaussian removed **Polynomial Model** **Remaining Across-Wafer Systematic Variation**

Systematic Variation Model Summary

- Across-field systematic variation:
  - Mask errors (magnified scaling factor) removed
  - Polynomial terms in X and Y across the field
- Across-wafer systematic variation:
  - Across-field systematic variation removed
  - Bivariate Gaussian for spot effect (likely linked to develop effect)
  - Polynomial terms in X and Y across the wafer

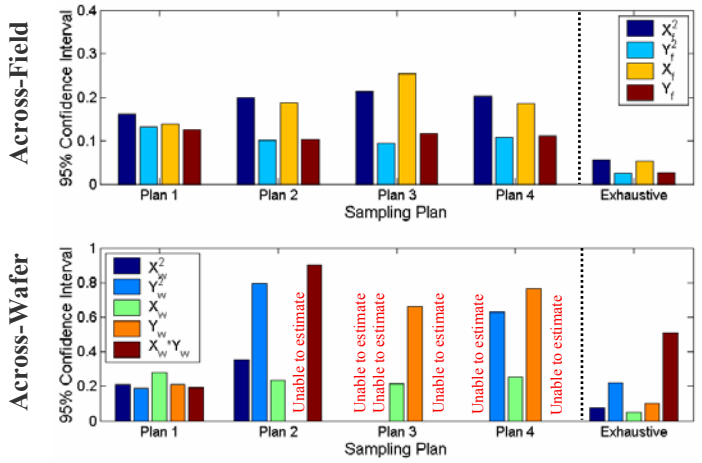


Reduced Sampling Plan Candidates



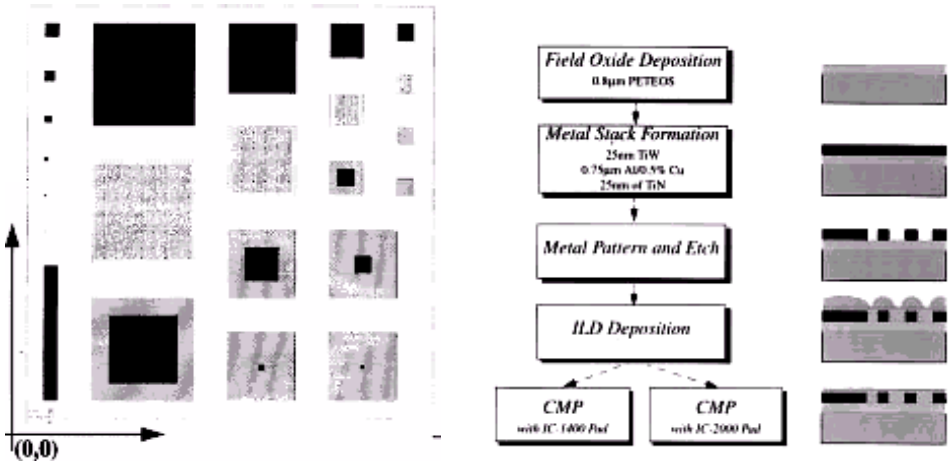
Each plan requires roughly one hour of measurement time
(Exhaustive plan had 21,252 measurements, requiring 25 hours)

Comparison of Reduced Sampling Plans



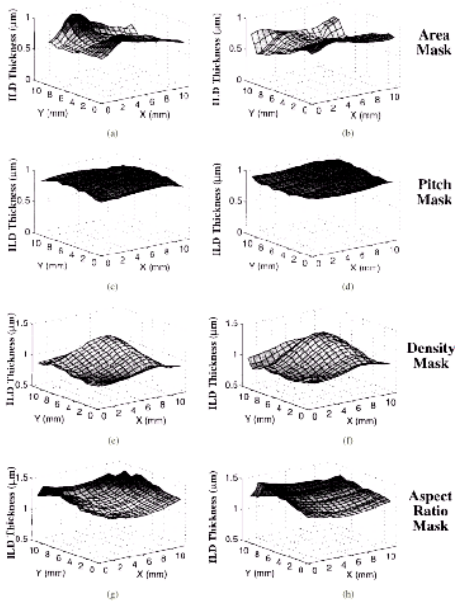
Plan 1 offers the best estimate of across-wafer variation without compromising the quality of the across-field estimate.

Statistical Metrology for Dielectrics



Rapid Characterization and Modeling of Pattern-Dependent Variation in Chemical-Mechanical Polishing
Brian E. Stine, Dennis O. Ouma, *Member, IEEE,* Rajesh R. Divecha, *Member, IEEE,* Duane S. Boning, *Member, IEEE,* James E. Chung, *Member, IEEE,* Dale L. Hetherington, *Member, IEEE,* C. Randy Harwood, O. Samuel Nakagawa, and Soo-Young Oh, *Member, IEEE,* IEEE TSM, VOL. 11, NO. 1, FEBRUARY 1998

Dielectric Thickness vs Position in Field



Studies like this can be used to complement “random” variability with the deterministic, pattern dependent variability.

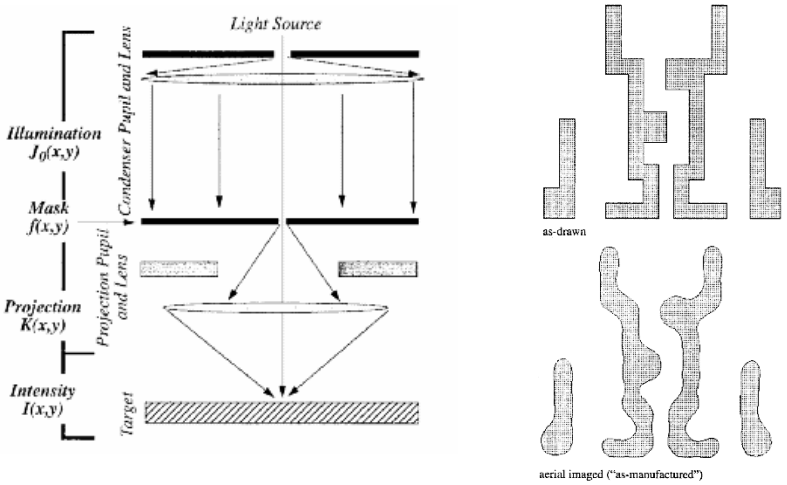
The combination of the two leads to simulation tools that can predict very well the “spread” of circuit performances.

Impact of Process Variability to Circuit Performance

- Obviously, not everything in the process impacts the Circuit Performance.
- Studies have tried to focus on the most important process parameters.
- CD is clearly one of them.

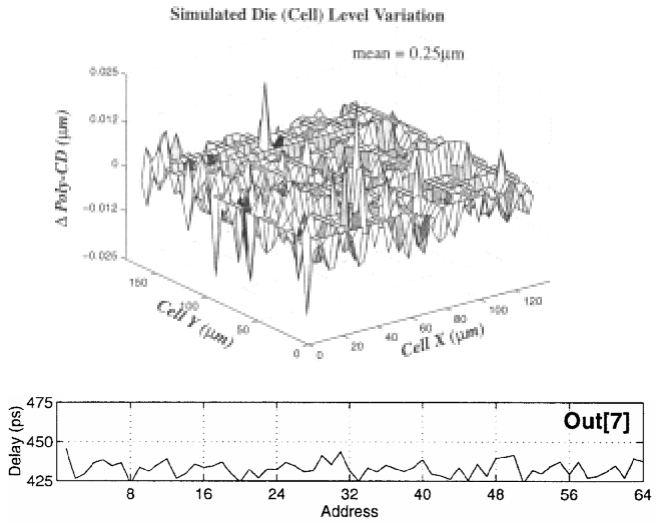
Impact of Pattern-Dependent Poly-CD Variation

Use basic Optical Model to determine “actual” pattern...



Simulating the Impact of Pattern-Dependent Poly-CD Variation on Circuit Performance, Stine, et al, IEEE TSM, Vol 11, No 4, November 1998

Simulated Performance Variability in 64x8 SRAM Macrocell



Circuit Sensitivity to Interconnect Variation

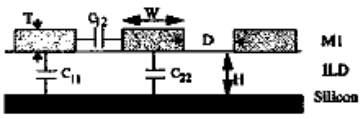


Fig. 1. Cross section of an interconnect structure.

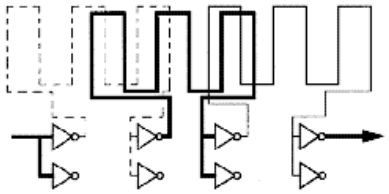


Fig. 6. Circuit diagram of a ring oscillator.

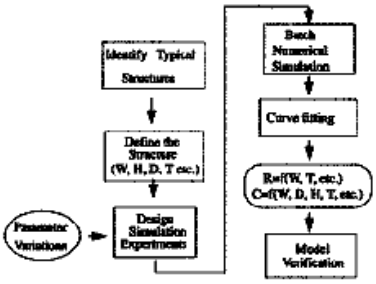
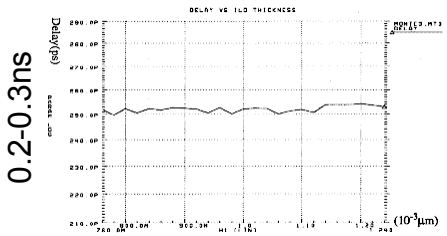


Fig. 2. Interconnect modeling flow.

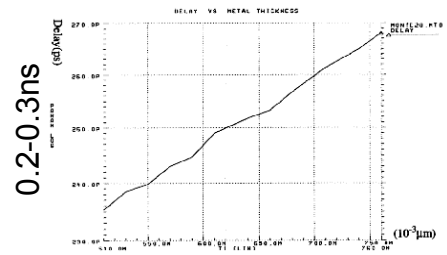
Circuit Sensitivity to Interconnect Variation, Lin, Spanos and Milor, IEEE TSM, Vol 11, No 4, November 1998

Sample Sensitivities to Interconnect



0.2-0.3ns

ILD Thickness



0.2-0.3ns

Metal Thickness!

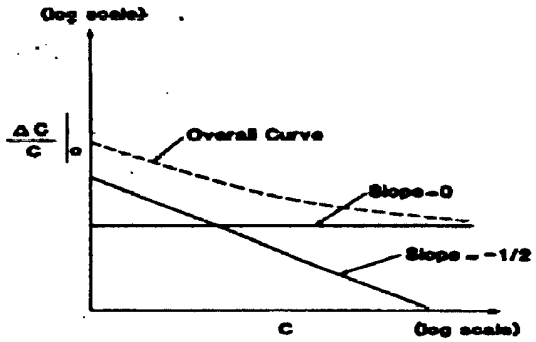
0.8 - 1.2µm

Modeling Spatial Matching

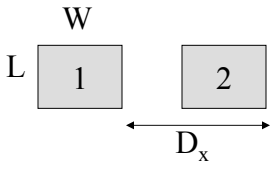
- Component Matching is an aspect of process variability that affects the yield of Analog Circuits:
  - D-A converters: capacitor matching.
  - Diff amplifiers, current sources: transistor matching.

Circuit Element "Matching" Models

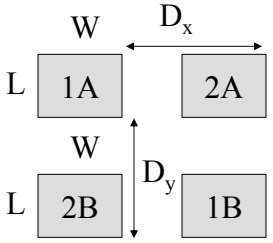
- In order to describe matching one needs a "spatial" distribution.
- In this case *location*, as well as *distance* are factors that will affect process (and performance) variability.
- Several models have been created, either empirically, or by taking into account detailed device parameters.



Pelgrom's Model



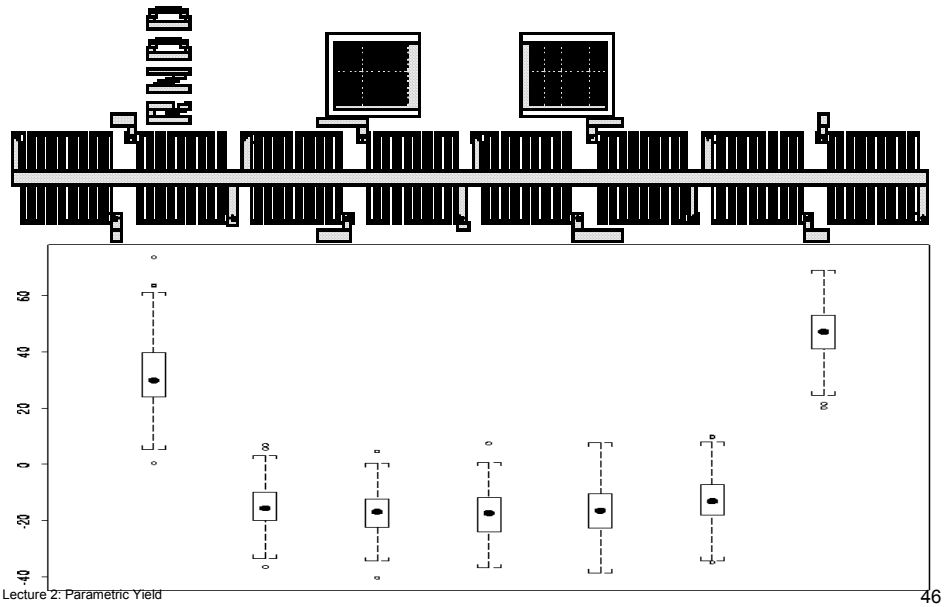
$$\sigma^2(\Delta P) = A^2_p/WL + S^2_p D^2_x$$



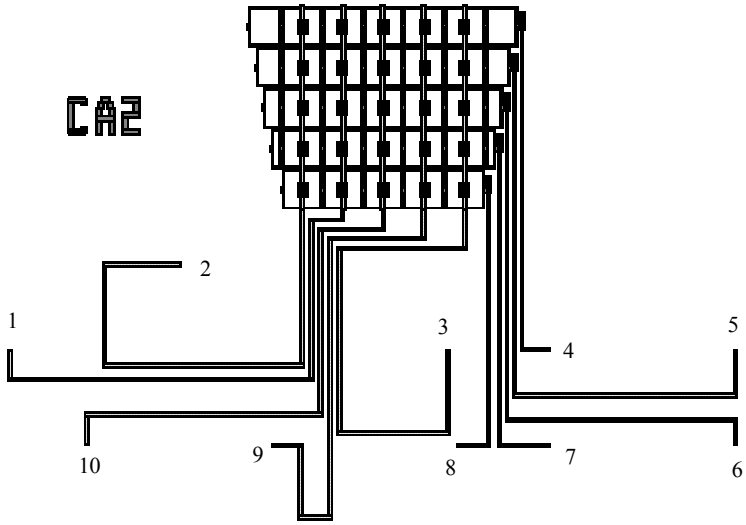
$$\sigma^2(\Delta P) = A^2_p/2WL + S^2_p D^2_x D^2_y/\text{wafer diameter}$$

Variance inversely proportional to area, proportional to distance^2.

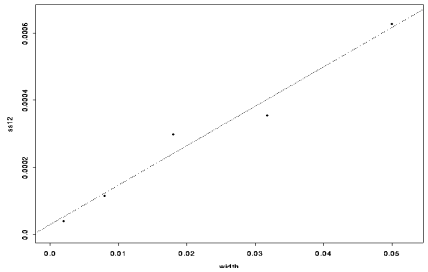
Example - Resistance Variance vs. Pattern



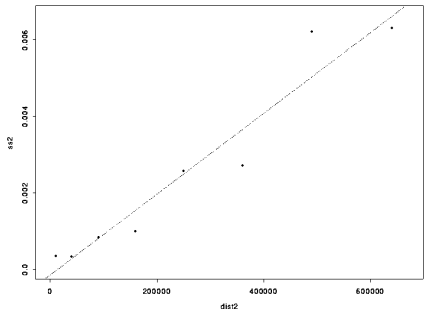
Example on Variance in Element Array



Example of Variance vs. size, distance



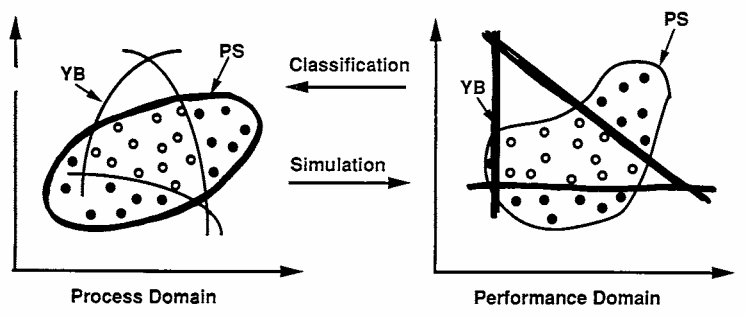
$\sigma^2_{\Delta R/R}$ vs $1/L$



$\sigma^2_{\Delta R/R}$ vs D^2

Simulating Parametric Yield

- The process domain can be mapped to the performance domain through random exploration.
- The Yield can then be estimated as Y= Np/N.
- Though this estimate converges rather slowly, it does have some nice properties.



Monte Carlo - the speed of Convergence

• Since Y is an estimate of a random variable, bounds for the actual value of Y are given by the general Tchebycheff inequality:

$$P\{|Y_{est}-Y| > k\sigma\} < 1/k^2$$

• Since each random experiment can be seen as a Bernoulli trial with Y probability of success, then if N is large and Y(1-Y)N>6 (or so), we can employ the approximation:

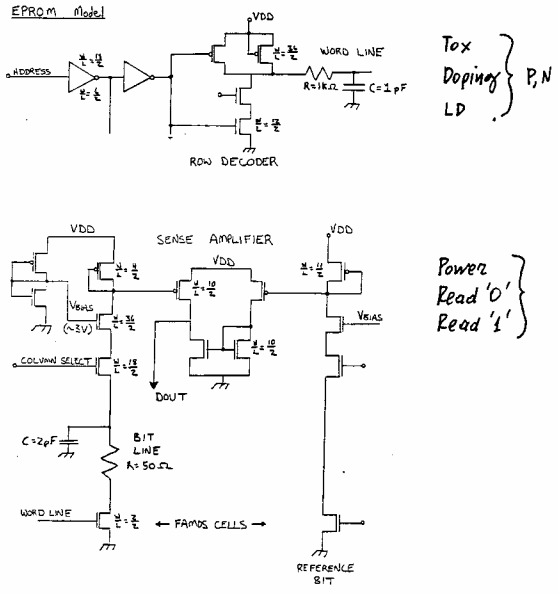
$$\mu_Y = Y$$

$$\sigma^2_Y = Y(1-Y)/N$$

• The estimation accuracy is <u>independent of the dimensionality of the process domain</u>.

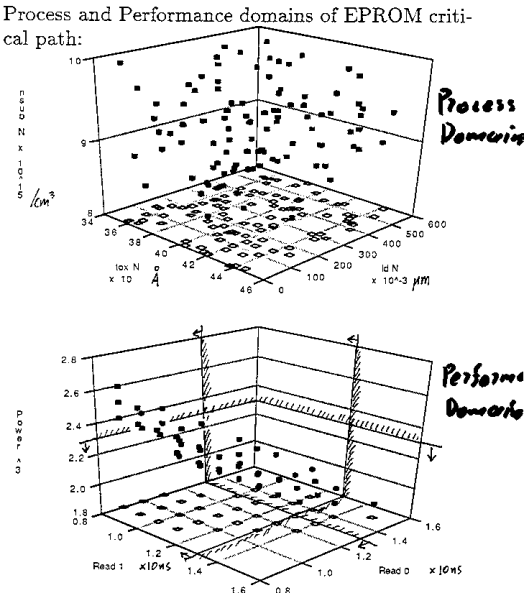
definitions: Y: actual yield, N: number of Monte Carlo trials, μ_Y, σ^2_Y are the mean and variance of the estimated yield Y_{est}.

An Example - EPROM Sense Amp



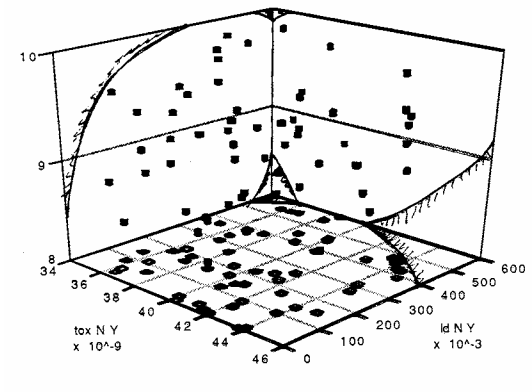
The two Domains for the Sense Amp

Process and Performance domains of EPROM critical path:



Yield Simulation Example

$N = 100$, $Np = 59$
$Y = 0.59$, $\sigma^2_y = Y(1-Y)/N = 0.05^2$
$Y = 0.59 +/- 0.15 \Rightarrow \underline{0.44 < Y < 0.74}$



Next Time on Parametric Yield

- Current and Advanced DFM techniques
  - The role of process simulation (TCAD)
  - Complete Process Characterization
  - Worst Case Files
  - Statistical Design
- The economics of DFM