ANNOUNCEMENTS

- **Final Exam:**
  - **When: Wednesday 12/10 12:30-3:30PM**
  - **Where: 10 Evans (last names beginning A-R)**
    60 Evans (last names beginning S-Z)
  - **Comprehensive coverage of course material**
  - **Closed book; 3 sheets of notes & calculator allowed**
- **For Chunlong's students (Lab Sections 17 & 20):**
  - **Section 17 (Wed 3-6 PM) students should attend an alternate section, to have their Tutebots checked off before Thu. 8 PM**
  - **Students in Lab Sections 17 & 20 (Wed 3-6 PM & Thu 5-8 PM) can receive their deposit checks back next week.**
- **Prof. King's Office Hours tomorrow: 1-5 PM, 476 Cory**

Final Exam Topics

1. **Circuit analysis**
2. **Equivalent circuits**
3. **Op-amp circuits**
4. **First-order circuits / transient response**
5. **Semiconductor properties, pn diodes**
6. **MOSFET devices and circuits**
7. **Logic circuits (including delay analysis)**
8. **CMOS process & layout**

Microelectronics Technology in the 21st Century

Outline

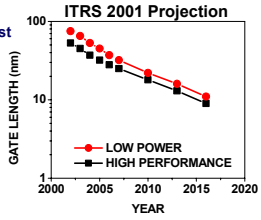
- Introduction
- Scaling Si Transistors to the Limit
- Beyond Scaling
- Conclusion

Reference Reading

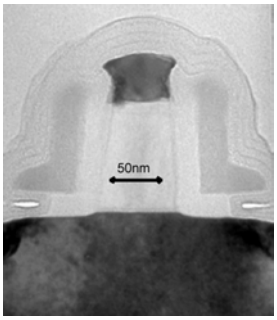
Rabaey *et al.*: Section 2.5.2

IC Technology Advancement

The growth of the semiconductor industry has been tied to transistor scaling



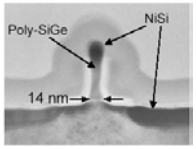
Intel's 90 nm CMOS Technology



Used for volume manufacturing of ICs on 300 mm wafers beginning 4Q03

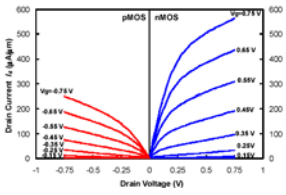
- L_g = 50 nm
- T_{ox} = 1.2 nm
- Strained Si channel

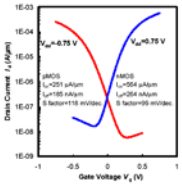
14 nm CMOS Transistors



Hokazono *et al.*, Toshiba Corporation, presented at the *International Electron Devices Meeting* (San Francisco, CA) Dec. '02

- 1.3 nm SiO_xN_y gate dielectric
- Poly-$Si_{0.9}Ge_{0.1}$ gate



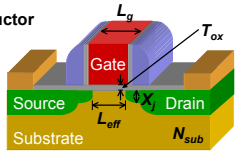


Bulk-Si MOSFET Scaling

- Leakage current is the main challenge to scaling
- To suppress leakage, we need to employ:
  - Higher body doping → lower carrier mobility, higher junction capacitance, increased junction leakage
  - Thinner gate dielectric → higher gate leakage
  - Ultra-shallow S/D junctions → higher R_{series}

Metal-Oxide-Semiconductor Field-Effect Transistor:

Desired characteristics:
- High ON current (I_{dsat})
- Low OFF current



Outline

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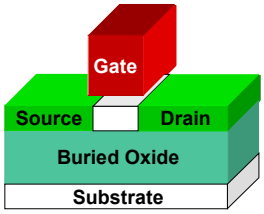
Advanced MOSFET Structures

- Must control leakage in order to scale down L_g
- Most of the leakage occurs far from the SiO_2 interface

  Let's get rid of it!

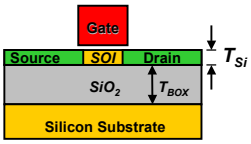
Thin-Body MOSFET



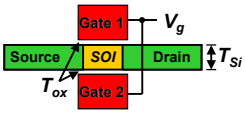
SOI Wafer

Thin-Body MOSFETs

Ultra-Thin Body



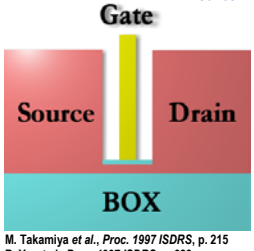
Double Gate



Common feature: A thin body, such that no conduction path is far from the gate

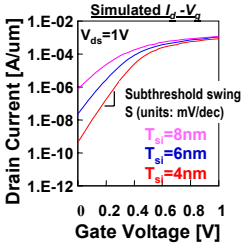
Ultra-Thin-Body MOSFET

- UTB suppresses leakage
- Thick S/D => low R_{series}

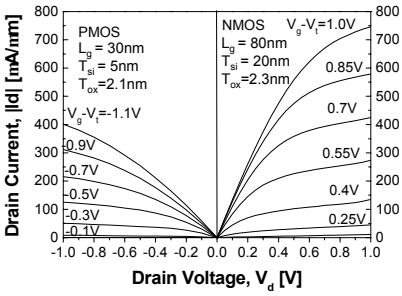


M. Takamiya *et al.*, *Proc. 1997 ISDRS*, p. 215
B. Yu *et al.*, *Proc. 1997 ISDRS*, p. 623

- L_g = 12 nm
- T_{ox} = 2 nm



Measured UTB MOSFET I_d-V_d



Good I_{dsat} achieved with thick S/D structure

Y.-K. Choi *et al.*, *IEDM* 1999

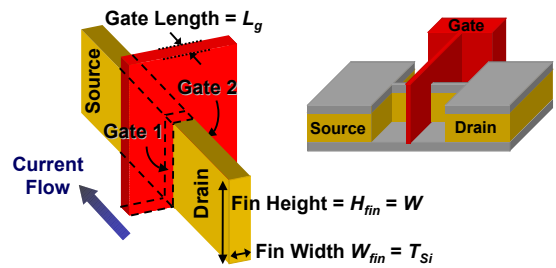
UTB MOSFET Scaling

- **Issues for bulk-Si MOSFET scaling obviated**
  - Body does not need to be heavily doped
  - T_{ox} does not need to be scaled as aggressively
  - Ultra-shallow S/D junction formation is not an issue
- **Body thickness must be less than ~1/3 x L_g**
  - Formation of uniformly thin body is primary challenge
  - For T_{Si} < 4 nm, quantum confinement & interface roughness → V_T variation and degraded g_m

K. Uchida *et al.*, *IEDM* 2002

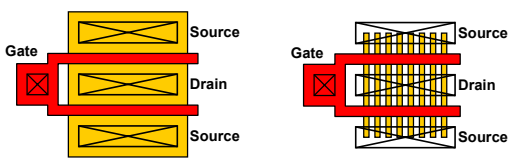
Double-Gate "FinFET"

- **Self-aligned gates straddle thin silicon fin**
- **Current flows parallel to wafer surface**



FinFET Layout

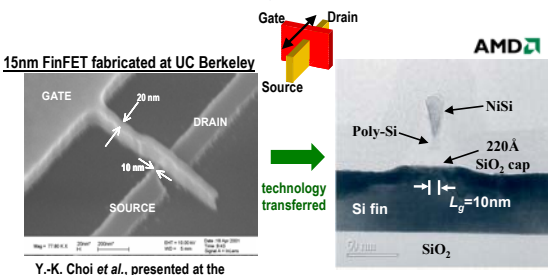
- **Layout is similar to that of conventional MOSFET**



Bulk-Si MOSFET FinFET

Scaling L_g to 10 nm

15nm FinFET fabricated at UC Berkeley



Y.-K. Choi *et al.*, presented at the *2001 Int'l Electron Devices Meeting*

B. Yu *et al.*, presented at the *2002 Int'l Electron Devices Meeting*

CMOS FinFETs fabricated using standard tools at AMD
(optical lithography plus photoresist trimming)

10 nm L_g FinFET I_d-V_d

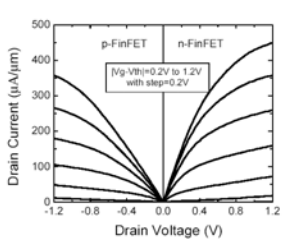


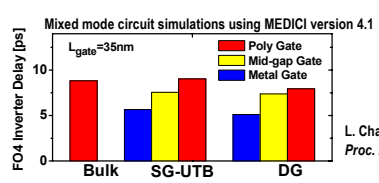
Fig.5 Id-Vd characteristics of 10nm gate length CMOS FinFET transistors.

B. Yu *et al.*, *IEDM Technical Digest*, pp. 251-254, 2002

AMD

Circuit Performance Comparison

- **No channel doping is needed in thin-body FETs**
  → higher I_{dsat} achieved, dopant fluctuation effects avoided

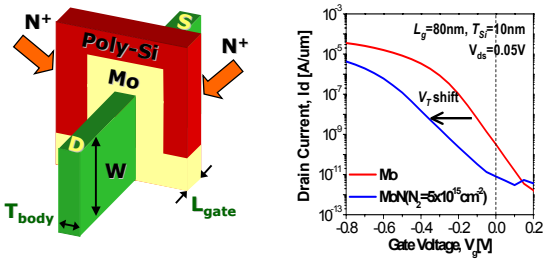


L. Chang *et al.*, *Proc. IEEE* 91 (2003)

V_T must be adjusted by gate work function engineering

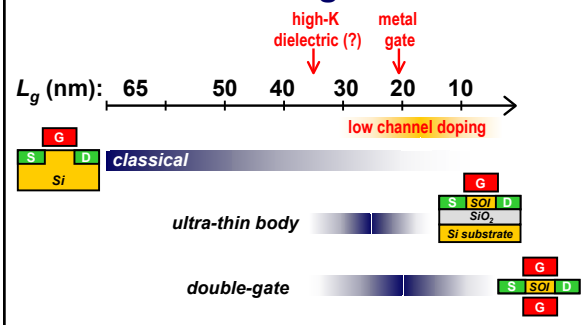
Molybdenum-Gated FinFETs

Y.-K. Choi *et al.*, 2002 IEDM



- Tilted N implantation (60°) used for sidewall gates
- ✓ N implantation lowers gate work function

MOSFET Scaling to the Limit



Outline

- Introduction
- Scaling Si Transistors to the Limit
- **Beyond Scaling**
- Conclusion

IC Technology Challenges

- **Limits to transistor scaling exist**
- **Power is an issue of increasing importance**
  - Portable & wireless-communication products require high speed, low cost & very low power

→ **Alternative approaches are needed**
- innovative circuit & system designs
- novel semiconductor devices that enable more efficient circuit designs
- **heterogeneous integration**

Heterogeneous Integration

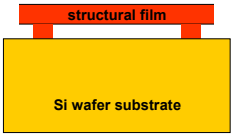
→ **Enhanced functionality/value of IC products**

Example: Integrated Micro-ElectroMechanical Devices

- **low-power, wireless building blocks**
  - **MEMS antennas, microswitches, filters**
- **cooler microprocessors**
  - **micropumps, valves, and channels for cooling**
- **smart sensors**
  - **environmental monitoring**
    - improved energy efficiency, emergency response, contamination detection…
- **bio chips**
  - **microfluidics**
    - biochemical sensors, DNA analysis chips, drug delivery

MEMS Technology

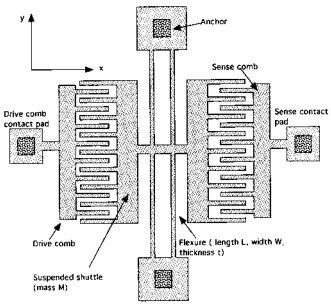
Surface Micromachining
(cross-sectional view)



- Mechanical structures can be made using conventional microfabrication techniques
- Structures are freed by selective removal of sacrificial layer(s)

- Polycrystalline silicon is the preferred structural material
  - ✓ as strong as steel
  - ✓ resists fatigue
  - -- requires high annealing temperatures (≥900°C)

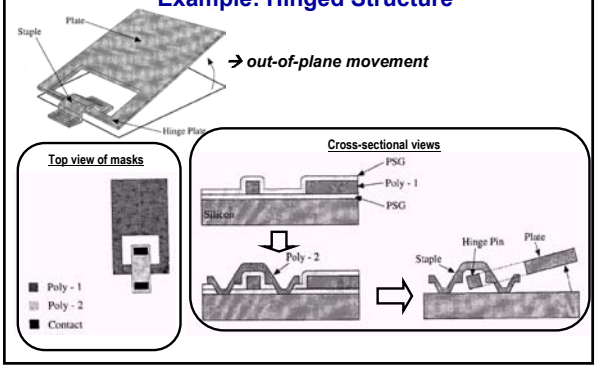
Surface Micromachined Resonator



- **Electrostatic force is applied by a comb drive electrode to a suspended shuttle.**
- **Motion is detected capacitively by a sense comb electrode.**

Benefit of Multiple Structural Layers

Example: Hinged Structure



Micromachines

Examples of MEMS Products

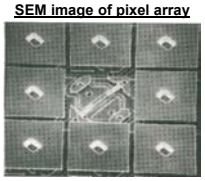
- **Chemical and pressure sensors**
- **Inertial sensors**
  - accelerometers and gyroscopes
- **Optical modulators**
  - micro-mirrors for communications, projection displays

DMD™ Projection Display Chip

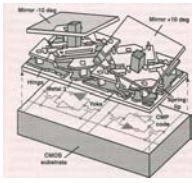
Texas Instruments Inc.

- Mirrors are made using metal layers (Al, alloys)
  - sacrificial material is photoresist

SEM image of pixel array



Schematic of 2 pixels

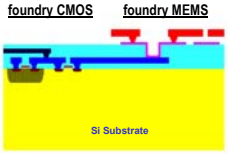


Each mirror corresponds to a single pixel, programmed by an underlying memory cell to deflect light either into a projection lens or a light absorber.

Integrated MEMS Technology

For low cost & high performance, we want:

- **Low thermal process budget**
  → can use semiconductor foundry for electronics, then add MEMS in a modular fashion
- **Capabilities similar to poly-Si MEMS**
  → can leverage MEMS foundry processes, and MEMS industry design experience



Enter Silicon-Germanium…

- **SiGe can be processed at significantly lower process temperatures than Si** (≤ 450°C)
  - Conventional process tools are used for deposition and patterning

III	IV	V
B	C	N
Al	Si	P
Ga	Ge	As

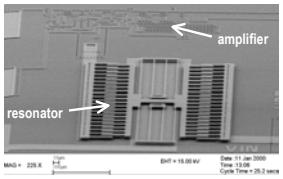
- **Properties are similar to those of Si, and can be tailored by adjusting Ge content**
- **The IC industry has significant experience with SiGe**

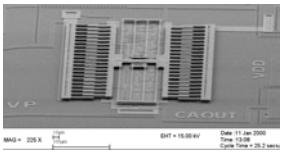
SiGe iMEMS Demonstration

High-performance MEMS can be fabricated directly on top of conventional CMOS circuits, using silicon-germanium for the structural layers

Resonator next to Amplifier
- conventional layout of integrated MEMS

Resonator on top of Amplifier
- smaller area --> lower cost
- reduced interconnect parasitics --> improved performance

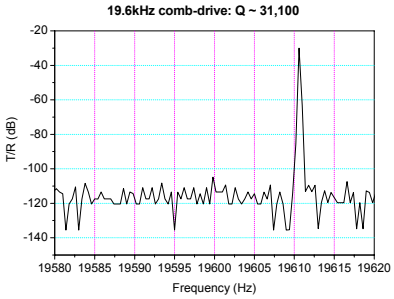




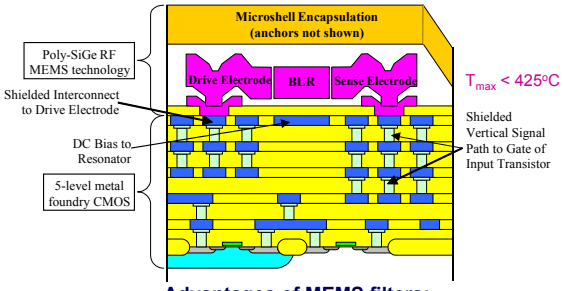
A. E. Franke *et al.*, *Solid-State Sensor and Actuator Workshop Technical Digest*, pp. 18-21, June 2000

SiGe iMEMS Resonator Response

S. A. Bhave *et al.*, *Solid-State Sensor and Actuator Workshop Technical Digest*, pp. 34-37, 2002



Future Application: RF MEMS



- **Advantages of MEMS filters:**
  - small size, low cost
  - low phase noise, high Q(?)

Outline

- Introduction
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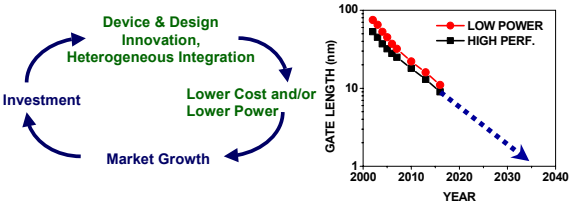
- **Conclusion**

Conclusion

- **Transistor scaling can extend to below 10 nm**
  - advanced structures, materials & processes needed



- **Alternative approaches to scaling will provide improvements in cost, power and/or performance, to sustain the silicon revolution well beyond 30 yrs**