

- HW #5 changes
- HW #6
- Will be up by tonight, 5 problems
- Due next Wednesday (08/06)
- Will be a good review for the midterm
- Return HWs 4 and 5 on Monday (08/04)
- Return HW 3 and corrected HWs 1 and 2 on Friday (08/01)
- Midterm II next Wednesday, 08/06/03!
- Practice problems up by tonight
- Review session?



- CMOS voltage transfer characteristic
- SUGGESTION: Go over lecture 16 STEP-BY-STEP
- Ask questions in discussion and office hours!



- CMOS inverter propogation delay analysis
- Complete our propogation delay model
- Understand MOS capacitances
- Switch-RC model of the CMOS inverter
- Understand τ_{LH} and τ_{HL}
- CMOS layouts and fabrication steps
- Extract capacitances, W and L from layout/crossection
- References: Lectures 18 and 19 (Fall 1999) and Lecture 21 (Spring 2003)

MOSFET Capacitances

Node connected to the gate:



Node connected to the drain (or source):

- pn junction capacitance between drain and bulk is C_{DB}
- capacitance C_{SB} is shorted out since V_S = V_B in digital circuits

The CMOS Inverter



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First Order CMOS Inverter Model

voltages The switches are "ganged" (move together) since they have the same trip

NMOS is closed when $v_{in} > V_{Th}$; PMOS is open **PMOS** is closed when $v_{in} < V_{T}$; **NMOS** is open

Reduce to a single switch (Fig. 2.10, R&R)



"Cascaded" CMOS Inverters

What's connected to the v_{out} node?

Representative "load" ... possibly another CMOS inverter



Cascaded Identical CMOS Inverter Circuit Model



Simpler Representation

inverter operate in a complementary fashion ightarrow reduce to a single switch per NMOS and PMOS transistors have the same logic thresholds, but



Transitions of interest:

previous "U" position 1. v_{int} increases above V_{Th} : switch for inverter 1 moves to "D" position from

2. v_{int} decreases below V_{TI} : switch for inverter 1 moves to "U" position from previous "D" position



Output Propagation Delay High to Low Version Date 04/03/03



When V_{IN} goes High V_{OUT} starts decreases with time

downstream gate to begin to switch is $V_{DD}/2$ or 2.5V. Assume that the necessary voltage swing to cause the next

high to low is the time to go from $V_{DD} = 5V$ to to $V_{DD}/2 = 2.5V$ That is the propagation delay τ_{HL} for the output to go from

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Output Propagation Delay High to Low (Cont.) Version Date 04/03/03



When $V_{OUT} > V_{OUT-SAT-D}$ the available current is $I_{OUT-SAT-D}$

is constant at I_{OUT-SAT-D} and the capacitor discharges. For this circuit when V_{OUT} > V_{OUT-SAT-D} the available current

The propagation delay is thus

$$\Delta t = \frac{C_{OUT} \Delta V}{I_{OUT-SAT-D}} = \frac{C_{OUT} V_{DD}}{2I_{OUT-SAT-D}} = \frac{50 \, fF \cdot 2.5V}{100 \, \mu A} = 1.25 \, ns$$

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Switched Equivalent Resistance Model

The above model assumes the device is an ideal constant current source.

1) This is not true below V_{OUT-SAT-D} and leads to in accuracies.

and parallel connections is problematic. 2) Combining ideal current sources in networks with series

equal to the Δt found above Instead define an equivalent resistance for the device by setting $0.69 R_p C$

gives
$$\Delta t = \frac{C_{OUT} V_{DD}}{2I_{OUT-SAT-D}} = 0.69 R_D C_{OUT}$$

This

$$R_D = \frac{V_{DD}}{2 \cdot (0.69) I_{OUT-SAT-D}} \approx \frac{3}{4} \frac{V_{DD}}{I_{OUT-SAT-D}} = \frac{3}{4} \frac{5V}{100 \mu A} = 37.5 k\Omega$$

Each device can now be replaced by this equivalent resistor.

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 $\frac{3}{4}$ V_{DD} is the average value of V_{OUT}

from (0,0) to ($I_{OUT-SAT-D}$, ${}^{3}\!\!/_{4} V_{DD}$). Approximate the NMOS device curve by a straight line

Interpret the straight line as a resistor with

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 $1/(\text{slope}) = R = \frac{3}{4} V_{\text{DD}}/I_{\text{SAT}}$

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Switched Equivalent Resistance Values

geometrical layout, design style and technology node. The resistor values depend on the properties of silicon,

higher than p-type. n-type silicon has a carrier mobility that is 2 to 3 times

width/length in the geometrical layout. The resistance is inversely proportion to the gate

predetermined fixed size Design styles may restrict all NMOS and PMOS to be of a

inversely with the linewidth. The current per unit width of the gate increases nearly

For convenience in EE 42 we assume $R_{D} = R_{U} = 10 \text{ k}\Omega$



CMOS

Challenge: build both NMOS and PMOS on a single silicon chip

NMOS needs a p-type substrate

PMOS needs an n-type substrate

Requires extra process steps



Additional Steps for CMOS

Well Formation



Process (before transistor fabrication)

- 1. start with p-type wafer; grow 250 nm oxide
- 2. pattern oxide with n-well mask
- 3. implant with phosphorus and anneal to form a 3 µm-deep n-type region

 \neg



AND ONE MORE COMPLICATION:

We need contacts to "body" or well and body of p-region

Easy to do – just modify "select" masks and oxide masks, i.e.,

① Create thin oxide spots for contact in original oxide mask, and

②Allow openings in select masks to dope these regions



p implant area in substrate is to make electrical contact by Al wire easier

How to get n-regions implanted selectively with arsenic?

Could simply invert polarity of select mask at contacts.

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Basic CMOS Process

Well mask + select mask(s) + NMOS process

W Oldham

Separate Masks

Well, oxide, and polysilicon masks





Separate Masks (cont.)

Select masks, contact mask, and metal mask

W Oldham

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CMOS Process Sequence

- 1. p-type starting material; grow 500 nm of oxide
- 2. pattern oxide with well mask
- 3. implant phosphorus and anneal ("well drive in") to a depth of 3 μm
- 4. strip off oxide
- 5. grow 500 nm of oxide
- 6. pattern with oxide mask
- 7. grow 5 nm of oxide
- 8. deposit 500 nm of n+ polysilicon
- 9. pattern with poly mask
- 10. spin on resist
- 11. pattern with the select mask (dark field)
- 12. implant boron; strip off resist
- 13. spin on resist
- 14. pattern with the select mask (clear field)

Same pattern except for well and substrate contacts

CMOS Process Sequence (cont.)

- 15. implant arsenic; strip off resist and anneal implants to form source and drain regions
- 16. deposit 500 nm of oxide
- 17. pattern using contact mask (dark field)
- 18. deposit 1 μm of aluminum
- 19. pattern using metal mask (clear field)

CMOS Cross Sections





- Completed our propogation delay model
- Switch-RC model of the CMOS inverter
- τ_{LH} and τ_{HL} calculations
- CMOS layouts and fabrication steps
- References: Lectures 18 and 19 (Fall 1999) and Lecture 21 (Spring 2003)



- Barring unforseen circumstances: GUEST LECTURE BY PROF. TSU JAE-KING
- HW #5 due!
- START PREPARING FOR MIDTERM!