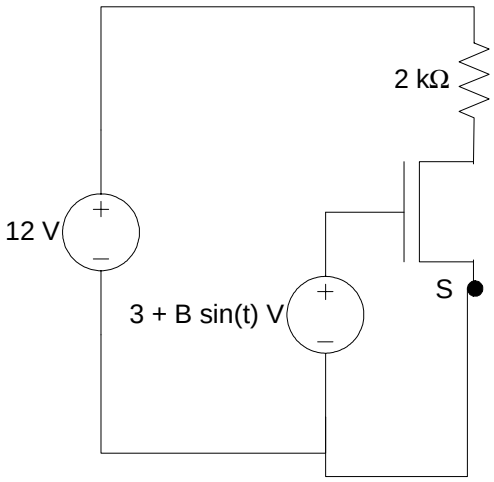
EE 40

Homework # 7

Due Tuesday, May 13, 2003 in class or in drop box by 3:30 PM

40 Total Points Possible

Problem 1: 10 Points Possible



For the following, let $(W/L)\mu_N C_{OX} = 2$ mA/V^2 and $V_{TH(N)} = 1$ V; ignore λ.

a) Let B = 0.3. Using the small-signal model, find the range of variation in the resistor voltage.

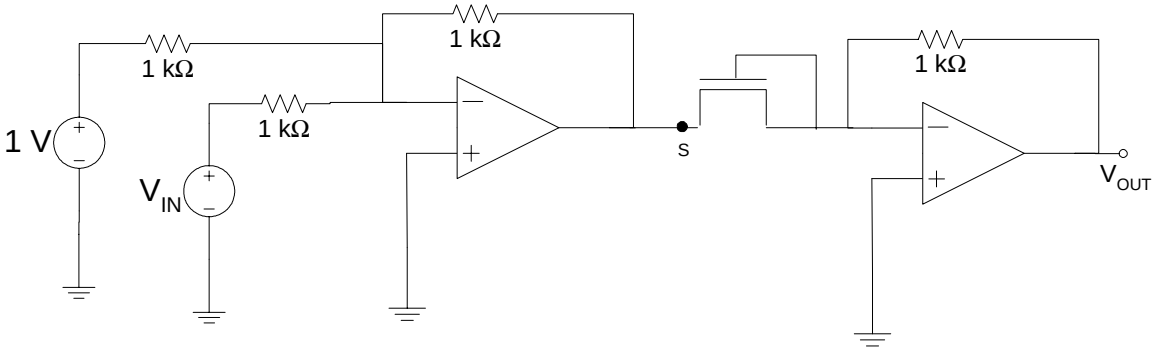
b) Find the gain: the magnitude of variation in the resistor voltage divided by the magnitude of variation of V_{GS}. You can use part a) values.

c) Write an equation for the resistor voltage as a function of time.

d) What is the maximum value of B allowed if the transistor is to remain in saturation mode?

Problem 2: 10 Points Possible

Find V_{OUT} for the circuit below, ignoring the effect of the rails.
Assume $V_{IN} > 0$ V. Use $(W/L)\mu_N C_{OX} = 2$ mA/V^2 and $V_{TH(N)} = 1$ V; ignore λ.



Problem 3: 10 Points Possible

Design a circuit with inputs A and B and output F, which performs the following function:

F = A B if control voltages C_1 C_0 = 0 0 or C_1 C_0 = 0 1
F = A + B if control voltages C_1 C_0 = 1 0
F = A $\oplus$ B if control voltages C_1 C_0 = 1 1

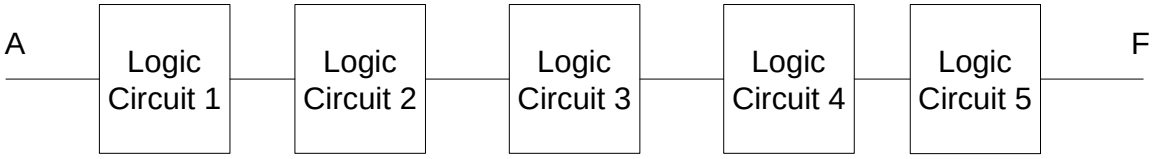
You may use regular logic gates, or a multiplexer.

Problem 4: 10 Points Possible

Consider the circuit below, where each logic circuit box has a propagation delay of 2 ns.

a) Calculate the total propagation delay that a logic signal will experience from the input A to the output F.

b) Suppose that a correct output F must be maintained for at least 1 ns before a new value can be put on the input to perform another computation. Calculate the number of computations that can be performed in one second. One computation means one input traveling all the way through the circuit from A to F, with correct output held for 1 ns.



Consider the pipelined circuit below, where each logic circuit box has a propagation delay of 2 ns and each latch has a propagation delay of 1 ns.

c) Calculate the total propagation delay that a logic signal will experience from the input A to the output F, assuming the clock signal is optimized to leave just enough time to charge the latch capacitances, leading to the propagation delays as stated above.

d) Suppose that a correct output F must be maintained for at least 1 ns before a new value can be put on the input to perform another computation. Calculate the number of computations that can be performed in one second. One computation means one input traveling all the way through the circuit from A to F, with correct output held for 1 ns. Use the pipelined input scheme as demonstrated in Lecture 28.