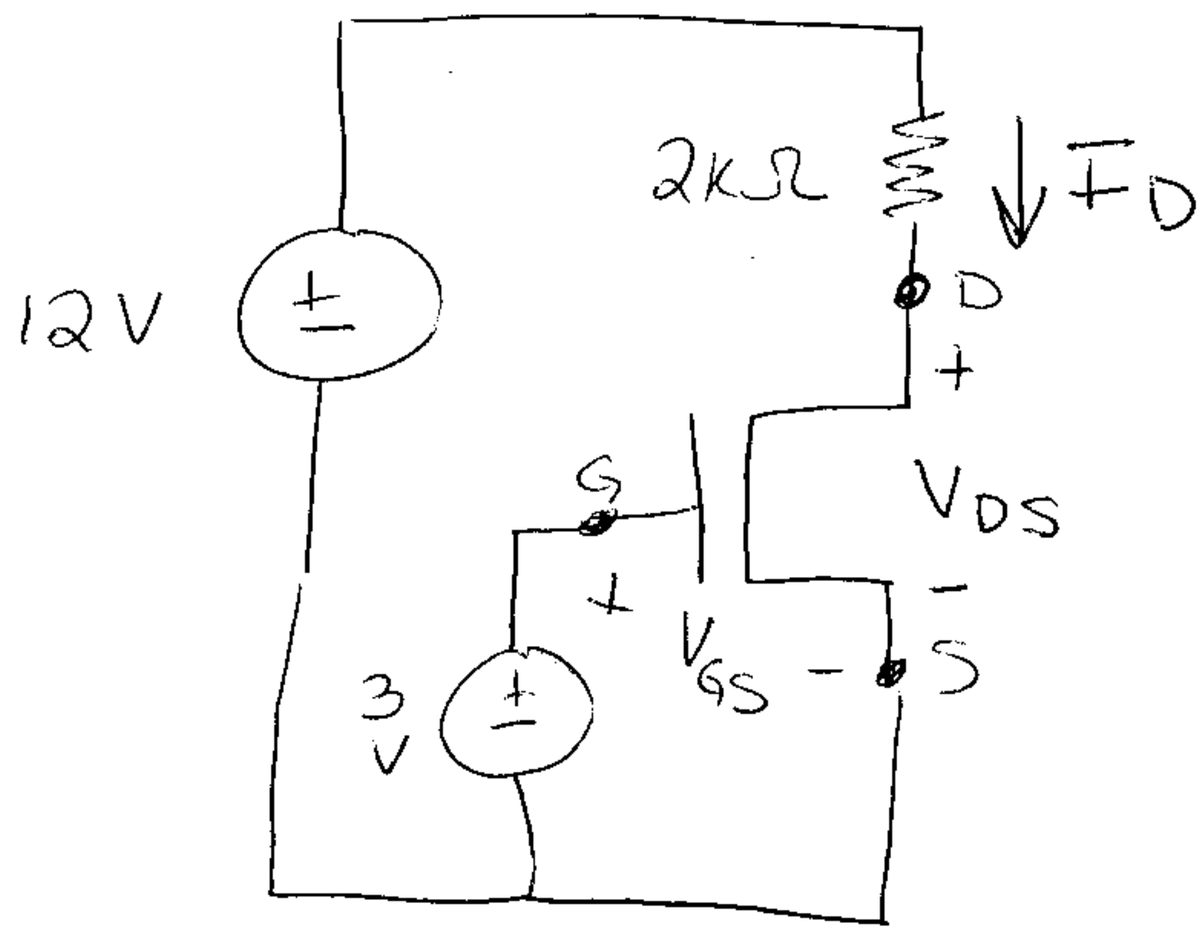
EE 40
Homework 5
Solutions

Problem 1:



$V_{GS} = 3V \Rightarrow$ transistor is <u>not</u> cutoff ($V_{GS} > V_{THN} = 1V$)

Assume saturation (since it is easiest).

$$I_D = I_{DSAT} = \tfrac{1}{2}\frac{W}{L}\mu_n C_{ox}(V_{GS} - V_{THN})^2$$
$$= \tfrac{1}{2}(1mA/V^2)(3V - 1V)^2$$
$$= 2mA$$

$V_{DS} = 12V - 2k\Omega I_D$ (KVL around outside loop)

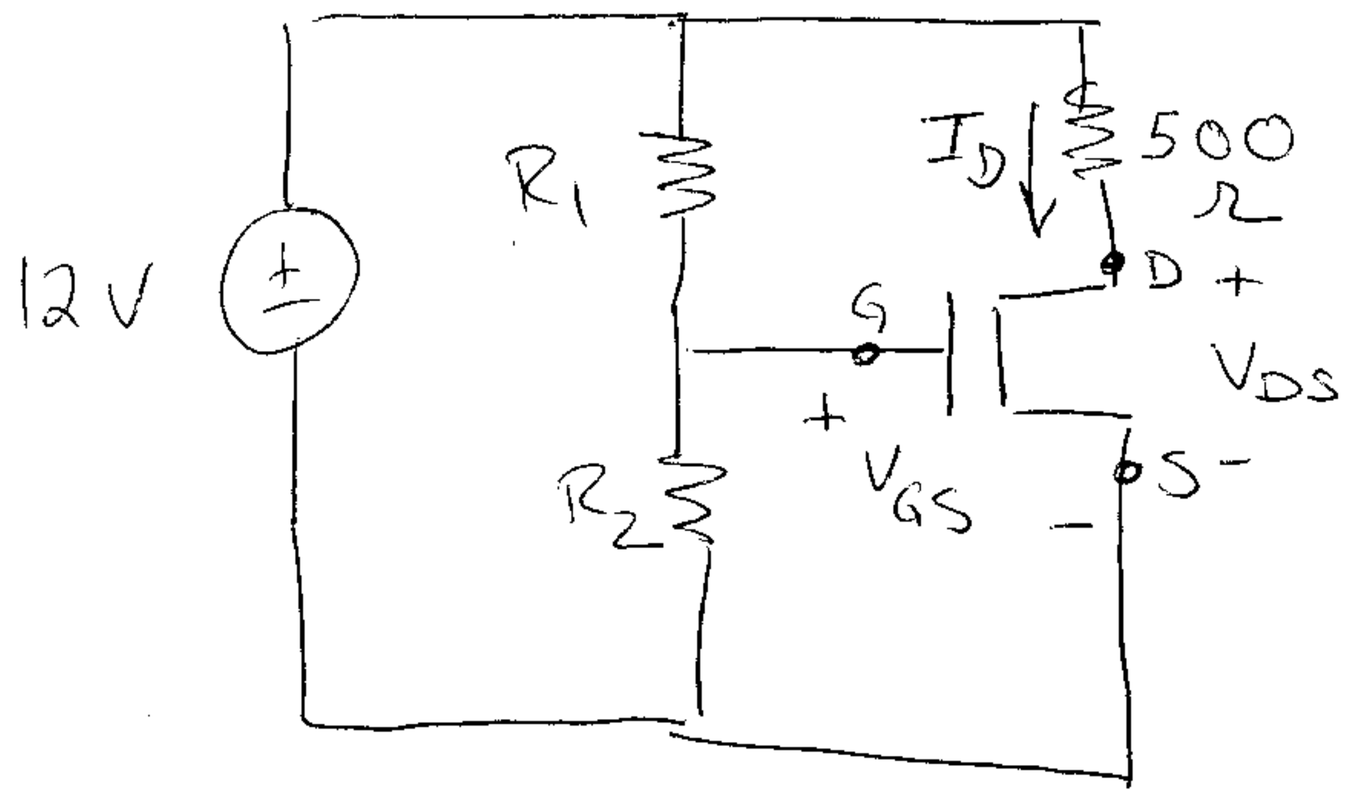
$= 12V - 2k\Omega \cdot 2mA = 8V$

Check that these answers are valid for saturation:

Saturation requires $V_{DS} \geq V_{GS} - V_{THN}$

Indeed $8V \geq 3V - 1V$ So answers are correct.

Problem 2:



Since no current goes into gate, R_1 + R_2 have same current.

$$V_{GS} = \frac{R_2}{R_1+R_2} \cdot 12\,V$$

by voltage division.

Saturation current should be 8mA:

$$8\,mA = I_{DSAT} = \tfrac{1}{2}\frac{W}{L}\mu_n C_{ox}(V_{GS}-V_{TH})^2$$

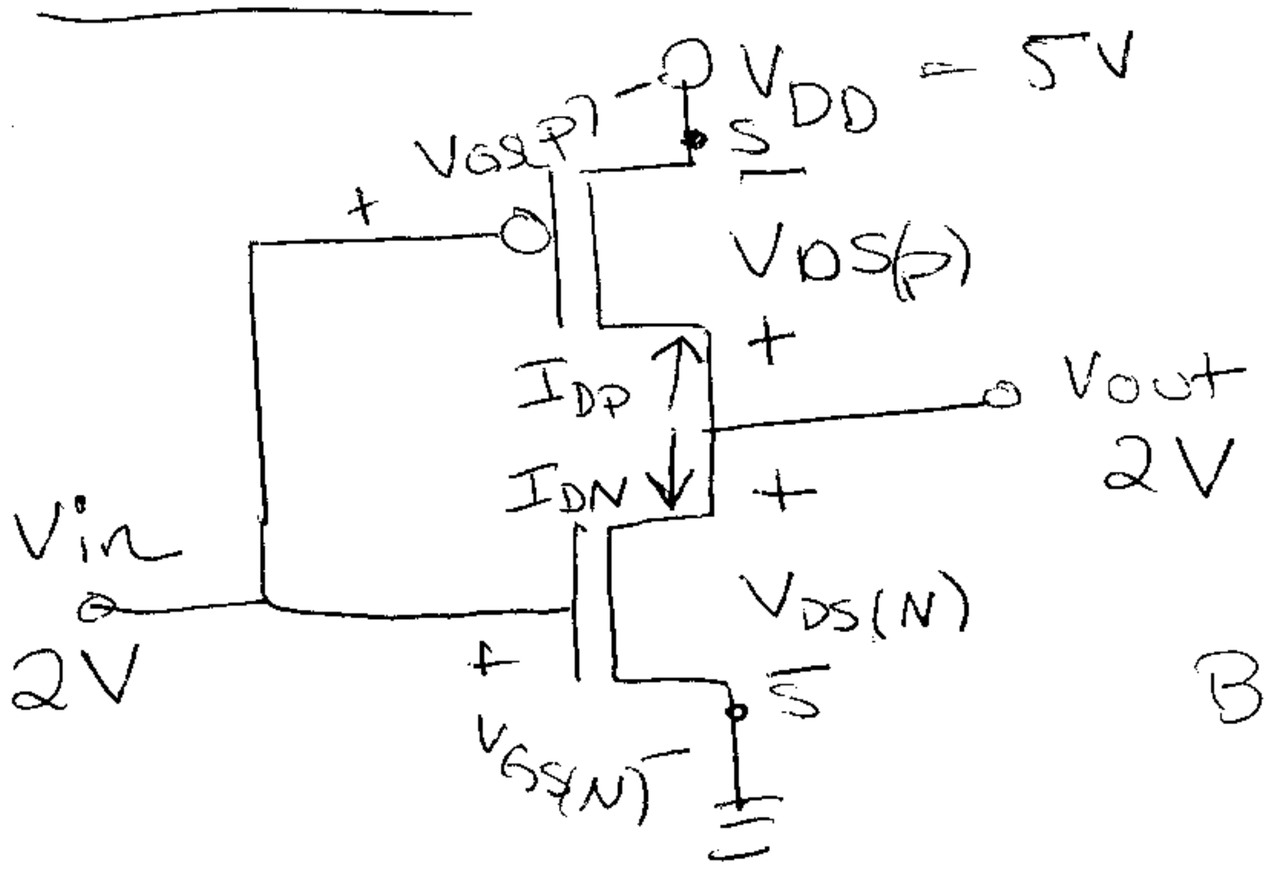
$$= \tfrac{1}{2} \cdot 1\,mA/V^2 (V_{GS} - 1V)^2$$

$$(V_{GS} - 1V)^2 = 16\,V^2 \Rightarrow V_{GS} = 5V$$

$$5V = V_{GS} = \frac{R_2}{R_1+R_2} \cdot 12\,V \Rightarrow \frac{R_2}{R_1+R_2} = \frac{5}{12}$$

Many solutions possible; for example, $R_2 = 5k\Omega$, $R_1 = 7k\Omega$.

Problem 3:



When $V_{IN} = V_{OUT} = 2V$,

$V_{GSP} = V_{DSP} = -3V$

$V_{GSN} = V_{DSN} = 2V$

Both transistors in saturation.

$I_{D(N)} = I_{DSAT(N)}$ $\qquad$ $I_{D(P)} = I_{DSAT(P)}$

By KCL, $I_{D(P)} + I_{D(N)} = 0 \Rightarrow I_{DN} = -I_{DP}$

$$I_{DSAT(N)} = \tfrac{1}{2}\frac{W_N}{L_N}\mu_N C_{ox}(V_{GSN} - V_{THN})^2$$

$$= \tfrac{1}{2}\cdot\frac{1}{2.5\mu m}\cdot W_N \cdot 50000\frac{mm^2}{Vs}\cdot\frac{5fF}{\mu m^2}(2V-1V)^2$$

$$= 50\,W_N$$

$$I_{DSAT(P)} = -\tfrac{1}{2}\frac{W_P}{L_P}\mu_P C_{ox}(V_{GSP} - V_{THP})^2$$

$$= -\tfrac{1}{2}\cdot\frac{1}{2.5\mu m}\cdot W_P \cdot 25000\frac{mm^2}{Vs}\cdot\frac{5fF}{\mu m^2}(-3V - -1V)^2$$

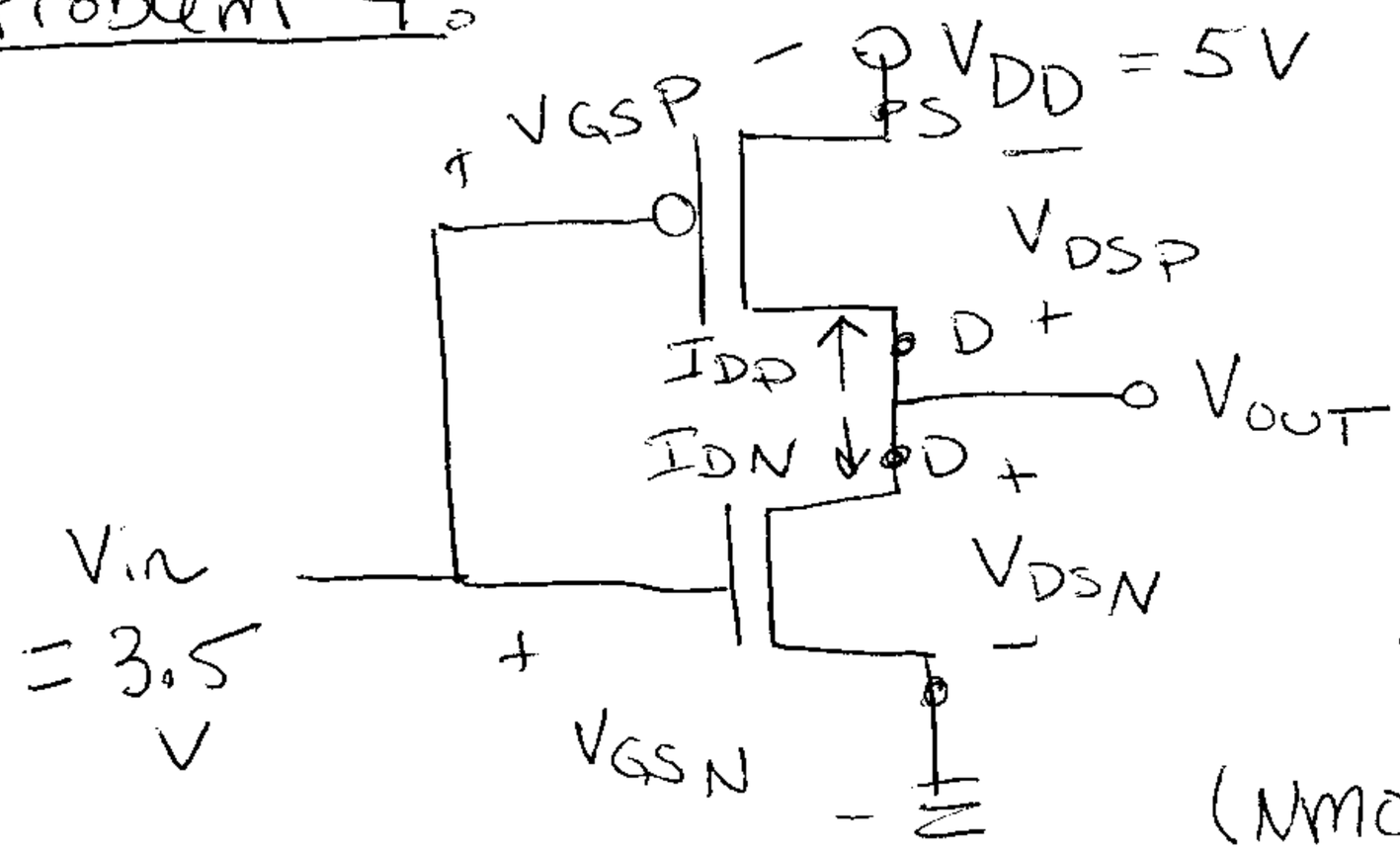
$$= -100\,W_P$$

$I_{D(N)} = -I_{D(P)} \Rightarrow I_{DSATN} = -I_{DSAP} \Rightarrow 50\,W_N = 100\,W_P$

$$\frac{W_N}{W_P} = 2$$

Possible answers: $W_N = 2\mu m$, $W_P = 1\mu m$

Problem 4:



$V_{GS(N)} = 3.5$ V

$V_{GS(P)} = -1.5$ V

Looks like "Region D" (NMOS fully on, PMOS barely on)

∴ Assume PMOS saturation, NMOS triode

$$I_{DP} = I_{DSATP} = -\tfrac{1}{2}\frac{W}{L}\mu_p C_{ox}(V_{GSP} - V_{THP})^2$$

$$= -\tfrac{1}{2} \cdot 1\,mA/V^2(-1.5V - -1V)^2$$

$$I_{DP} = -125\,\mu A$$

$$I_{DN} = \frac{W}{L}\mu_N C_{ox}\left(V_{GSN} - V_{THN} - \frac{V_{DSN}}{2}\right)V_{DSN}$$

$$= 1mA/V^2\left(3.5V - 1V - \frac{V_{DSN}}{2}\right)V_{DSN}$$

By KCL, $I_{DN} = -I_{DP}$

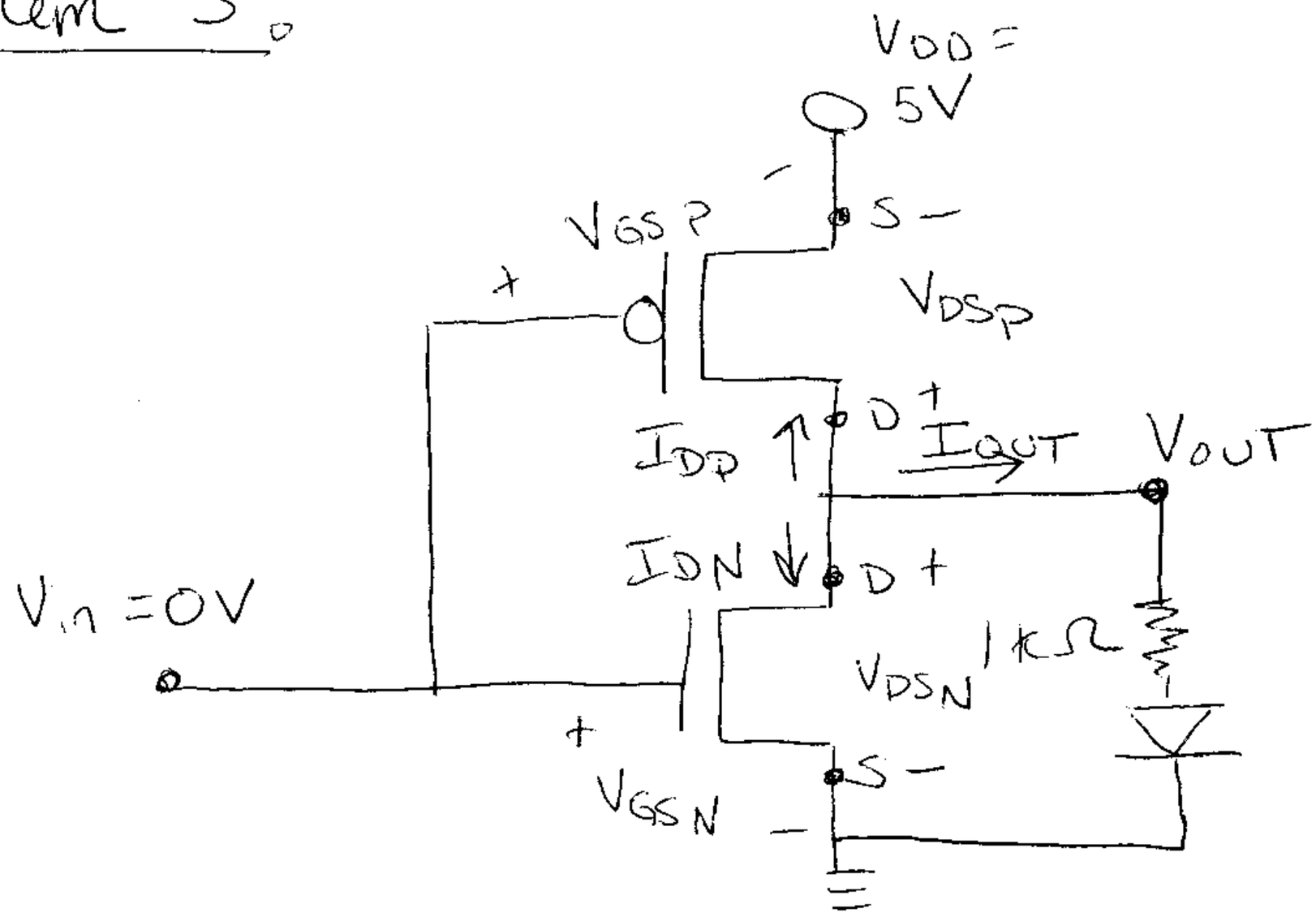
$$-I_{DP} = 125\,\mu A = I_{DN} = 1mA/V^2\left(2.5V - \frac{V_{DSN}}{2}\right)V_{DSN}$$

Solutions: $V_{DSN} = \{0.05\,V, 4.95\,V\}$

4.95 V impossible for triode; $4.95V \not< V_{GSN} - V_{THN} = 2.5V$

$V_{DSN} = 0.05$ V $\quad V_{DSP} = V_{DSN} - V_{DD} = -4.95$ V

Problem 5:



NMOS cutoff! $V_{GSN} = 0V < V_{THN}$

PMOS "fully on" $V_{GSP} = -5V$

PMOS triode happens to be the right guess, but it's hard to guess this.

First I will show that PMOS triode is correct. Then I will show why PMOS saturation is wrong.

PMOS triode: (Also guess diode forward biased)

$$I_{D_P} = -\frac{W}{L}\mu_p C_{ox}\left(V_{GSP} - V_{THp} - \frac{V_{DSP}}{2}\right)V_{DSP}$$

$$= -1mA/V^2\left(-5V - -1V - \frac{V_{DSP}}{2}\right)V_{DSP}$$

$$I_{D_P} + I_{D_N} + I_{OUT} = 0 \quad \text{by KCL}$$

$$I_{DP} = -I_{OUT} \quad \text{"1"} \qquad I_{OUT} = \frac{V_{DSN} - 0.7}{1K} \quad \text{"2"}$$

$$V_{DSN} = V_{DD} + V_{DSP} = 5\,V + V_{DSP} \quad (3)$$

Plug equations (1), (2) and (3) into I_{DP} triode eqn

$$-\frac{5V + V_{DSP} - 0.7V}{1\,k\Omega} = -1mA/V^2\left(-4V - \frac{V_{DSP}}{2}\right)V_{DSP}$$

Solutions: $V_{DSP} = \{-9.05V, -0.95\,V\}$

$V_{DSP} = -9.05V < V_{GSP} - V_{THP} = -4V$
so this is impossible for triode mode.

$V_{DSP} = -0.95\,V$ is possible for triode mode.

$$I_{DP} = -I_{OUT} = -\frac{5V + V_{DSP} - 0.7V}{1\,k\Omega} = -3.35\,mA$$

Power absorbed by PMOS transistor:

$$P_{PMOS} = I_{D_P} V_{DS_P} = (-3.35mA)(0.95V) = 3.18\,mW$$

Power absorbed by NMOS transistor:

$$P_{NMOS} = I_{DN} V_{PSN} = 0\,W \quad (I_{DN} = 0A \text{ since NMOS cutoff})$$

Power absorbed by resistor:

$$P_R = I^2 R = (3.35mA)^2 \cdot 1k\Omega = 11.2\,mW$$

Power absorbed by diode:

$$P_D = VI = 0.7V \cdot 3.35mA = 2.34\,mW$$

Now to show PMOS saturation is wrong:

If PMOS saturation,

$$I_{Dp} = -\tfrac{1}{2}\, W/L\, \mu_p C_{ox} (V_{GSp} - V_{THp})^2$$

$$= -\tfrac{1}{2}\, 1mA/V^2 (5V - -1V)^2 = 8mA$$

Thus current must flow in the branch with the resistor + diode (since NMOS cutoff $\Rightarrow I_{DN} = 0A$). So diode is forward biased. (Voltage 0.7 V.)

Resistor voltage is $8mA \cdot 1k\Omega = 8V$.

$$V_{DSp} = 8V + 0.7V - 5V = 3.7V$$

Which is impossible for saturation; V_{DSp} must be less than $V_{GSp} - V_{THp} = -4V$.