EE 40
Homework #7
Solutions & Grading

Problem 1:

a) The additional I_D current, ΔI_D, is

$$\Delta I_D = \frac{W}{L} \mu_N C_{ox} (V_{GS_{DC}} - V_{TH}) \Delta V_{GS}$$

ΔV_{GS} ranges between $-B = -0.3$ & $B = 0.3$

ΔI_D ranges between $\pm 2\frac{mA}{V^2}(3V - 1V)\, 0.3V$

ΔI_D ranges between $-1.2\,mA$ & $1.2\,mA$

I_D ranges between $I_{D_{DC}} \pm \Delta I_D$

$I_{D_{DC}} = 1/2 \cdot W/L\, \mu_n C_{ox} (V_{GS_{DC}} - V_{TH})^2 = 4\,mA$

I_D ranges between $2.8\,mA$ & $5.2\,mA$

resistor voltage $= 2\,k\Omega\, I_D$

resistor voltage ranges between $5.6\,V$ & $10.4\,V$

---

* This will take transistor out of saturation mode! I told students that our approximation is still ok a little bit into triode mode.

Full credit for students who just assumed model is ok, <u>and</u> for students who reworked for triode mode.

b) gain: $\dfrac{10.4V - 5.6V}{0.3V - -0.3V} = \dfrac{4.8V}{0.6V} = 8$

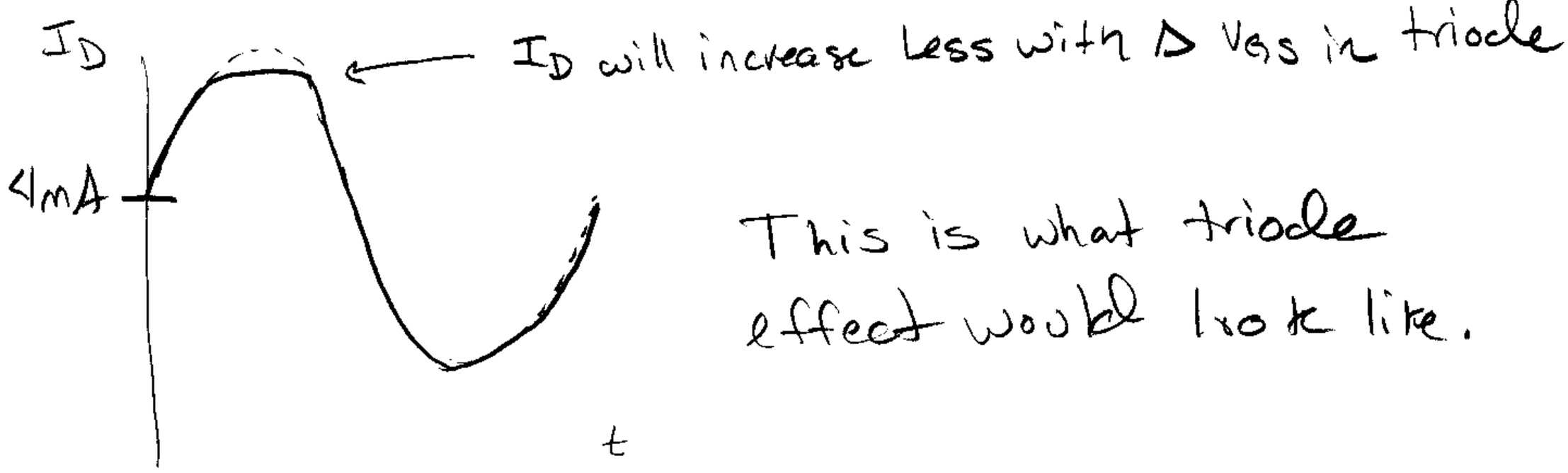
c) Assuming model is ok even just outside saturation mode,

$$I_D = 4mA + \frac{W}{L}\mu_n C_{ox}(V_{GS_{DC}} - V_{TH})\Delta V_{GS}$$

$$= 4mA + \frac{2mA}{V^2}(3V - 1V)\,0.3\sin t$$

$$= 4mA + 1.2mA \sin t$$

If triode taken into account, equation is quite complicated.



This is what triode effect would look like.

d) At saturation borderline when

$$V_{GS} - V_{TH} = V_{DS}$$

$$V_{GS_{DC}} + \Delta V_{GS} - V_{TH} = V_{DD} - 2K I_D$$

$$V_{GS_{DC}} + \Delta V_{GS} - V_{TH} = V_{DD} - 2K(I_{D_{DC}} + g_m \Delta V_{GS})$$

$$3\,V + B\sin t(V) - 1V = 12\,V - 2K\left(4\,mA + \frac{4mA}{V} B\sin t(V)\right)$$

$$2V + B\sin t(V) = 4\,V - 8\,B\sin t\,(V)$$

$$9\,B\sin t\,(V) = 2\,V$$

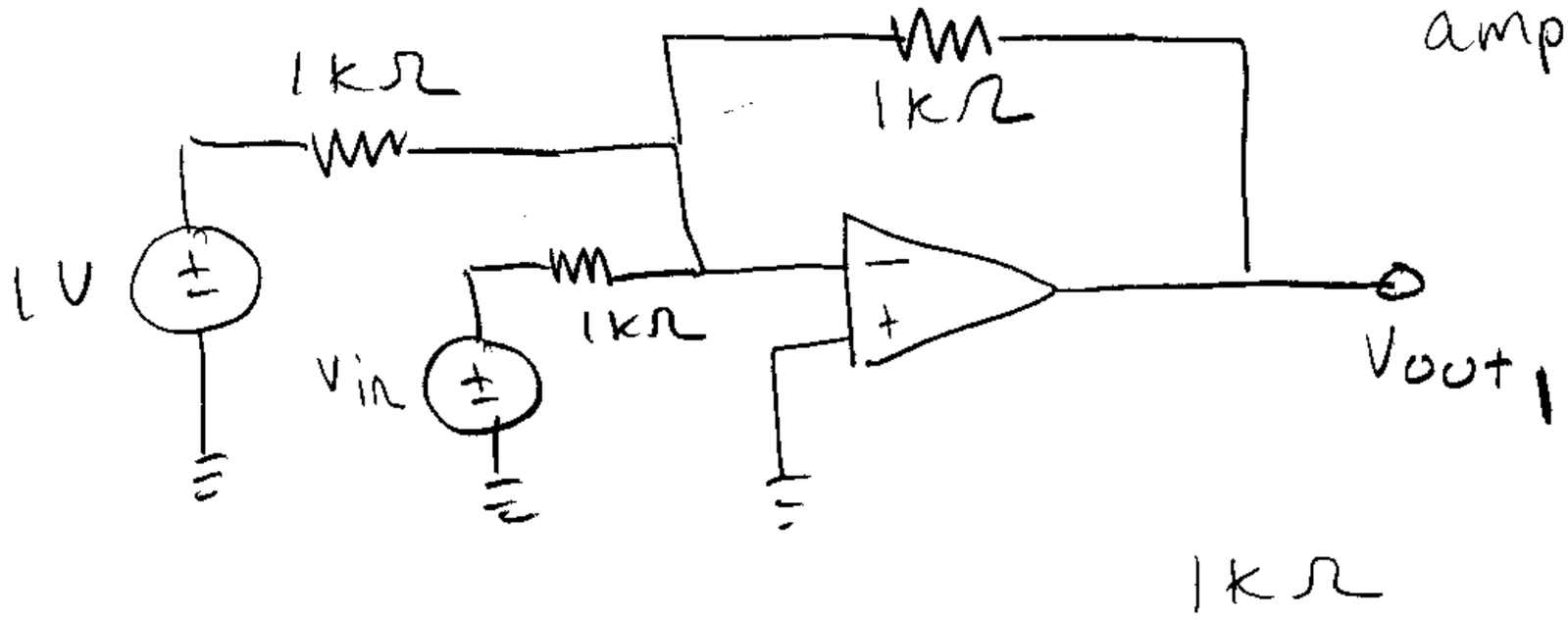
$$B = 2/9$$

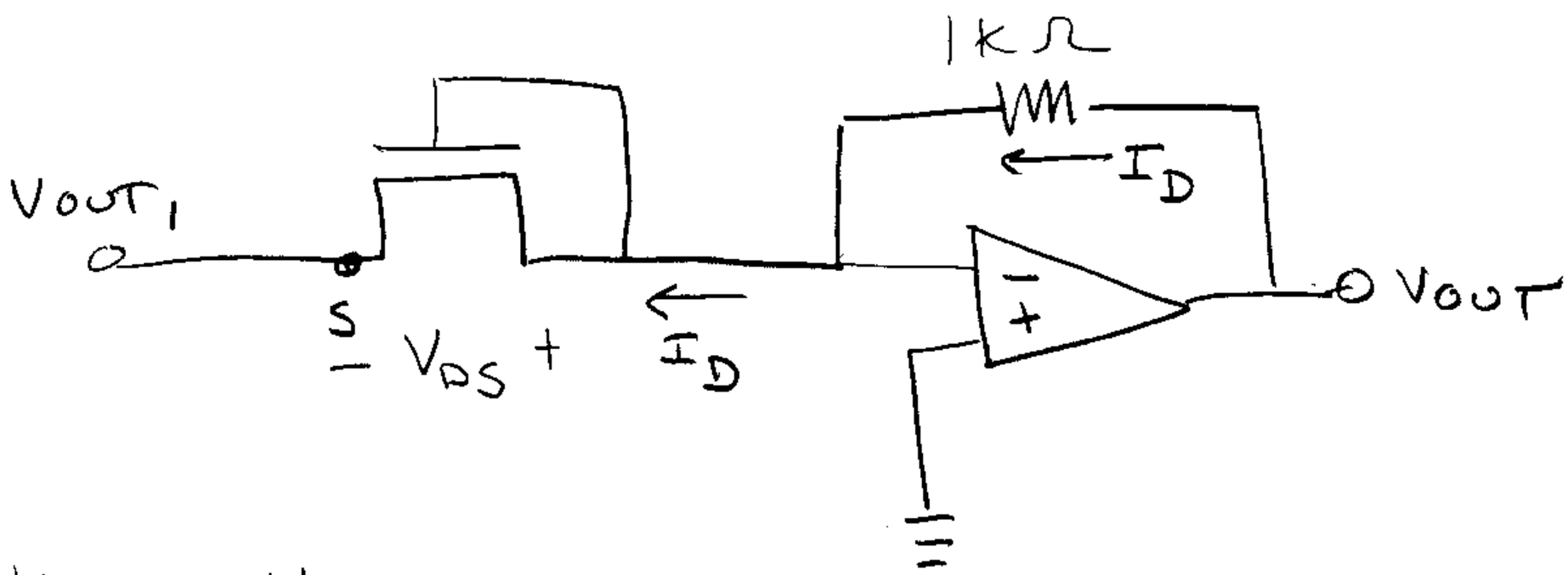
Problem 1 Grading: −2 for significant errors
−1 for minor errors

Problem 2:

Inverting-summing amplifier:

$$V_{OUT_1} = -V_{in} - 1\,V$$





KVL: $V_{OUT_1} + V_{DS} = 0$ $\qquad V_{DS} = -V_{OUT_1} = V_{in} + 1\,V$

$V_{GS} = V_{DS}$ since gate tied to drain

$V_{GS} = V_{DS} \Rightarrow$ Saturation mode $(V_{GS} - \underset{1V}{V_{TH}} < V_{DS})$

$$I_D = \tfrac{1}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 = \tfrac{1}{2}\, 2\,\frac{mA}{V^2}\,(V_{in} + 1V - 1V)^2$$

$$= 1mA\ V_{in}^2$$

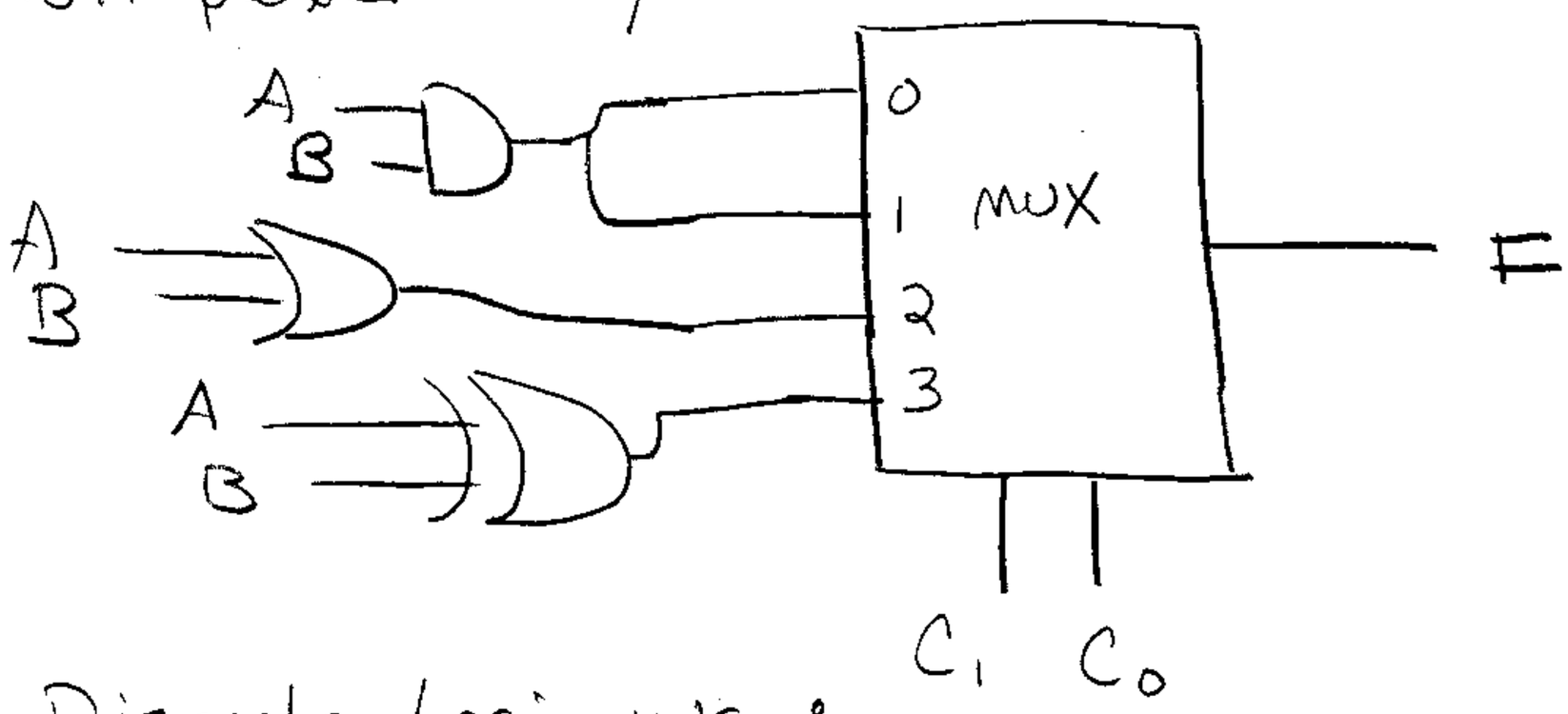
KVL: $V_{out} - 1K I_D = 0 \quad V_{OUT} = 1K I_D$

$$V_{OUT} = 1K\Omega \cdot 1mA\ V_{in}^2 = V_{in}^2$$

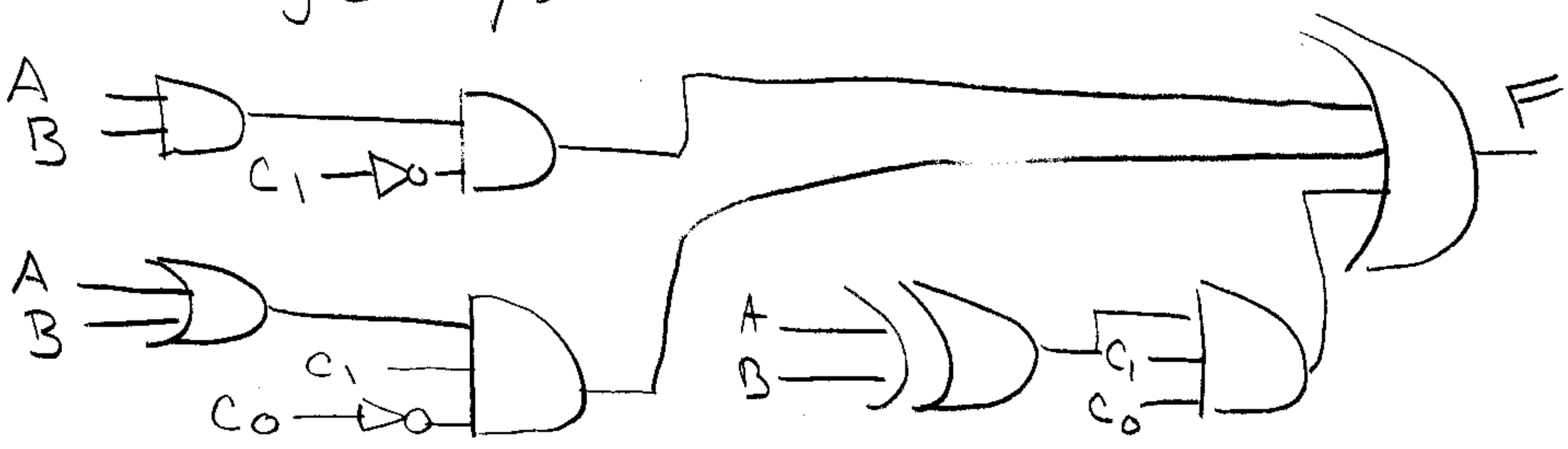
Problem 2 Grading: -1 for minor errors (signs, etc)
-3 for significant errors

Problem 3:

Multiplexer way:



Discrete Logic way:



Problem 3 Grading: -2 for each error

Problem 4:

a) 5 circuits x 2 ns/circuit = 10 ns

b) When you read that a circuit has "propagation delay of 2ns", that is the max signal delay. There may exist paths within the circuit with less delay.

So we must wait the full 11 ns between computations; a new signal could zip right through and change the output.

$$\frac{1 \text{ computation}}{11 \text{ ns}} = 90.9 \times 10^6 \text{ computations/s}$$

c) $5 \text{ circuits} \times \frac{2 \text{ ns}}{\text{circuit}} + 5 \text{ latches} \times \frac{1 \text{ ns}}{\text{latch}} = 15 \text{ ns}$

d) After a signal gets past the first latch (3ns), a new signal can be put on the input.

Maximum throughput when pipeline is full:

$$\frac{1 \text{ computation}}{3 \text{ ns}} = 333 \times 10^6 \text{ computations/s}$$

Alternatively, one can calculate throughput when the pipeline just starts up:

During the first computation (which takes 16 ns), the 2nd computation is in the pipeline for 13 ns, the 3rd for 10 ns, etc.

So the beginning throughput is

$$\frac{1 + 13/16 + 10/16 + 7/16 + 4/16 + 1/16}{16 \text{ ns}} = 199 \times 10^6 \text{ computations/s.}$$

In real life, the pipeline has to start over a lot due to "data hazards", so the pipeline throughput varies.

Full credit for any reasonable analysis like the ones above.

<u>Problem 4 Grading</u>: -1 for minor error or misunderstanding
-2 for significant error