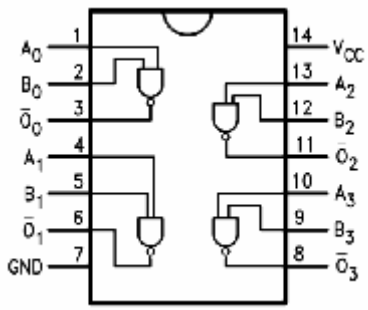
# EE43/EE100 — LAB #9
# Digital Logic Guide

## I. Introduction

In this introduction to CMOS digital logic, you will use commercially available "quad NAND gates" to breadboard the NOT gate and the XOR gate and measure their propagation delays on the oscilloscope.

### Commercial NAND Gates

In this lab, you will construct logic circuits using a DIP-package NAND gate from a family of standard logic ICs. In particular, you will be using the 74HC00, a Quad NAND array (or the Quad NAND IC). You will need more than one IC to construct the XOR function.




NOTE : This is a **TOP VIEW**. A half-circle or small circle indicates where pin 1 is.

**Figure 1.** The 74HC00 IC

There are 4 NAND gates in one package (see connection diagram above), hence it is named the "Quad NAND". Two special symbols require attention. One is the $V_{cc}$ (pin 14), which provides power to the chip and serves as the high logic level. $V_{cc}$ can be from +2 to +6V. The other is GND (pin 7), which serves as power return ground as well as the low logic level. Please see the full datasheet for more details.

### Normal Operation and Absolute Maximum Ratings

Please observe these parameters from the datasheet, especially the Absolute Maximum Ratings.
In particular:

1) **$V_{CC}$ CANNOT BE MADE NEGATIVE with respect to ground**
2) **inputs A and B CANNOT BE MADE NEGATIVE with respect to ground**
3) **inputs are NOT ALLOWED TO EXCEED $V_{CC}$**

The latter caution is somewhat subtle and particularly easy to violate (burning out the chip). For example if you are studying normal operation at 5V you may be tempted to use logic levels of 0 and 5 V at the inputs. Now if you turn down $V_{CC}$ and you continue to drive the inputs with a 5V logic signals, you will violate rule 3!!!! THEREFORE, BE CAREFUL NEVER TO DRIVE THE INPUTS WITH VOLTAGES EXCEEDING $V_{CC}$.

Another feature to note from the datasheet is the dependence of the gate delay performance on $V_{CC}$. "Nominal worst case" operation is at $V_{CC}$ = 4.5V (because that is the lower end of the nominal power supply range of 5V +/- 10%). But these devices are also designed to work at much lower values of $V_{CC}$, down to 2V. This provides a great opportunity to observe gate delays in a regime where they are very easy to measure.

## II. Experimental Section

### Part 1: Chain of Inverters

1. Before studying an XOR gate constructed from NAND gates, we want you to first study a much simpler circuit: a chain of inverters (NOT gates). We suggest making the inverters by wiring one of the NAND inputs to logic 1. This gives the input signal a load of only one gate input. On your lab report draw the breadboard diagram of the chain of inverters constructed using one 74HC00. Include the top view of the 74HC00 plugged into your prototype board and the wiring used to complete the circuit. Whenever using ICs, all input pins should be defined, not floating. Here, we will be using every pin on the package. In this diagram you can show the internal wiring of the breadboard explicitly.
2. Verify the static operation of the chain of inverters by constructing the inverter chain, then using a wire to apply either $V_{dd}$ = 5V = logic 1 or $V_{ss}$ = 0V = logic 0 to the chain input. Using the scope, verify the logic states within the chain. Repeat for $V_{dd}$ = 2V. Next, set up the function generator to provide a 1kHz square wave to the input and verify the switching of all the inverters in the chain.

### Part 2: Propagation Delay of Inverter Chain

3. We will measure the delay of 4 inverters, 3 inverters, two inverters and a single inverter using the oscilloscope. (To do this you use the square-wave generator to drive the input and to trigger the scope. Set the scope Main Delay time reference to left. You can use the cursors to measure the gate delay. For example, to measure the gate delay through gate 3 you measure the time between when the *input* reaches 50% ($0.5*V_{CC}$) and the time the *output* reaches 50%.) Repeat for $V_{CC}$ = 5V, 2V. Assuming that the probe disturbs the delay (by adding capacitance), you can estimate this disturbance from the measurements above. In particular, the difference between one gate and three gates represents two times the average gate delay.

$$\tau_{propagationdelay} = \frac{\tau_{low-to-high} + \tau_{high-to-low}}{2}$$

4. Set the function generator to a 1 kHz square wave. Measure the gate delays through 1, 2, 3, and 4 gates at $V_{dd}$ = 5V, then $V_{dd}$ = 2V. Be sure to set the function generator $V_{PP}$ and $V_{DC}$ for different $V_{dd}$ (do not violate the rules outlined in the Introduction!). The square wave will also need to be offset, to avoid violating rule 2. Ask your GSI for help if you are unsure of how to do this. To switch between high-to-low (HL) and low-to-high (LH) transitions, switch the trigger edge direction. For convenience, set Time Ref to Left.
5. Based on the average of the difference between 1 and 3 gates (two gate delays), what is the average gate delay at each of the $V_{dd}$ supply voltages? (Note: we do not want to use measurements from the last gate since it is not loaded by any other logic gate input).

### Part 3: The XOR Function

6. In the prelab you showed the NAND realization of the XOR function. Although this may not be an optimal design, it will work, and it will have at most three gate delays (one inverter and two NAND delays). On your lab report, draw the layout on your prototype board of an XOR circuit using two 74HC00 packages. Show all wires including the "hidden" wires in the prototype board. You will use five NAND gates plus one more to act as the load on the output. (Show this one also in your circuit). Short the inputs on the two unused NAND gates to ground and leave the outputs open.
7. Construct the XOR circuit, and verify its static operation by wiring inputs to logic high ($V_{dd}$) or low (Vss = 0V) and using the scope to view the output.. Fill out the truth table on your lab report. Show the circuit to your TA and show proper static logic functionality**.**

**Part 4: Propagation Delay of the XOR**

8. Now we will measure the dynamic performance of the XOR circuit. You have loaded the output with a spare NAND gate input, so in the following you are measuring the delay of an XOR gate with a fanout of 1.
9. Use a square wave input on input A and measure propagation delay for the XOR, at $V_{dd}$ = 5V and 2V. Use the same technique as in the inverter chain. Make sure to adjust the square wave to match the $V_{dd}$ voltage levels (**AGAIN: THE INPUT LOGIC VOLTAGE CANNOT EXCEED $V_{CC}$ !!!**). How do these delay times compare with the inverter gate delays?

**More fun: Using LEDs to see digital logic states (optional)**

To detect the logic level of a given circuit node, one can use a voltmeter or scope. However, for static measurements, it is attractive to have a simple visual indicator. You can build such a logic probe using an LED in series with a resistor. Note that the LED is a diode with a polarity, and is meant to conduct electrons and emit light in one direction. The amount of current you need (typically from 1 to 10 mA) to be able to clearly see the LED light depends on the LED efficiency. The high current end is limited by the source capability of the NAND gate output, which is about 10mA at 5V. Assuming a diode drop of about 1.6V to 1.8V, a resistor in the range of 300 ohms may be adequate for the full voltage range, but you must test your detector for correct operation and adequate LED brightness over the range 2V to 5V. WARNING: YOU CAN DAMAGE both the LED and the logic chip if you have too low a resistance. In no case use less than 200 ohms. Show your logic probe to your GSI.