Name: Solutions

EE 40

FINAL EXAM

December 13, 2002

PLEASE WRITE YOUR NAME ON EACH ATTACHED PAGE

PLEASE SHOW YOUR WORK TO RECEIVE PARTIAL CREDIT

Problem 1: 10 Points Possible _____

Problem 2: 10 Points Possible _____

Problem 3: 15 Points Possible _____

Problem 4: 15 Points Possible _____

Problem 5: 30 Points Possible _____

Problem 6: 30 Points Possible _____

Problem 7: 60 Points Possible _____

Part 7a: 30 Points Possible _____

Part 7b: 30 Points Possible _____

Part 7c: 30 Points Possible _____

Complete 2 of these 3 parts of Problem 7, for a total of 60 points.

If you complete all 3 parts, your 2 highest-scoring parts will count.

Problem 8: 30 Points Possible _____

Problem 9: 1 Point Possible _____

TOTAL: 201 Points Possible _____

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Problem 1: 10 Points Possible

Match each description below to a substance by writing the number next to the substance.

Note: Some substances have more than one matching description!

1. Makes a good material for transistor gate because of its low resistance and ability to withstand high temperature anneals
2. Deposited onto wafer by "sputtering"
3. Implanted into wafer by high-energy ion impact and heated to a temperature > 800 °C
4. "Grown" on wafer through thermal oxidation
5. Medium which allows designer to pattern layers using a mask
6. Protects materials from removal during "etching"
7. Serves as insulator between conducting layers
8. Deposited by shooting argon atoms at a target made of the deposit material, knocking loose atoms which fall on the wafer surface
9. Parts which are exposed to light wash away in a developing liquid
10. Deposition of this material causes damage to wafer, requiring "annealing" to repair

Silicon Dioxide 4, 7

Dopants 3, 10

Aluminum 2, 8

Photoresist 5, 6, 9

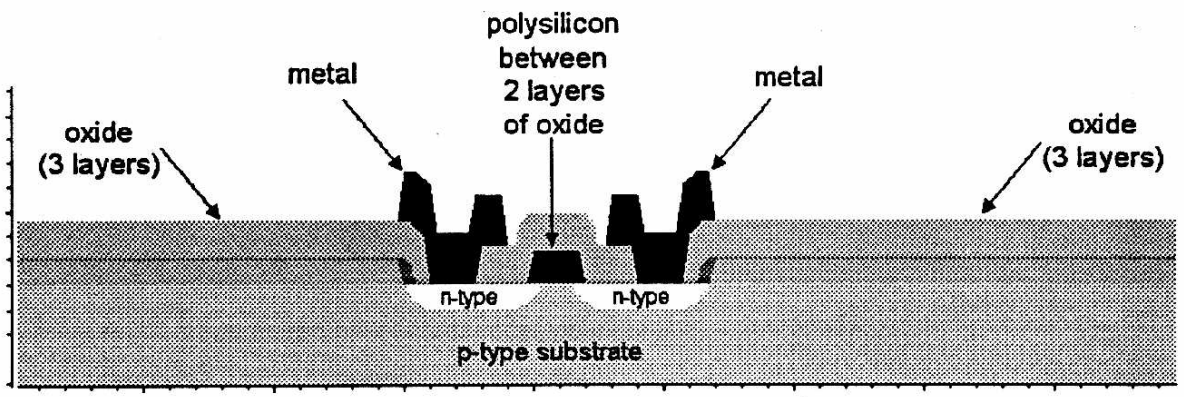
Polysilicon 1

Name: _____

Problem 2: 10 Points Possible

Consider the NMOS transistor with cross-section shown. Put the steps involved in the fabrication of this device in correct order.

Pattern metal	Step 1:	Grow oxide 500nm
Grow oxide (20 nm thick)	Step 2:	Pattern oxide
Implant donors	Step 3:	Implant donors
Deposit polysilicon	Step 4:	Grow oxide 20nm
Grow oxide (500 nm thick)	Step 5:	Deposit polysilicon
Deposit metal	Step 6:	Pattern polysilicon
Pattern polysilicon	Step 7:	Deposit oxide 750nm
Pattern oxide	Step 8:	Pattern oxide
Deposit oxide (750 nm thick)	Step 9:	Deposit metal
Pattern oxide	Step 10:	Pattern metal



Name: Solutions

Problem 3: 15 Points Possible

Suppose we have connected the output of CMOS inverter 1 to the input of CMOS inverter 2, where the inverters have the following characteristics:

Both inverters:

$\mu_N = 500\ cm^2/(Vs)$	$\mu_P = 250\ cm^2/(Vs)$	$V_{T(N)} = -V_{T(P)} = 1\ V$
$t_{ox} = 10\ nm$ (oxide thickness)	$k_{ox} = 4$ (oxide dielectric constant)	$V_{DD} = 5\ V$
$L_I = 20\ \mu m$ (interconnect length)	$W_I = 1\ \mu m$ (interconnect width)	$\varepsilon_0 = 8.85 \times 10^{-12}\ F/m$

Inverter 1:

$L_N = L_P = 2\ \mu m$	$W_N = 6\ \mu m$	$W_P = 24\ \mu m$	$C_{DB(P)} = C_{DB(N)} = 50\ fF$

Inverter 2:

$L_N = L_P = 2\ \mu m$	$W_N = 8\ \mu m$	$W_P = 16\ \mu m$	$C_{DB(P)} = C_{DB(N)} = 75\ fF$

Find the propagation delay for the output of inverter 1, when the input of inverter 1 changes from logic 0 to logic 1 instantaneously (after being logic 0 for a long time).

$$t_p = 0.69\,\tau$$

$$\tau = R_N\left(C_{DBN_1} + C_{DBP_1} + C_{GBN_2} + C_{GBP_2} + C_I\right)$$

$$R_N = 0.75\,V_{DD}/I_{DSAT_1} = 0.75V_{DD}\Big/\left(\frac{W_{N1}}{2L_{N_1}}\mu_n C_{ox}(V_{GSN_1} - V_T)^2\right)$$

$$= 0.75(5)\Big/\left[\left(\frac{6\cdot10^{-6}}{2\cdot2\cdot10^{-6}}\right)(500\cdot10^{-4})\left(\frac{4(8.85\cdot10^{-12})}{10\cdot10^{-9}}\right)(5-1)^2\right]$$

$$= 883\,\Omega$$

$$C_{GBN_2} = C_{ox}W_{N_2}L_{N_2} = \frac{4(8.85\cdot10^{-12})}{10\cdot10^{-9}}(8\cdot10^{-6})(2\cdot10^{-6}) = 56\,fF$$

$$C_{GBP_2} = C_{ox}W_{P_2}L_{P_2} = \frac{4(8.85\cdot10^{-12})}{10\cdot10^{-9}}(16\cdot10^{-6})(2\cdot10^{-6}) = 112\,fF$$

$$C_I = C_{ox}W_I L_I = \frac{4(8.85\cdot10^{-12})}{10\cdot10^{-9}}(1\cdot10^{-6})(20\cdot10^{-6}) = 70\,fF$$

$$t_p = 0.69(883)(56+112+70+50+50)10^{-15}$$

$$= 206\,ps$$

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Problem 4: 15 Points Possible

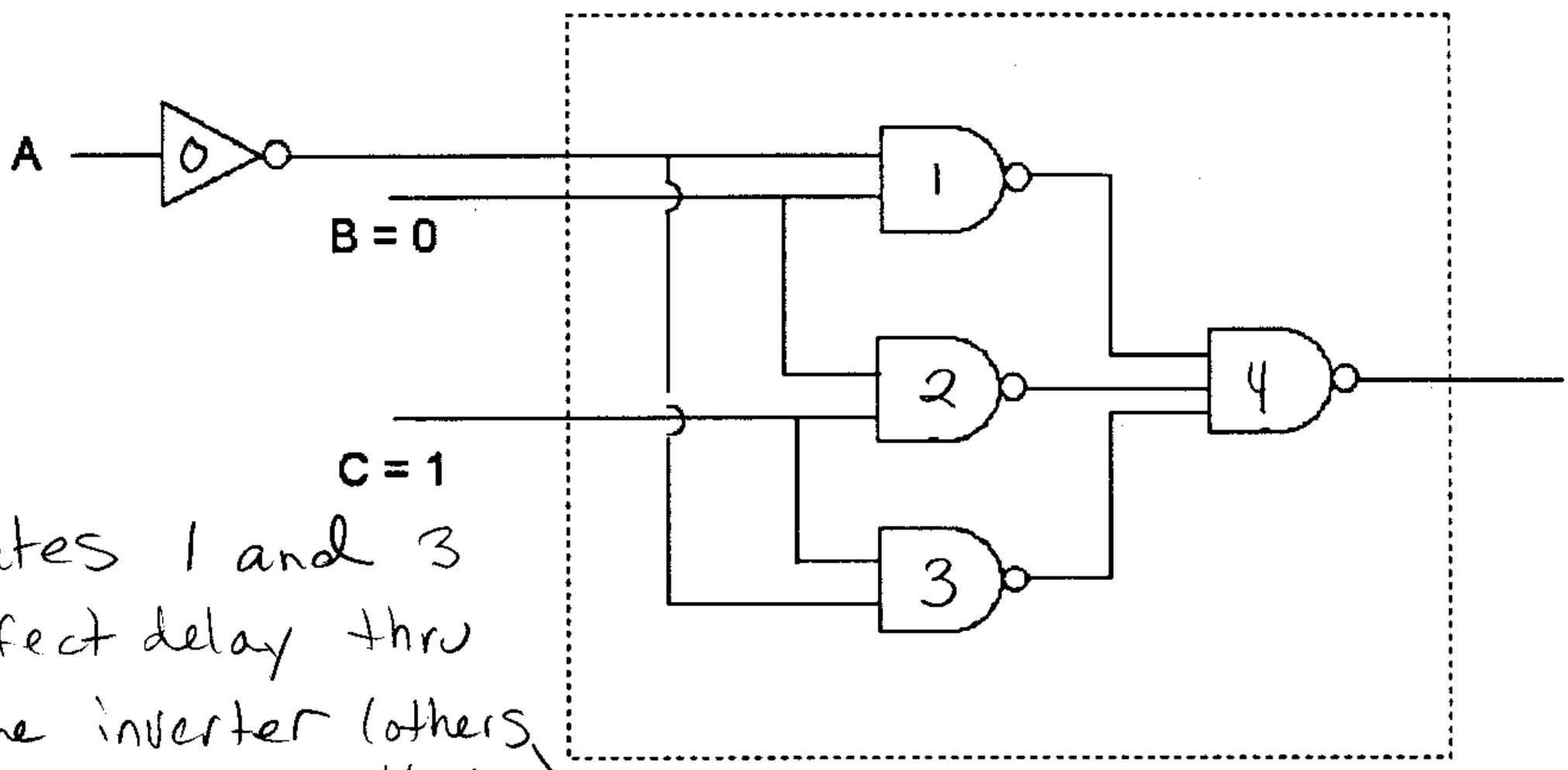
Suppose I hook an inverter up to one of the inputs of our 3-bit adder's most significant digit function. Find the propagation delay from the input to the output of the inverter when the inverter input A goes from low to high (with the other adder inputs held constant as shown).

For all of the gates, use

$C_{DB(P)} = C_{DB(N)} = 50$ fF $C_{GB(P)} = 50$ fF $C_{GB(N)} = 75$ fF

$C_I = 100$ fF **per gate** $R_N = 3$ kΩ $R_P = 2$ kΩ

A NAND-NAND implementation of the circuit is shown below.



Gates 1 and 3 affect delay thru the inverter (others not directly attached).

One connection to gate 1 and one connection to gate 3: Use 2 gate capacitances (C_{GBN} and C_{GBP}) for gate 1 and for gate 3. Use 2 C_I (2 gates connected).

$$t_p = 0.69 R_N (C_{DBN_0} + C_{DBP_0} + C_{GBN_1} + C_{GBP_1} + C_{GBN_3} + C_{GBP_3} + 2C_I)$$

$$= 0.69(3000)(50 + 50 + 75 + 50 + 75 + 50 + 2 \cdot 100)10^{-15}$$

$$= \boxed{1.14 \text{ ns}}$$

Name: Solutions

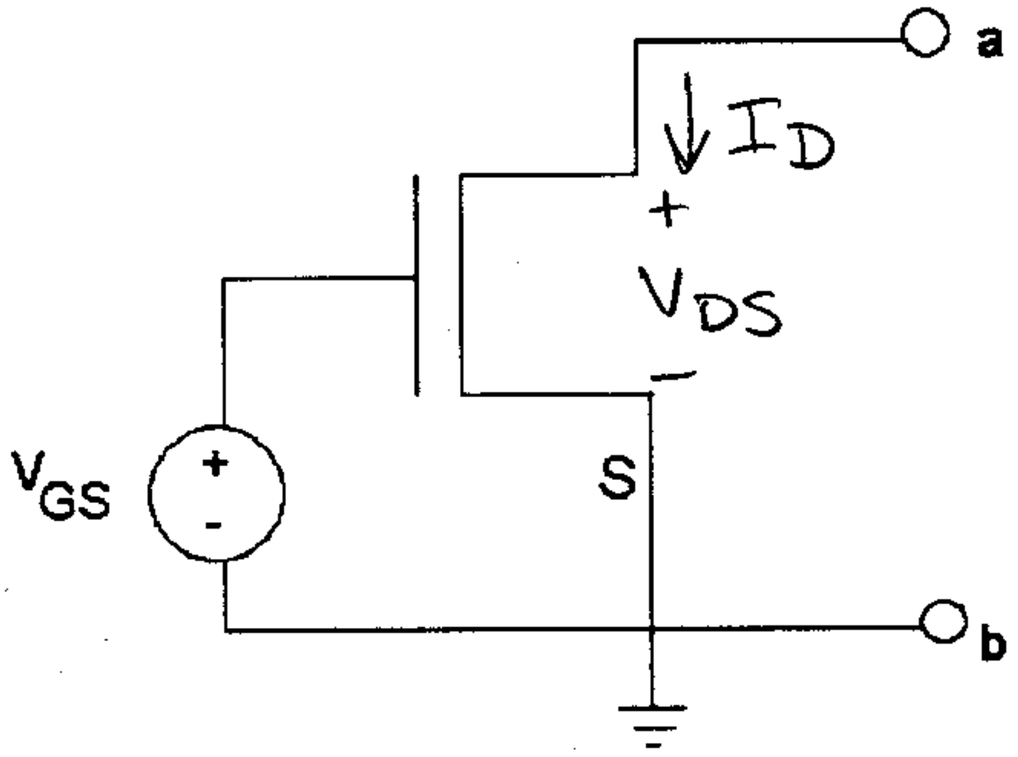
Problem 5: 30 Total Points Possible

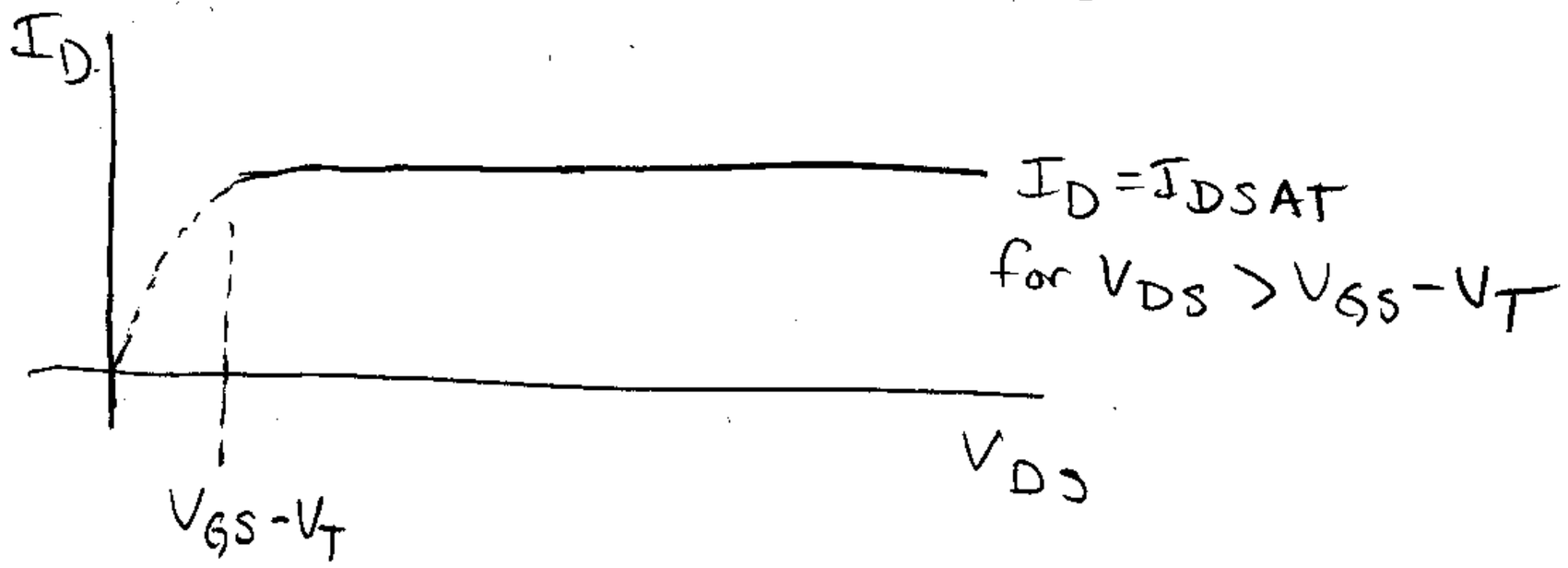
a) 10 Points Possible

Consider the NMOS transistor circuit below, where V_{GS} is constant and above V_T.

Assume $\lambda = 0$. Graph the I_D vs. V_{DS} relationship for $V_{DS} > V_{GS} - V_T$.

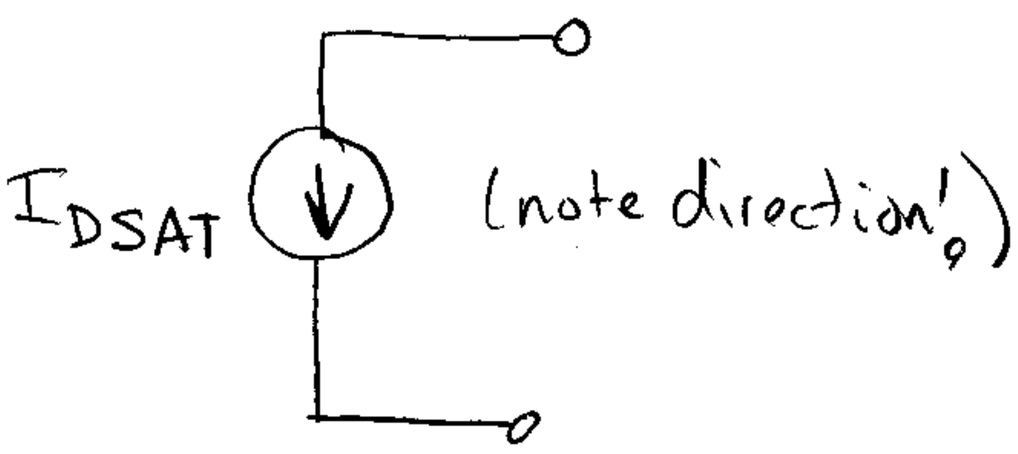
Does this circuit have a Thevenin and/or Norton equivalent for this region of operation (when $V_{DS} > V_{GS} - V_T$)? If yes, give the equivalents. If no, explain why the equivalents do not exist.





Constant current, any voltage ⇒ current source

Norton equivalent:



Thevenin equivalent:
does not exist for current source

Name: Solutions

Problem 5 continued

b) 10 Points Possible

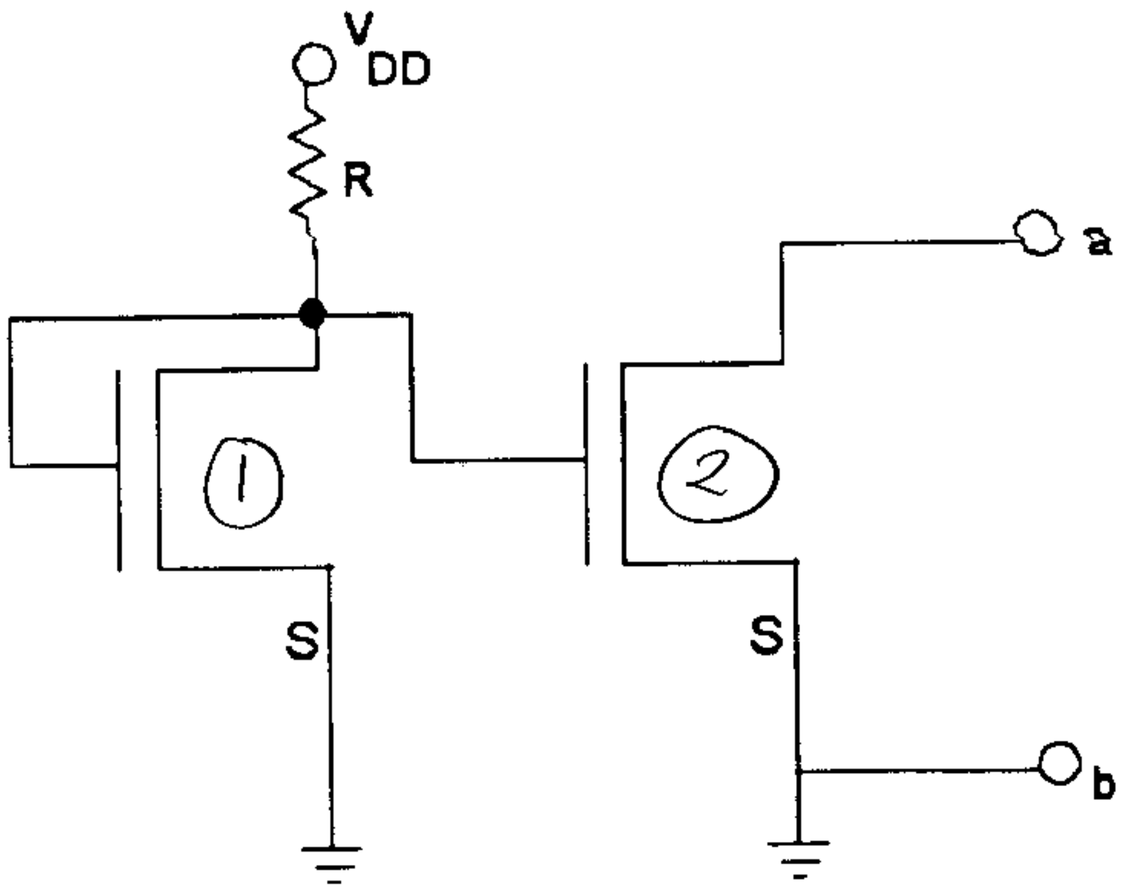
Consider the NMOS transistor circuit below, where V_{DD} is constant and above V_T.

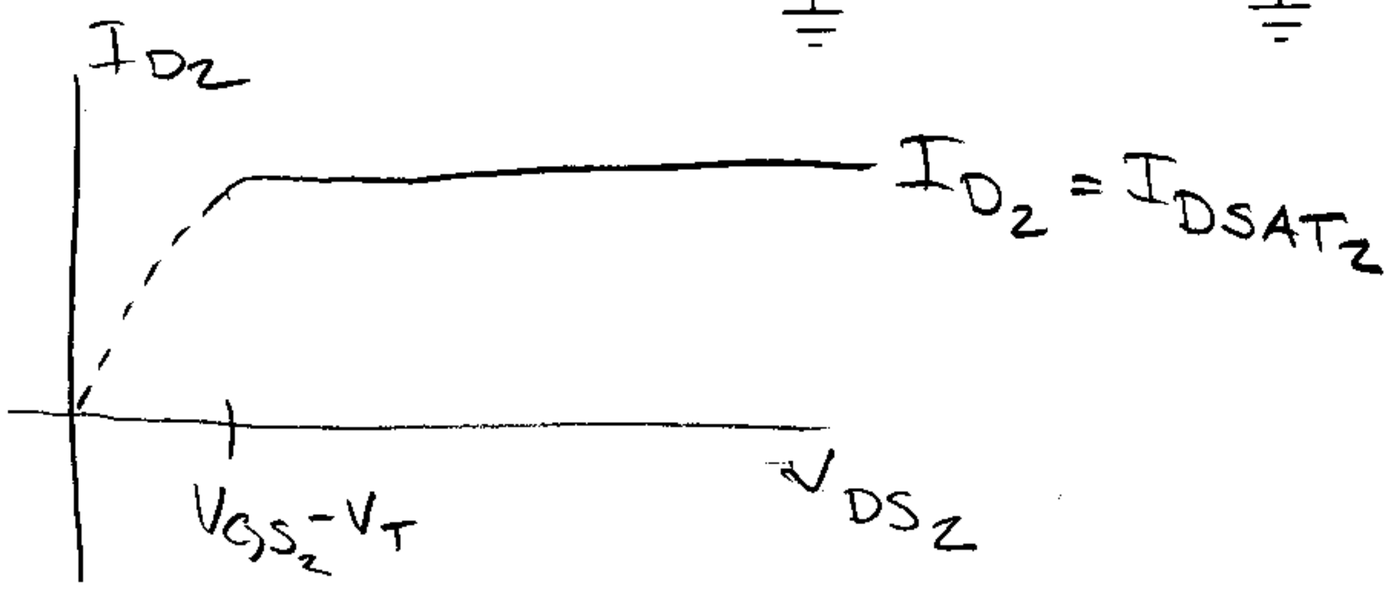
Assume that both transistors have all the same parameters, and $\lambda = 0$.

Graph the $I_{D(2)}$ vs. $V_{DS(2)}$ relationship for $V_{DS(2)} > V_{GS(2)} - V_T$.

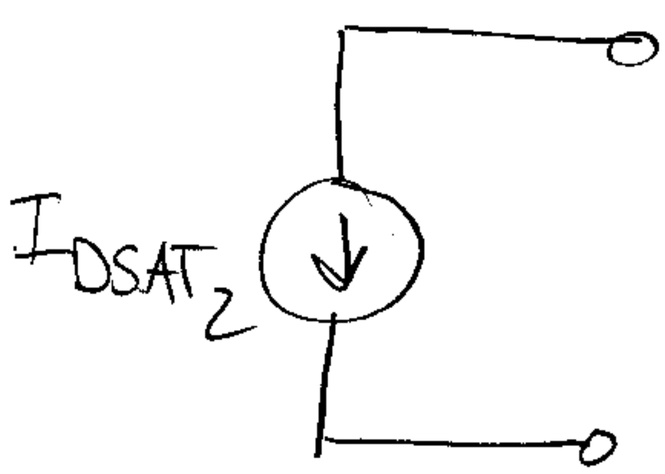
Does this circuit have a Thevenin and/or Norton equivalent for this region of operation (when $V_{DS} > V_{GS} - V_T$)? If yes, give the equivalents. If no, explain why the equivalents do not exist.

$V_{DS_1} = V_{GS_2}$ and is constant since supply voltage (V_{DD}) is constant.





Norton equivalent:



Thevenin equivalent! does not exist for current source

Name: Solutions

Problem 5 continued

c) 10 Points Possible

Suppose that as the circuits operate, they heat up. This causes an increase in the electron mobility μ_N. How does this affect the operation of the circuit in Part a? How does this affect the operation of the circuit in Part b?

Part a: When μ_N increases, I_{DSAT} increases. The current supplied by this "current source" circuit increases.

Part b: When μ_N increases, both I_{DSAT_1} and I_{DSAT_2} increase.

An increase in I_{DSAT_1} means that the voltage over the resistor increases.

Since $R I_{DSAT_1} + V_{DS_1} = V_{DD}$ (constant), V_{DS_1} must decrease.

This decreases the value of V_{GS_2} and therefore decreases I_{DSAT_2}.

The overall increase in the current supplied by the current source will be smaller than for part a due to this negative feedback.

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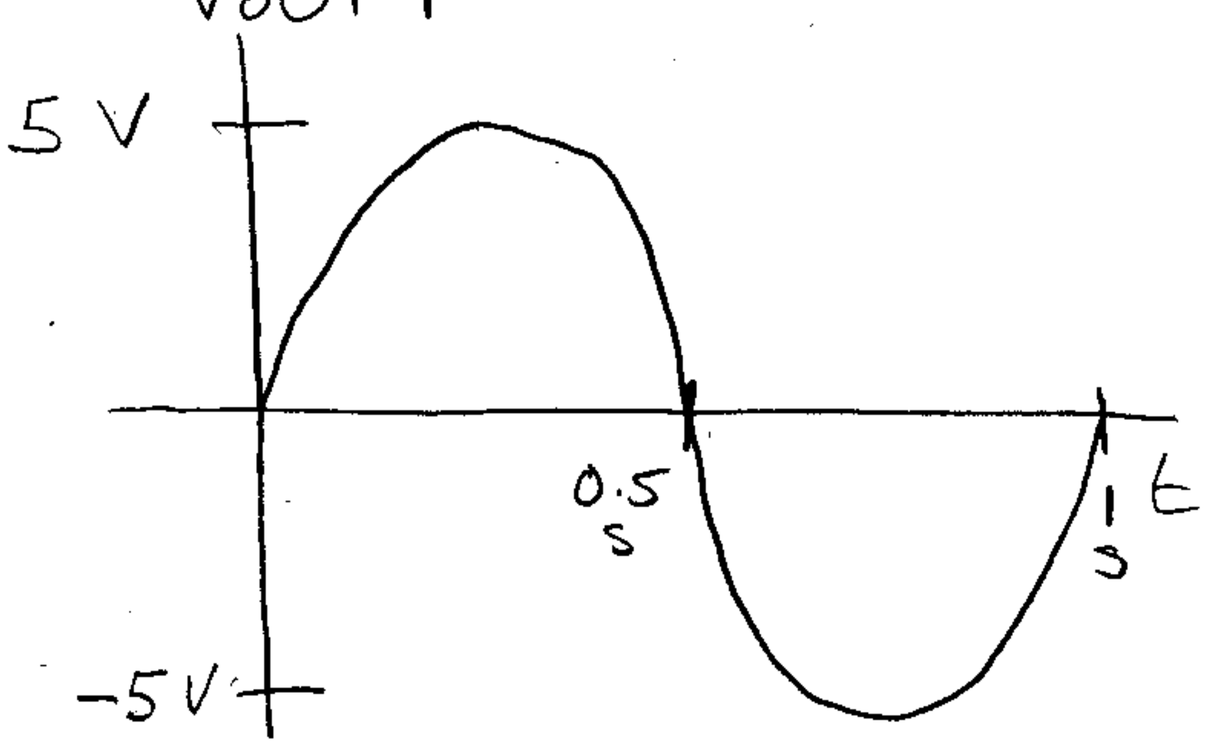
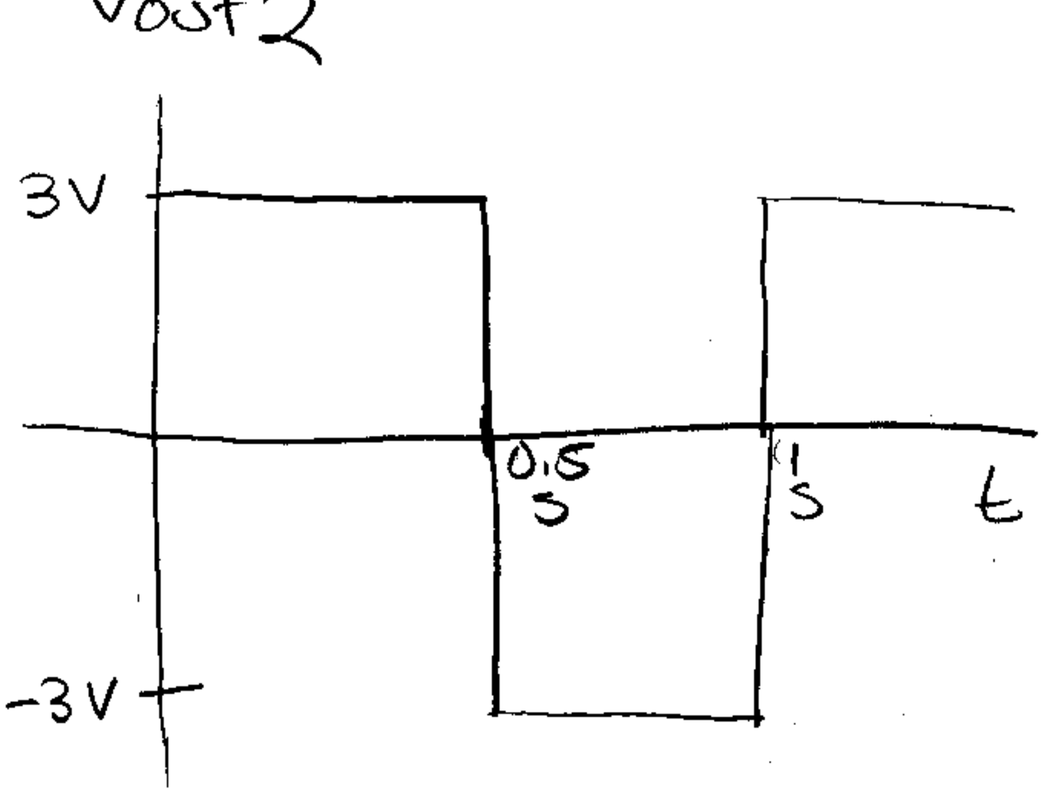
Problem 6: 30 Points

The circuit on the next page has 5 outputs: V_{OUT1}, V_{OUT2}, V_{OUT3}, V_{OUT4}, and V_{OUT5}. Graph each of these outputs with respect to time. The more detailed your graphs are, the more points you get (up to 6 points per graph).

Vout 1

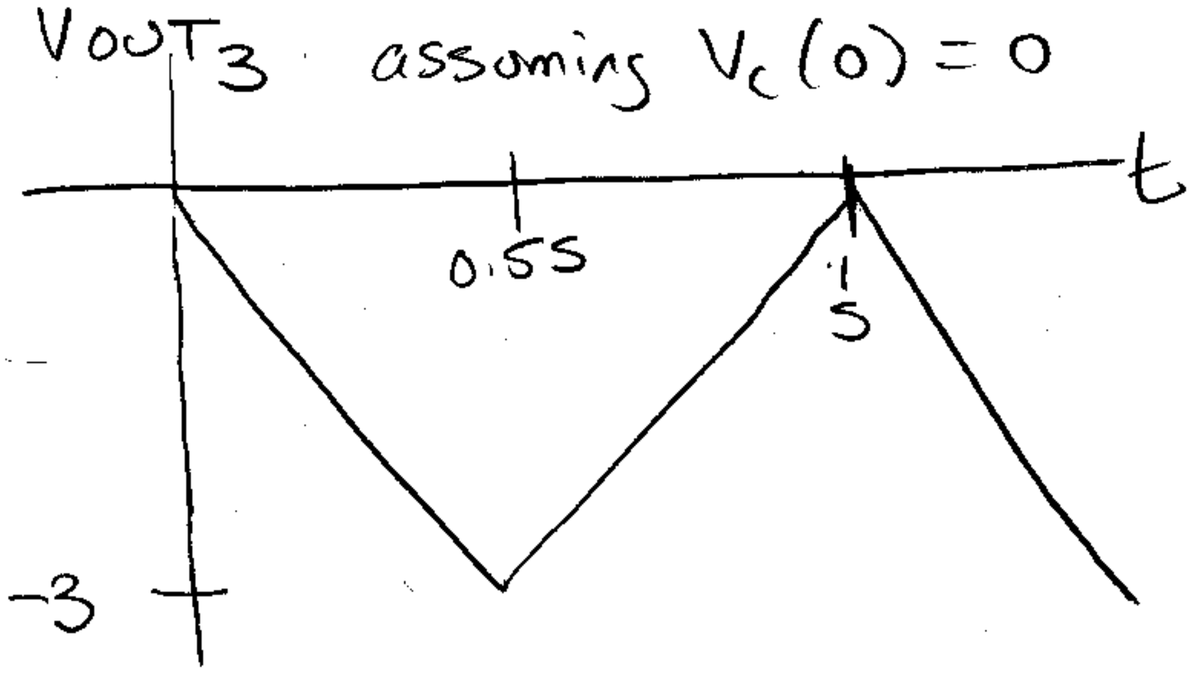


Vout 2

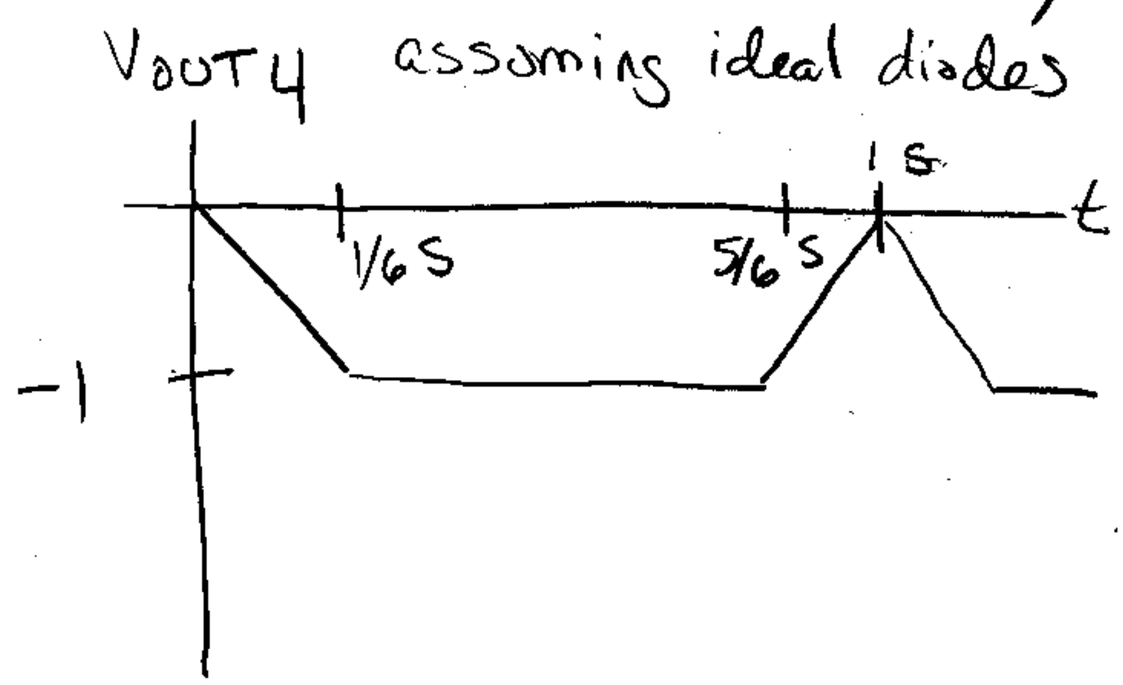


V_{OUT3} and V_{OUT4} may look different depending on initial phase when circuit started operation. Assuming 0 phase,

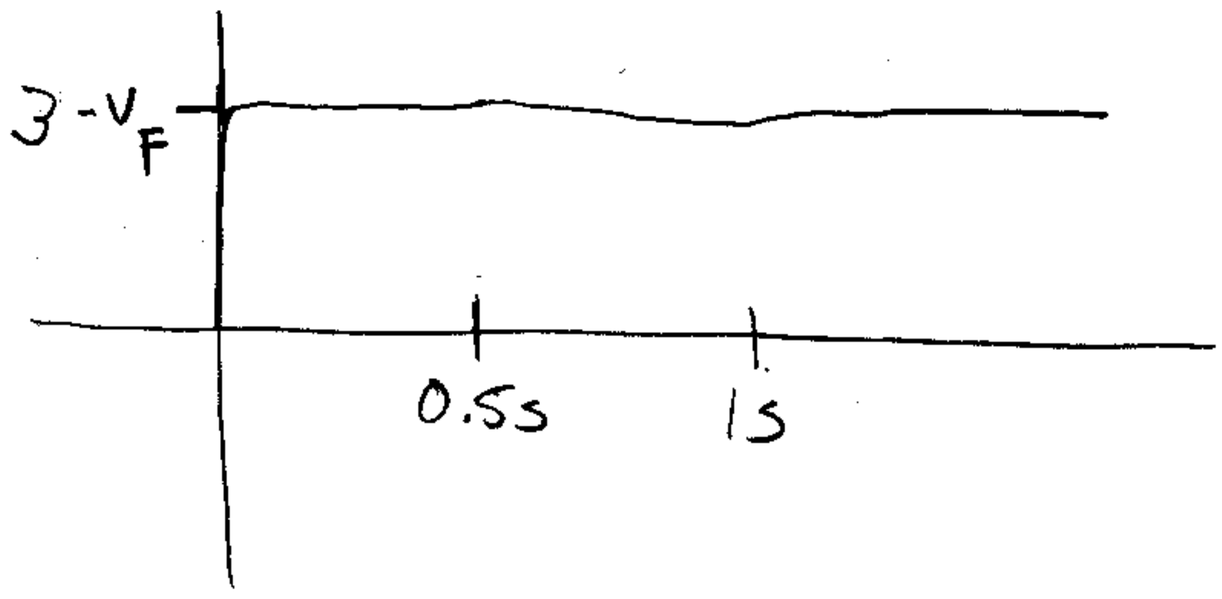
V_{OUT3} assoming $V_c(0) = 0$



V_{OUT4} assoming ideal diodes



$Vout_5$ assoming small-signal diode



- Charging is almost immediate since diode resistance small
- Discharging extremely slow, keeps 99.95% of value after 0.5 s

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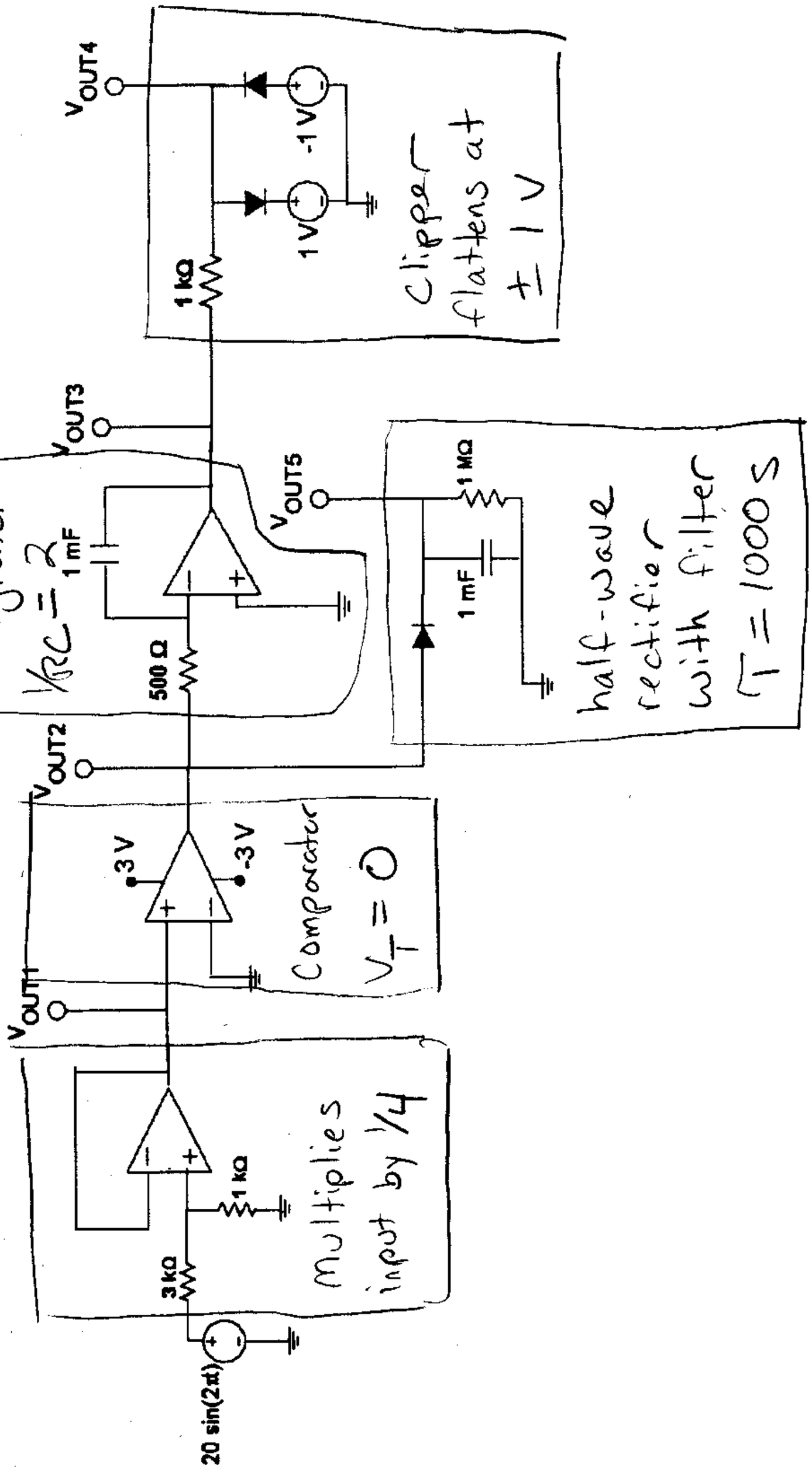
Problem 6 continued



Name: Solutions

Problem 7: 60 Points Possible

Perform 2 of the following 3 designs, worth 30 points each. If you complete all 3 designs, the 2 highest scores will be counted.

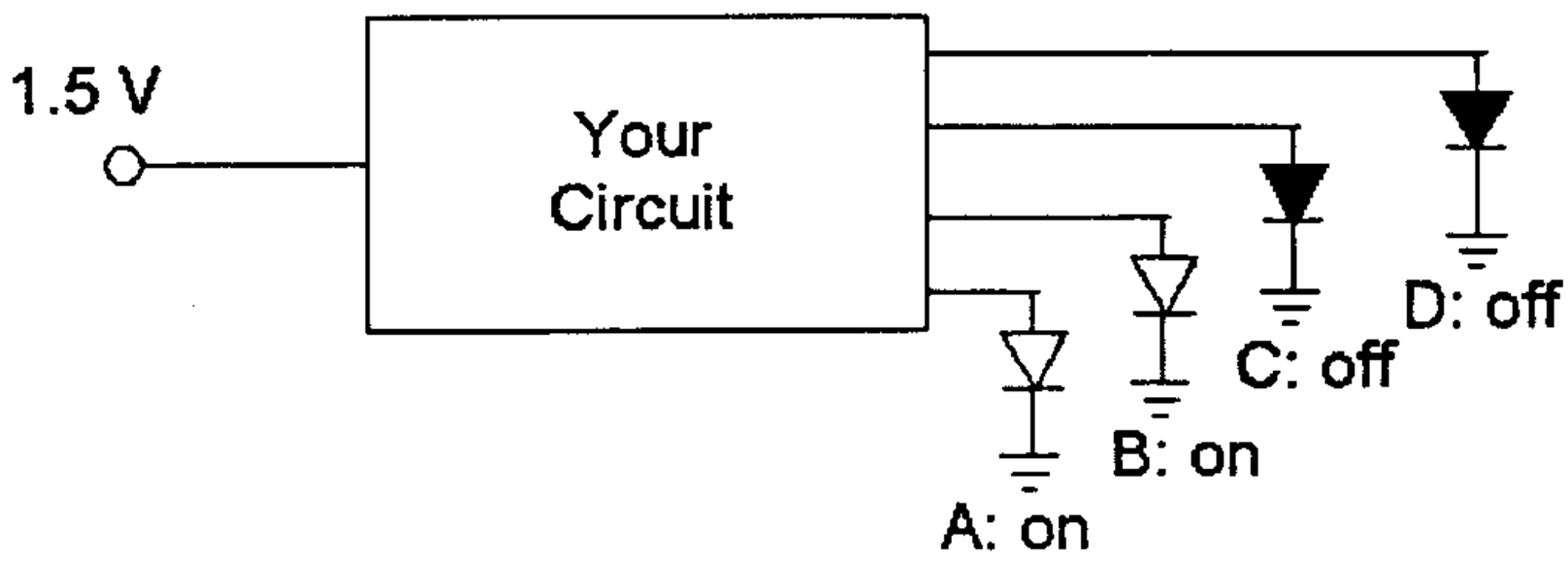
Indicate clearly which design problem you are answering, and what your final design is. Indicating the important features of your design will help us give you maximum credit.

a) As input, you are given an analog voltage (continuous voltage) between 0 V and 4 V. You are also given 4 LED's named A, B, C and D.

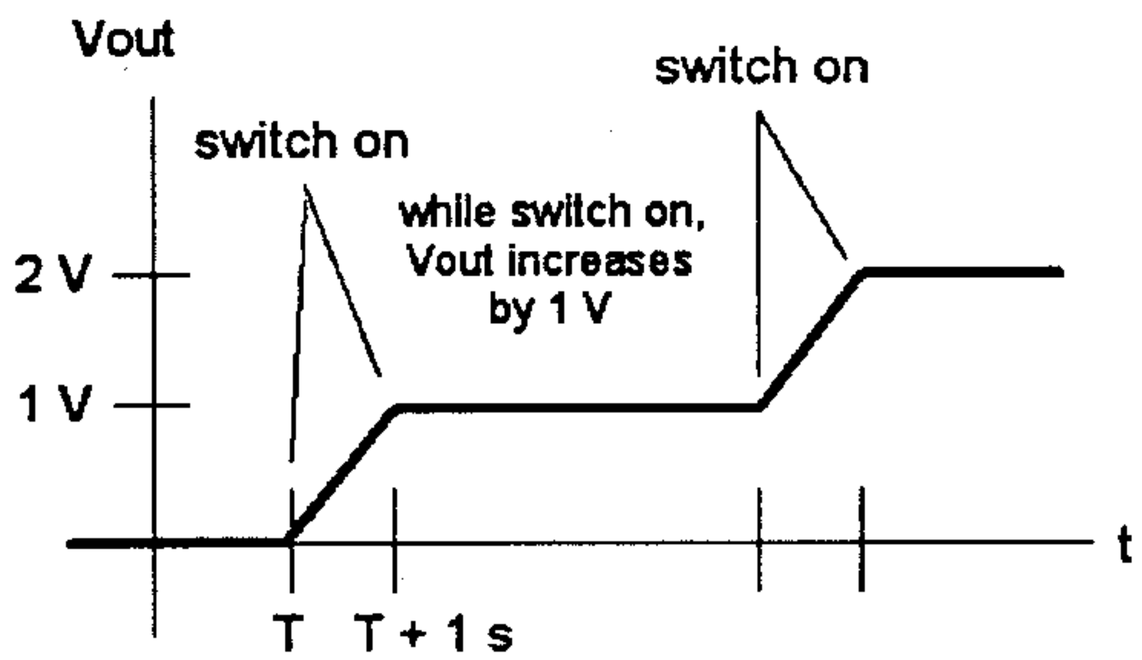
If the input voltage is below 1 V, LED A should light up. If input is between 1 V and 2 V, LED's A and B light up. If input is between 2 V and 3 V, LED's A, B and C light up. If input is above 3 V, LED's A, B, C, and D light up.

Example:

Vin = 1.5 V, so LED's A and B light up:



b) A user will occasionally flip a switch on, leave it on for 1 second and then turn it off. Create a circuit that counts how many times the user has done this. The output should look like this:



Include a way to reset the counter in your design, that is, a way to take the output back to zero at the flip of a switch. You may use push-button or regular switches.

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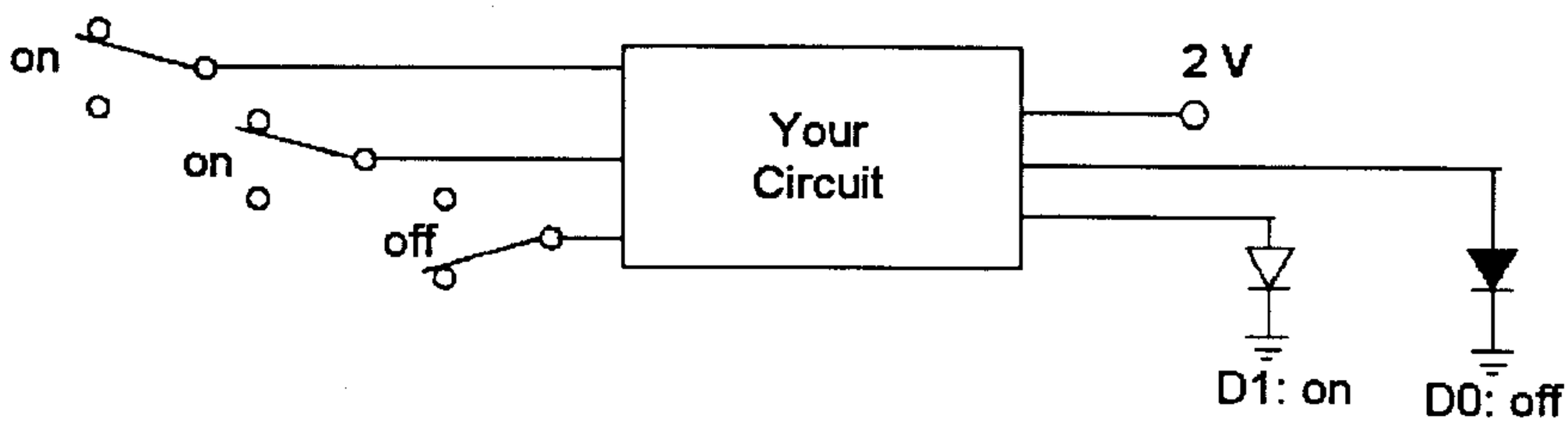
c) You are given 3 ordinary switches which can be in the "on" position or the "off" position. Create a circuit that counts the number of switches that are "on" and provides output:

1) in binary (LED's that represent the binary number of "on" switches)
2) and as an analog voltage (output 0 V for 0 switches on, 1 V for 1 switch on, 2 V for 2 switches on, 3 V for 3 switches on).

Example:

2 switches turned on, so binary output is 10 and analog output is 2 V:



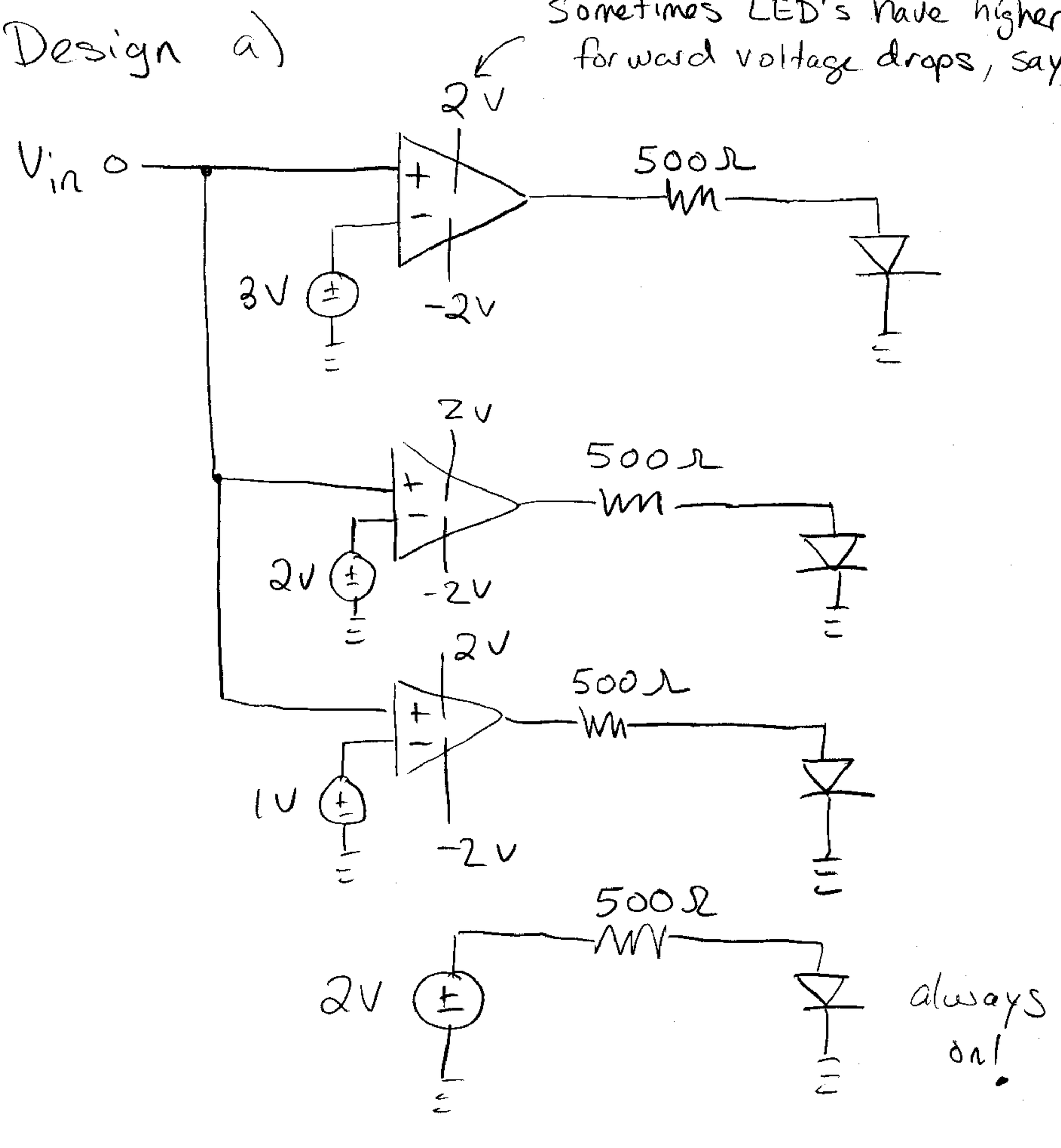
(You would have to attach something to the on/off terminals on each switch to make this work, that is not shown here for simplicity).

Name: Solutions

Problem 7 Workspace

Design a)

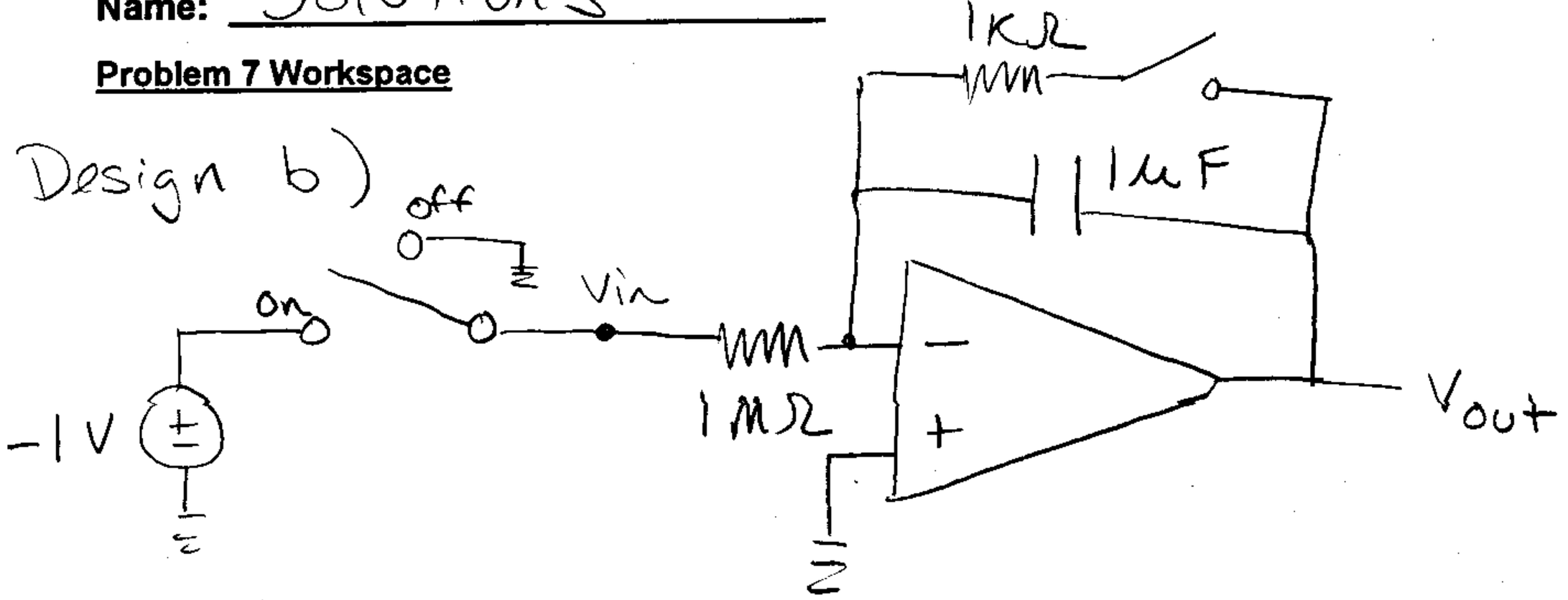
Sometimes LED's have higher forward voltage drops, say ≈ 1 V.



This is just one of many possible designs.

Name: Solutions

Problem 7 Workspace



On the integrator,

$$V_{out} = -\frac{1}{RC}\int_0^t V_{in}(t')\,dt'$$

So making $RC = 1s$ accomplishes our needs.

Note:

- When resetting circuit, make $V_{in} = 0V$. You could attach an override switch that makes $V_{in} = 0V$ when reset switch down.
- Try to choose small capacitance to make reset time constant small. If you do this with small reset resistance, current will be high.
- Operation continues normally until V_{out} hits a rail. Make the rail your max counter value.

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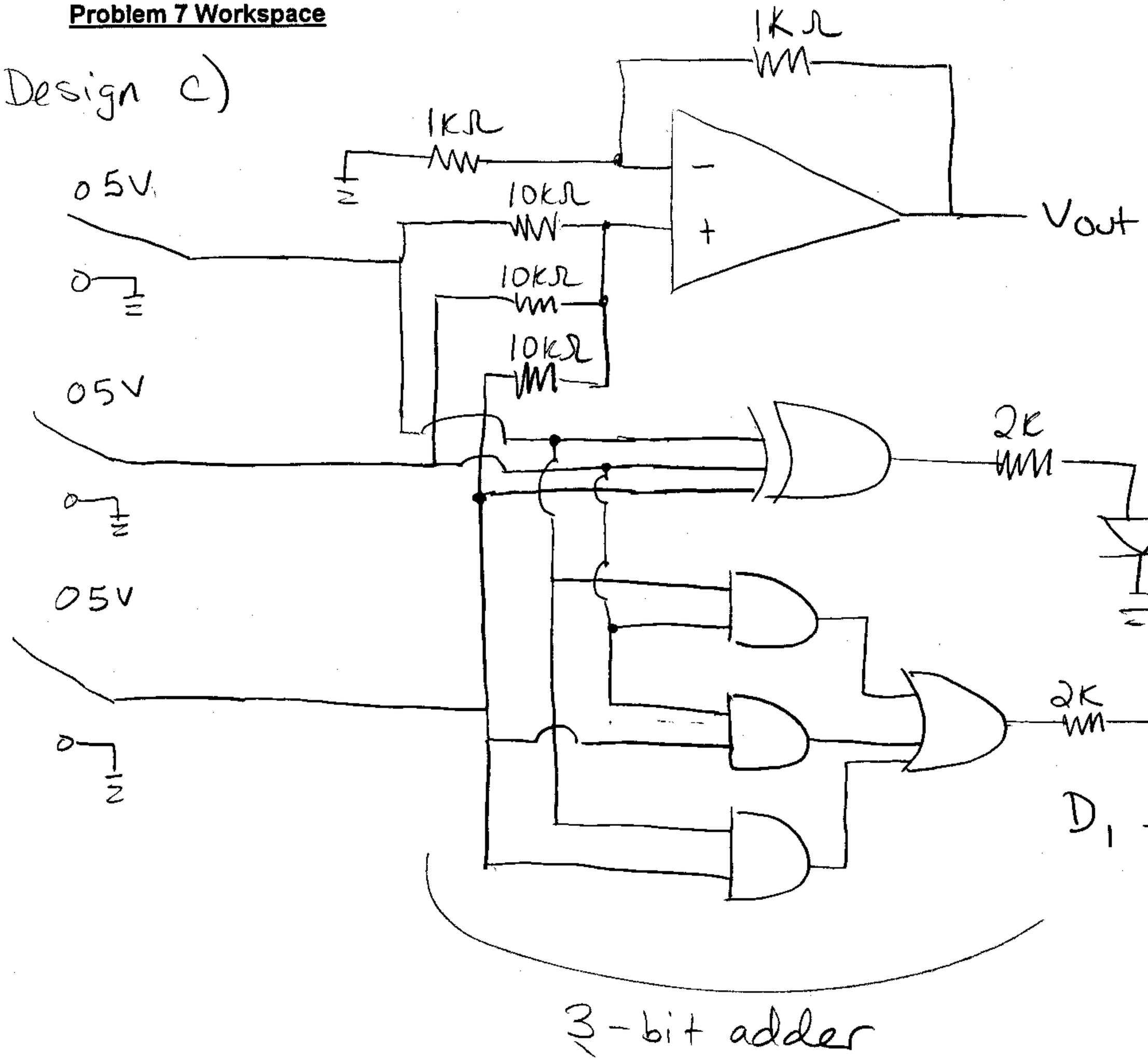
Problem 7 Workspace



You should avoid using logic voltages below 3V Unless you have special technology.