UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS 40 Fall 2003
Introduction to Microelectronic Circuits Prof. King

FINAL EXAMINATION

December 10, 2003
Time allotted: 2 hours 50 minutes (170 minutes)

NAME: _____, _____
(print) **Last** **First**

Signature: _____ **STUDENT ID#:** _____

1. This is a **CLOSED BOOK** exam. However, you may use 3 sheets of notes and a calculator.
2. **SHOW YOUR WORK or REASONING** on this exam.
   (Make your methods clear to the grader.)
3. **Write your answers clearly (legibly) in the spaces (lines, boxes, or plots) provided.**
4. Remember to specify the units on answers whenever appropriate.

SCORE: **1** _____ **/ 20**

2 _____ **/ 20**

3 _____ **/ 20**

4 _____ **/ 20**

5 _____ **/ 20**

6 _____ **/ 20**

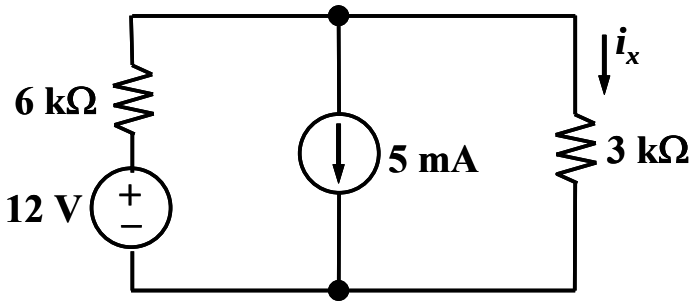
7 _____ **/ 20**

8 _____ **/ 10**

Total: _____ **/ 150**

Problem 1: Circuit Analysis and Equivalent Circuits [20 points in total]

a) Consider the following circuit:



i) Use a source transformation in order to find i_x. **[6 pts]**

i_x = _____

ii) What is the power developed/absorbed by the 5 mA current source? **[3 pts]**

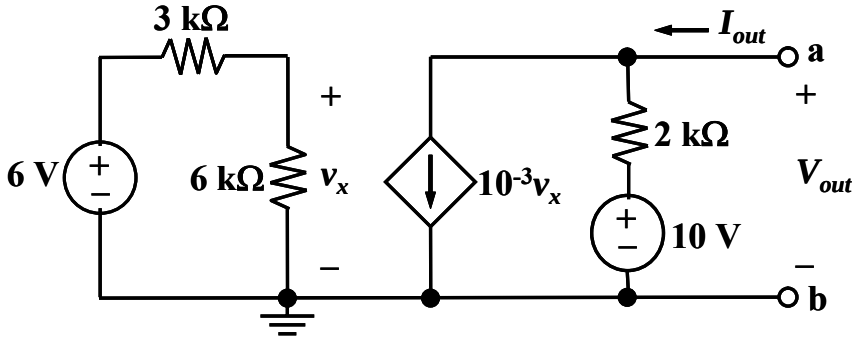
Power = _____

[developed, absorbed]

(circle the correct choice)

Problem 1 (continued)

b) Consider the following circuit:

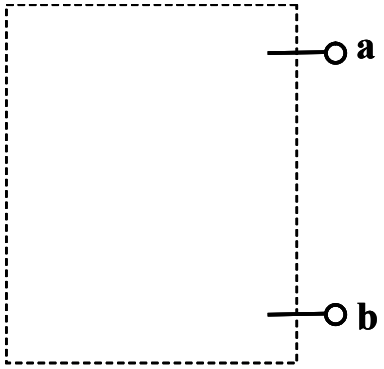


i) Find V_{out}. **[6 pts]**

V_{out} = _____

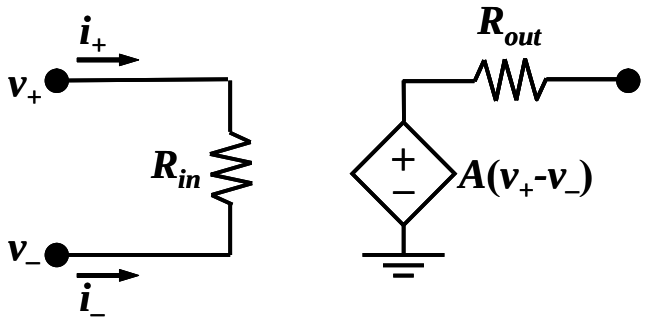
ii) Draw the Thevenin Equivalent circuit. **[5 pts]**

Thevenin Equivalent Circuit:



Problem 2: Op Amp Circuit [20 points in total]

a) The following is the circuit model for an op amp circuit operating in its linear region:

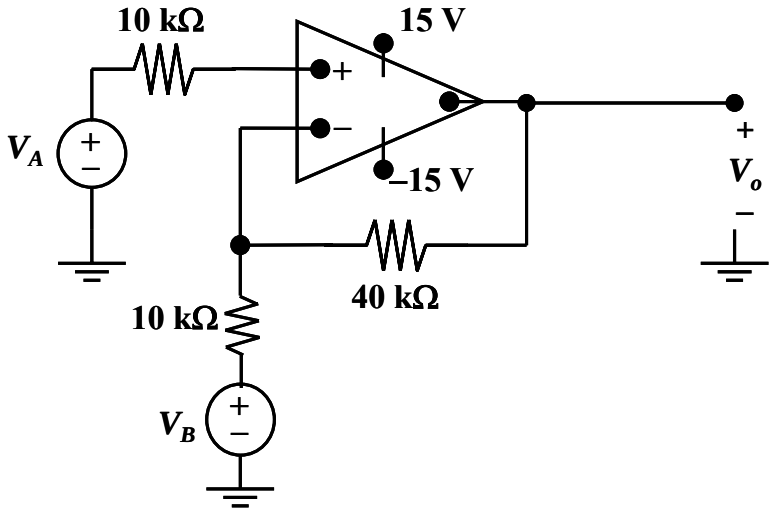


Typically, R_{in} is very large (~1 MΩ), A is very large (>10^4), and R_{out} is very small (<100 Ω).

What type of feedback is used in an op amp circuit, in order to ensure that the op amp will operate in its linear region? Illustrate (with a simple diagram) how this is achieved. **[5 pts]**

Problem 2 (continued)

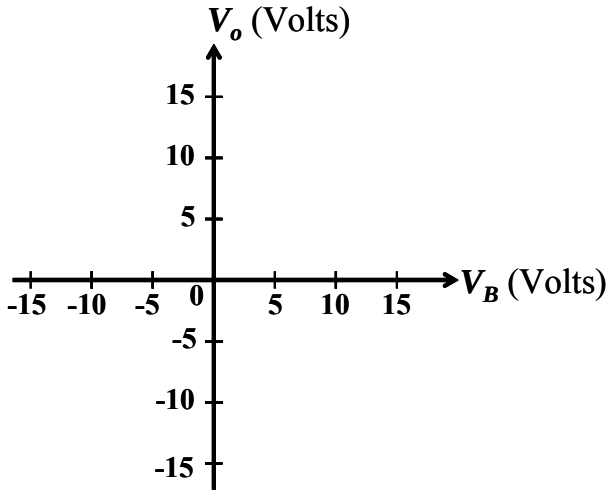
b) Consider the following op amp circuit below. You can assume that the op amp is ideal.



i) Find an expression for V_o, using superposition. **[10 pts]**

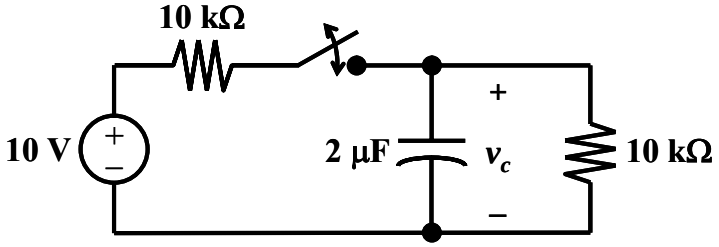
V_o = _____

ii) Suppose V_A is fixed at 1 Volt. Plot V_o vs. V_B. **[5 pts]**



Problem 3: First-Order Circuits [20 points in total]

In the circuit below, the switch is open for all $t < 0$. The switch is closed at $t = 0$, and then it is opened again at $t = 10$ ms.



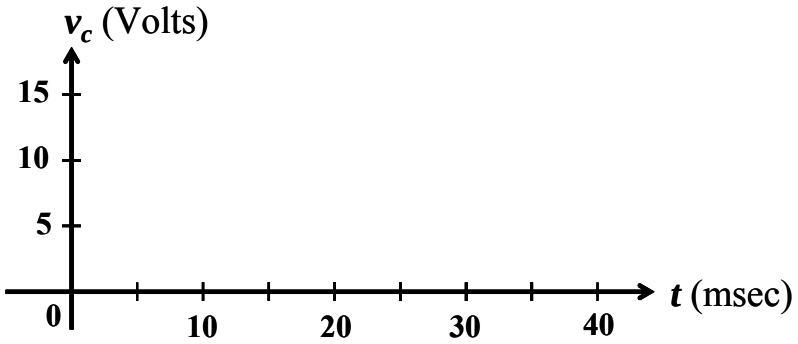
i) Write an equation for $v_c(t)$, for $0 \le t \le 10$ ms. **[8 pts]**

$0 \le t \le 10$ ms: $v_c(t) =$ _____

ii) Write an equation for $v_c(t)$, for $t > 10$ ms. **[8 pts]**

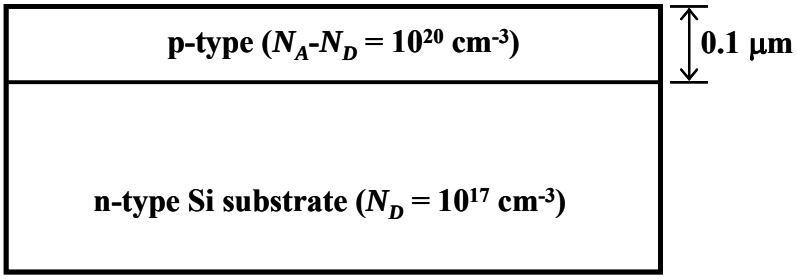
$t > 10$ ms: $v_c(t) =$ _____

iii) Sketch $v_c(t)$ for $t > 0$ **[4 pts]**



Problem 4: pn junctions; diodes [20 points in total]

a) Consider a pn junction formed in the surface of an n-type silicon wafer maintained at T = 300K. The p and n regions are uniformly doped, as indicated in the figure below:



Schematic cross-sectional view of pn junction

In the p-type region, the electron mobility is 100 cm^2/V•s and the hole mobility = 50 cm^2/V•s

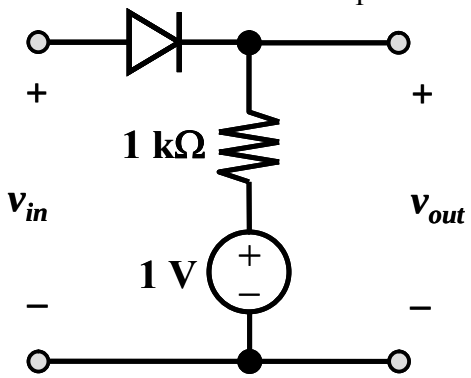
i) Estimate the sheet resistance of the p-type region. **[6 pts]**
(Use the following values of constants: $q = 1.6\times10^{-19}$ C, $n_i = 10^{10}$ cm^{-3})

Sheet resistance = _____

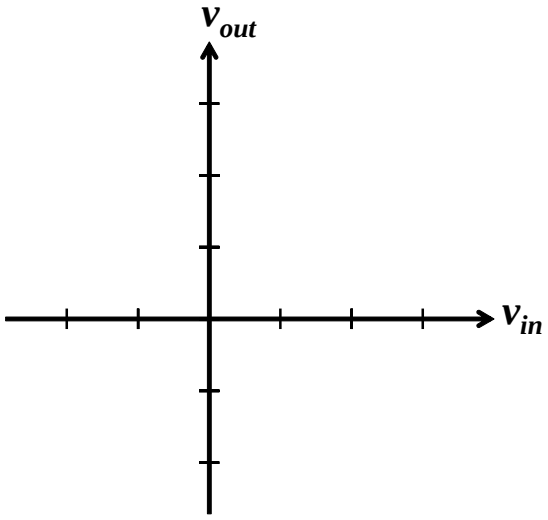
ii) Suppose the p-type region serves as the drain region of a p-channel MOSFET in a CMOS inverter, and that the n-type substrate is therefore biased at the power-supply voltage V_{DD}. How will the pn-junction capacitance change as the PMOSFET is turned on (so that the drain bias is changed from 0 V to V_{DD})? Explain briefly. **[4 pts]**

Problem 4 (continued)

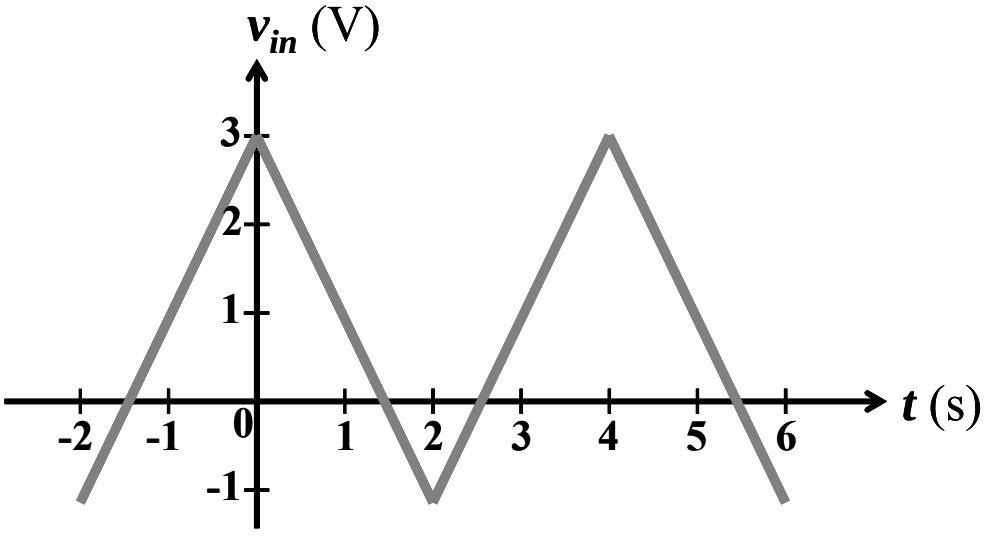
b) Consider the diode circuit below. Assume the diode is a perfect rectifier.



i) Plot v_{out} *vs.* v_{in}. **[5 pts]**



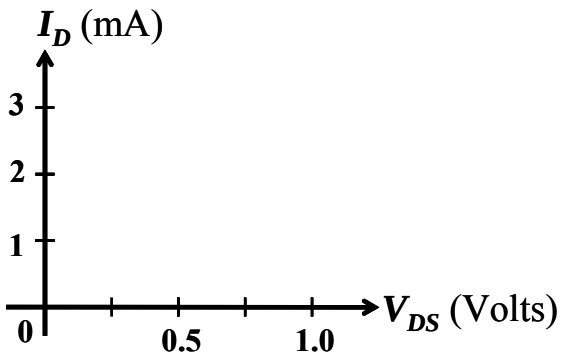
ii) Sketch v_{out} for the given $v_{in}(t)$, using the same axes. **[5 pts]**



Problem 5: MOSFET [20 points in total]

a) Consider an NMOSFET with parameters $W = 1\ \mu m$, $L = 0.1\ \mu m$, $k_n' = 10^{-3}\ A/V^2$, $V_T = 0.5V$, biased at $\boldsymbol{V_{GS} = V_{DD} = 1\ V}$. The areal gate capacitance $C_{ox} = 3\times10^{-6}\ F/cm^2$.

i) Accurately sketch the I_D *vs.* V_{DS} characteristic in the range $0 \le V_{DS} \le 1$ V, neglecting velocity saturation and channel-length modulation. Indicate the numerical values for the saturation voltage (V_{DSAT}) and current (I_{DSAT}). **[6 pts]**



ii) Estimate the effective resistance of this MOSFET (for digital circuit applications). (Again, assume that velocity saturation and channel-length modulation can be neglected. **[3 pts]**

iii) On the same plot in part (i) above, accurately sketch and label the I_D *vs.* V_{DS} characteristic, taking into account that the electron velocity in the MOSFET channel saturates at 10^7 cm/s. **[5 pts]**

Problem 5 (continued)

b) High drive current (I_{DSAT}) is desirable for reduced equivalent resistance, to achieve smaller propagation delay to allow higher-speed circuit operation. Indicate in the table below how you would adjust various MOSFET parameters so as to increase I_{DSAT}. Briefly describe the tradeoff or disadvantage involved, if any, for each. (For example, the answer for gate length L is given.) **[6 pts]**

MOSFET Parameter	**To increase I_{DSAT}, parameter must be**	**Associated tradeoff or disadvantage**
Gate length L	**decreased**	Subthreshold leakage current increases, so that static power dissipation increases
Threshold voltage V_T		
Channel width W		

Problem 6: Logic Circuits [20 points in total]

a) Given the following truth table for the logic function **F**:

A	B	F
0	0	1
0	1	0
1	0	1
1	1	1

i) Write a simple logic expression for **F**. **[2 pts]**

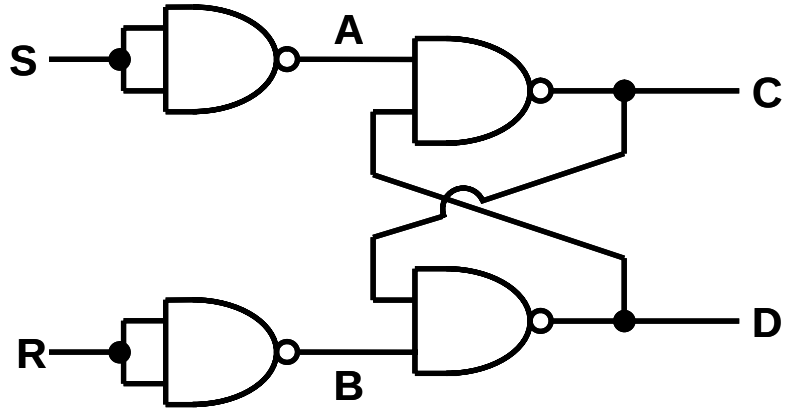
F = _____

ii) Implement the function **F**, using only 2-input NAND gates. **[5 pts]**

Logic circuit for F:

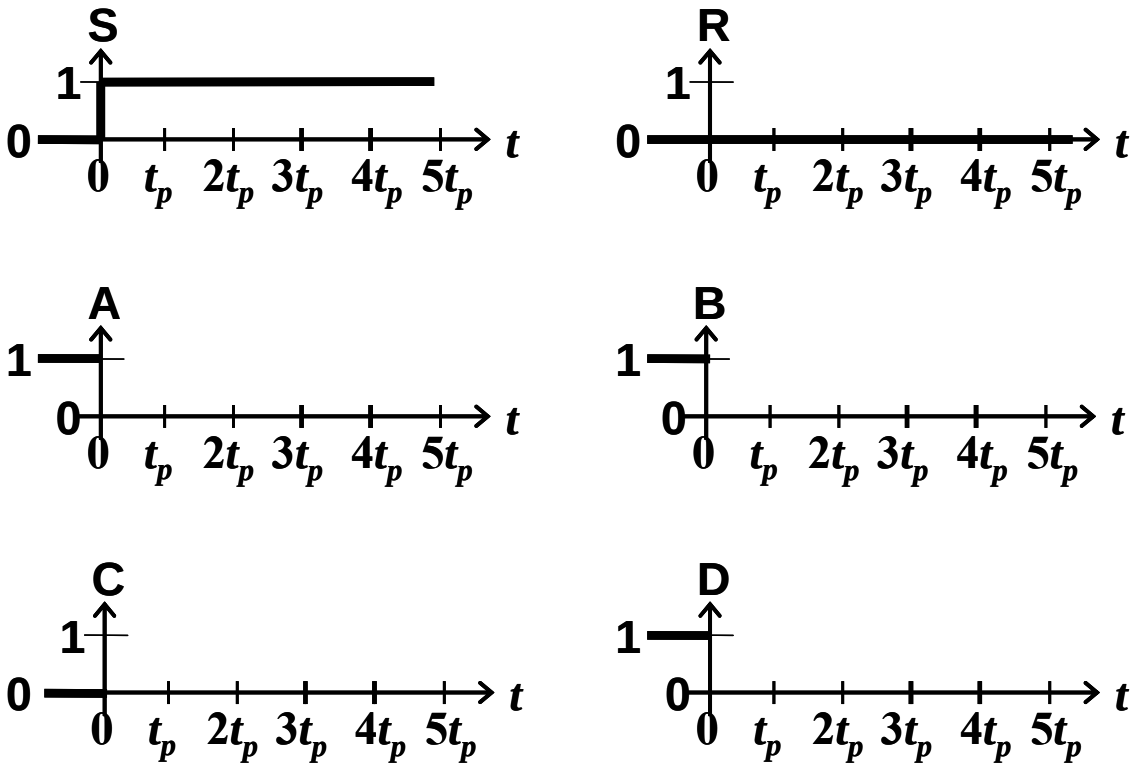
Problem 6 (continued)

b) Consider the S-R flip-flop circuit below:

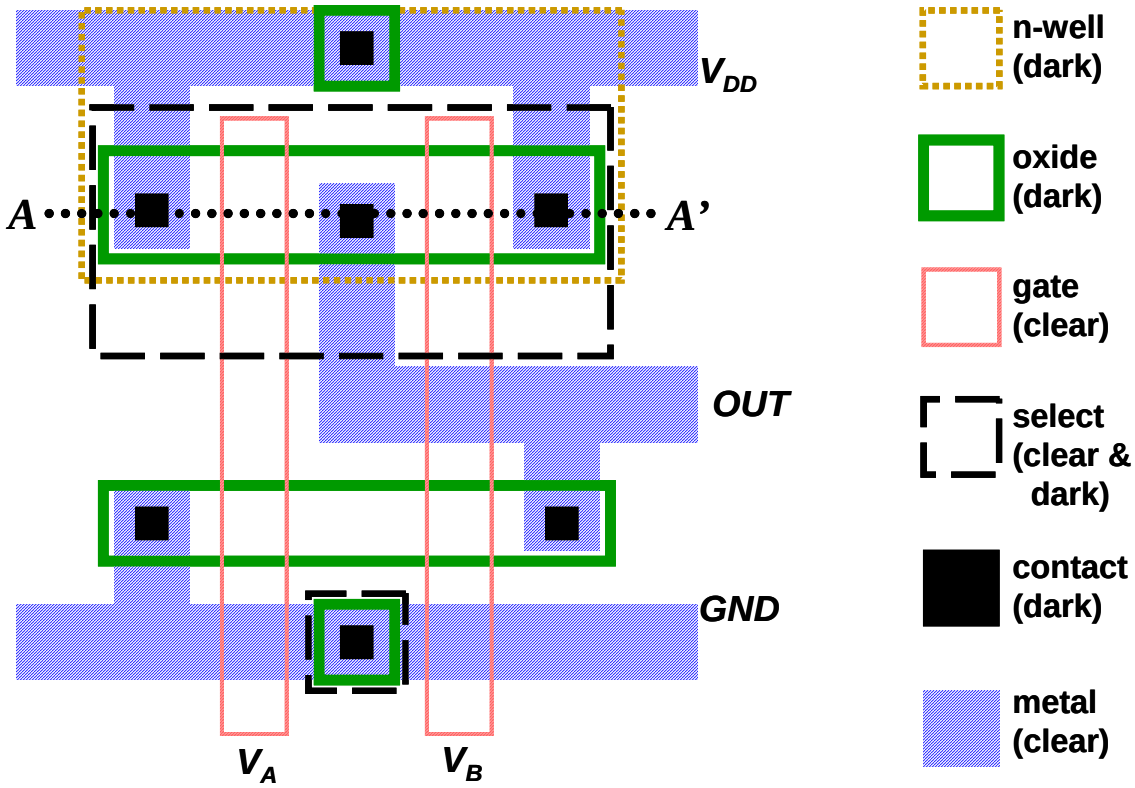


The output C is initially equal to 0, and the output D is initially equal to 1.

For the given **S** and **R** timing diagrams below, draw the timing diagrams (for $t > 0$) for **A**, **B**, **C**, and **D** on the plots provided. **[13 pts]**



Problem 7: CMOS Technology [20 points in total]
The layout of a CMOS logic gate is shown below:

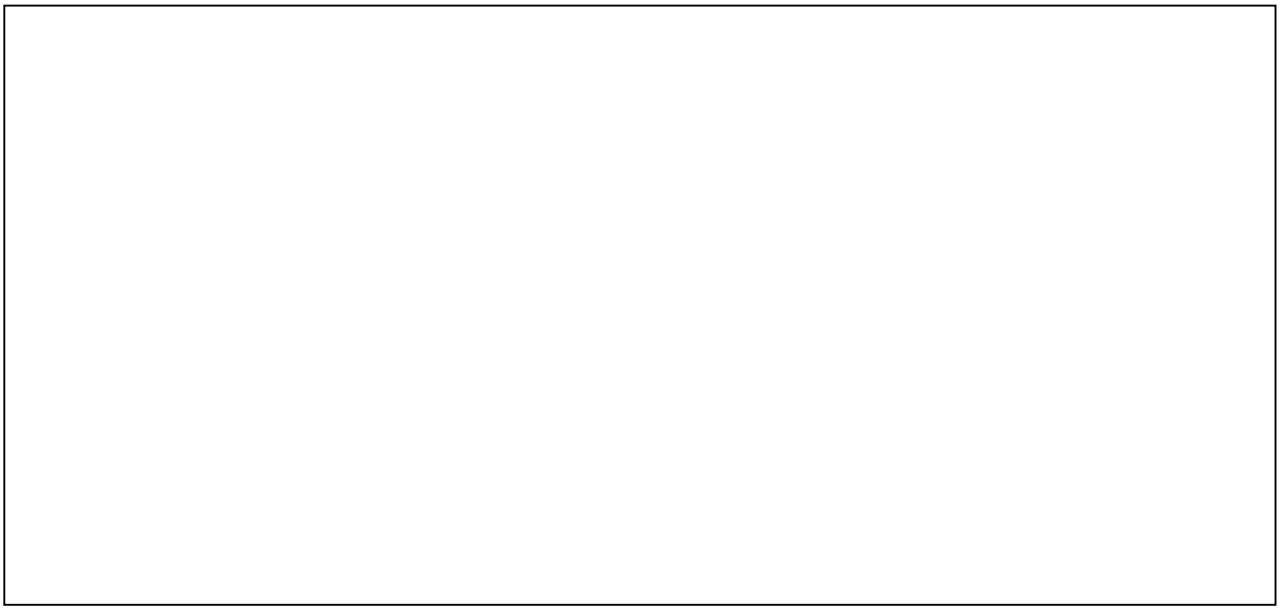


The following fabrication process (starting with a p-type Si wafer) is used:

1. Thermally grow 700 nm of SiO_2.
2. Pattern the SiO_2 using the n-well mask.
3. Implant phosphorus and perform a high-temperature, long anneal to "drive in" the well to a depth of 1 μm.
4. Remove the SiO_2 (using a highly selective wet etch process which does not etch Si).
5. Grow 0.5 μm of SiO_2 ("field oxide").
6. Pattern the SiO_2 using the oxide mask.
7. Thermally grow 10 nm of SiO_2 ("gate oxide") in the bare regions of the Si.
8. Deposit 200 nm of poly-Si (by CVD).
9. Pattern the poly-Si using the gate mask.
10. Use clear-field select mask to pattern photoresist; implant phosphorus. This will form the n+ source and drain junctions for the n-channel MOSFETs.
11. Use dark-field select mask to pattern photoresist; implant boron. This will form the p+ source and drain junctions for the p-channel MOSFETs.
12. Thermally anneal the wafer in order to activate the implanted dopants. The final source/drain junction depth is 100 nm.
13. Deposit 0.5 μm of SiO_2 ("passivation oxide").
14. Pattern the deposited SiO_2 using the contact mask.
15. Deposit 0.5 μm of aluminum.
16. Pattern the aluminum using the metal mask.

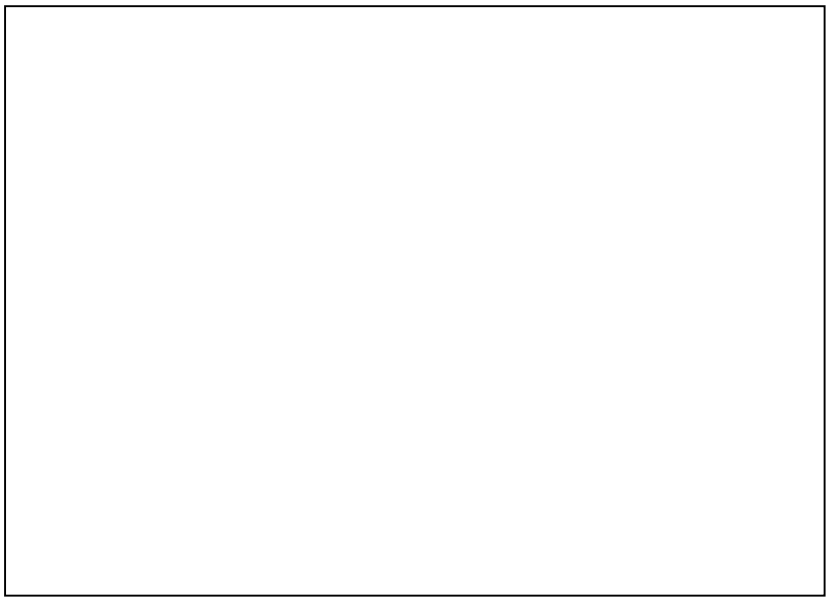
Problem 7 (continued)

a) Draw cross-section *A*-*A*′ in the space provided. Identify all layers clearly. **[10 pts]**



Cross-section *A*-*A*′

b) Draw the circuit schematic, labeling V_{DD}, *GND*, V_A, V_B, and *OUT*. **[5 pts]**



Circuit Schematic

c) Assuming that $k_n' = 3k_p'$, would you expect this logic gate to have comparable worst-case "pull-up"and "pull-down" propagation delays? (Is $t_{pLH} \cong t_{pHL}$?) Justify your answer. **[5 pts]**

Problem 8: Technology Scaling (Short-Answer Questions) [10 points in total]

a) Explain how transistor scaling improves both the cost (per function) and performance (circuit operating speed) of CMOS integrated circuits. **[5 pts]**

b) Explain why interconnect delay is becoming more of a concern as CMOS technology advances. **[5 pts]**