# UNIVERSITY OF CALIFORNIA, BERKELEY <br> College of Engineering <br> Department of Electrical Engineering and Computer Sciences 

EECS 40
Spring 2000
Introduction to Microelectronic Devices
MIDTERM EXAMINATION \#1
Time allotted: 80 minutes

NAME:
(print)
Last
First
Signature

## STUDENT ID\#:

$\qquad$

1. This is a CLOSED BOOK EXAM. However, you may use 1 page of notes and a calculator.
2. Show your work on this exam.

MAKE YOUR METHODS CLEAR TO THE GRADER.
3. Write your answers clearly in the spaces (lines, boxes or plots) provided. Numerical answers must be accurate to within $\mathbf{1 0 \%}$ unless otherwise noted.
4. Remember to specify the units on answers whenever appropriate.
5. Do not unstaple the pages of this exam.

SCORE:
1 $\qquad$ / 20

2 / 30

3 $\qquad$ / 25

4 $\qquad$ / 25

Total: $\qquad$ / 100

## Problem 1: Logic Gates and Timing Diagrams [25 points]

Consider the following digital logic circuit:

a) Fill out the truth table for the logic function G. [8 pts]

| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{G}$ |
| :---: | :---: | :---: |
| $\mathbf{0}$ | $\mathbf{0}$ |  |
| $\mathbf{0}$ | $\mathbf{1}$ |  |
| $\mathbf{1}$ | $\mathbf{0}$ |  |
| $\mathbf{1}$ | $\mathbf{1}$ |  |

b) Write a simple logical expression for the function G. [5 pts]

$$
\mathrm{G}=
$$

$\qquad$
c) How many unit gate delays are there between the inputs (A and B) and the output (G)? [2 pts] (In other words, how many unit gate delays must you wait, after changing A and/or B, before you can trust the value of $G$ to be valid?)


## Problem 1 (continued)


d) Assume each logic gate has a unit gate delay $\tau=100 \mathrm{ps}$.

Draw the timing diagrams for $t=0$ to $t=700 \mathrm{ps}$, for the given logic input values A and B. [ $\mathbf{1 0} \mathbf{~ p t s}]$

logic value of B

logic value of $\mathbf{C}$

logic value of $\mathbf{D}$

logic value of $\mathbf{E}$

logic value of $\mathbf{F}$


## Problem 2: Resistive Circuits [30 points]

a) Find the equivalent resistance $R_{a b}$ for the following circuit. [ $\mathbf{6} \mathbf{~ p t s}$ ]

 ply of $10 \mathrm{k} \Omega$ resistors. Being a clever Cal student, how would you connect several $10 \mathrm{k} \Omega$ resistors together, to achieve a $6 \mathrm{k} \Omega$ resistance? [ 7 pts ]

Circuit diagram of $10-\mathrm{k} \Omega$ resistors connected to give $R_{c d}=6 \mathrm{k} \Omega$ :


## Problem 2 (continued)

c) Consider the following circuit:

$R_{1}=1 \mathrm{k} \Omega$
$R_{2}=2 \mathrm{k} \Omega$
$R_{3}=2 \mathrm{k} \Omega$
i) Find $V_{c d}$. $[\mathbf{3} \mathbf{~ p t s}]$

ii) Find the power developed/absorbed by the current source, $P_{I}$. [3 pts]

| $P_{I}=$ |
| ---: |
| [developed, absorbed] |
| (circle correct choice) |

iii) Indicate in the table below (by checking the appropriate boxes) how various circuit parameters would change if the terminals $\mathbf{c}$ and $\mathbf{d}$ were to be shorted together. Justify your answers. [ $\mathbf{6} \mathbf{~ p t s ]}$

| Parameter | Value will: |  | Brief Explanation/Justification |  |
| :--- | :--- | :--- | :---: | :--- |
|  | increase | decrease |  |  |
| $V_{b d}$ |  |  |  |  |
| $I_{l}$ |  |  |  |  |
| Power developed <br> by voltage source |  |  |  |  |

iv) What is the value of $I_{3}$ when the terminals $\mathbf{c}$ and $\mathbf{d}$ are shorted together? [ $\mathbf{5} \mathbf{p t s}$ ]


## Problem 3: Nodal Analysis [20 points]

a) In the circuit below, the independent source values and resistances are known.

Use the nodal analysis technique to write 3 equations sufficient to solve for $V_{a}, V_{b}$, and $V_{c}$. To receive credit, you must write your answer in the box below. [10 pts]
DO NOT SOLVE THE EQUATIONS!


Write the nodal equations here:

|  |
| :--- |
| $\square$ |

## Problem 3 (continued)

b) Similarly to part (a), use the nodal analysis technique to write 3 equations sufficient to solve for $V_{a}, V_{b}$, and $V_{c}$. To receive credit, you must write your answer in the box below. [10 pts] DO NOT SOLVE THE EQUATIONS!


Write the nodal equations here:

| $\square$ |
| :--- |
| $\square$ |

## Problem 4: Thevenin and Norton Equivalent Circuits [25 points]

a) Find the Thevenin Equivalent Circuit for the following circuit. [10 pts]

b) Use the source transformation method to obtain the Norton Equivalent Circuit for the circuit in part (a). [5 pts]


## Problem 4 (continued)

c) The Thevenin Equivalent Circuit for a certain linear circuit is given below. Plot the current (I) versus the output voltage $(\boldsymbol{V})$ for the circuit, labelling the $\mathbf{y}$-intercept and $\mathbf{x}$-intercept. [ $\mathbf{5} \mathbf{p t s}$ ]

Thevenin Equivalent Circuit


d) The circuit in part (c) is connected to a $1 \mathrm{k} \Omega$ load resistor (placed between the terminals $\mathbf{a}$ and b). Find the power absorbed in the load resistor, $P_{1 k}$ [ $\mathbf{5} \mathbf{~ p t s ]}$


