UNIVERSITY OF CALIFORNIA, BERKELEY
College of Engineering
Department of Electrical Engineering and Computer Sciences

EECS 40 — Spring 2000
Introduction to Microelectronic Devices — Prof. King

MIDTERM EXAMINATION #2

April 6, 2000
Time allotted: 80 minutes

NAME: ______________________________ ____________________
(print) Last First Signature

STUDENT ID#:____________________

1. This is a **CLOSED BOOK EXAM**. However, you may use 2 pages of notes and a calculator.
2. Show your work on this exam.
   MAKE YOUR METHODS CLEAR TO THE GRADER.
3. **Write your answers clearly in the spaces (lines, boxes or plots) provided. Numerical answers must be accurate to within 10% unless otherwise noted.**
4. Remember to specify the units on answers whenever appropriate.
5. **Do not unstaple the pages of this exam.**

SCORE:

1 __________ **/ 20**

2 __________ **/ 30**

3 __________ **/ 25**

4 __________ **/ 25**

Total: __________ **/ 100**

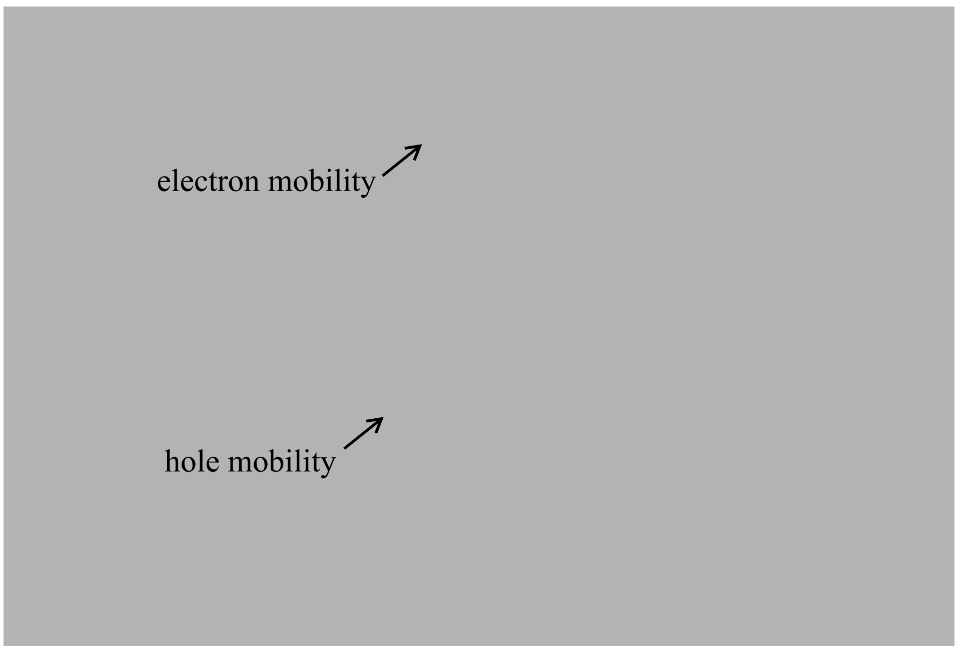
Physical Constants

Description	Symbol	Value
Electronic charge	q	1.602×10^{-19} C
Permittivity of vacuum	ε_o	8.854×10^{-14} F/cm
Boltzmann's constant	k	8.62×10^{-5} eV/K
Thermal voltage at 300K	kT/q	0.026 V

Properties of Silicon at 300K

Description	Symbol	Value
Thermal velocity	v_{th}	10^7 cm/s
Relative permittivity	ε_r	11.7
Intrinsic carrier density	n_i	1.45×10^{10} cm^{-3}

Electron and Hole Mobilities in Silicon at 300K



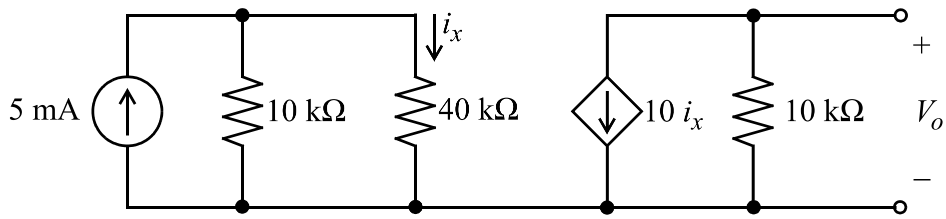
Conversion Factors

1 eV = 1.602×10^{-19} J
1 μm = 10^{-4} cm = 10^{-6} m

Farad = Coulomb / Volt
Henry = Volt / (Ampere/second)
Watt = Volt x Ampere
Joule = Watt x second

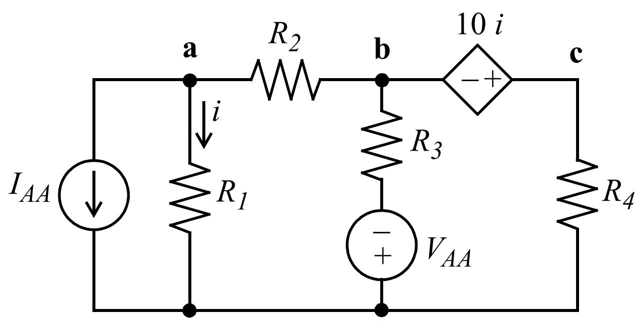
Problem 1 **Circuits with Dependent Sources [20 points]**

a) Find V_o. **[4 pts]**



V_o = __________ V

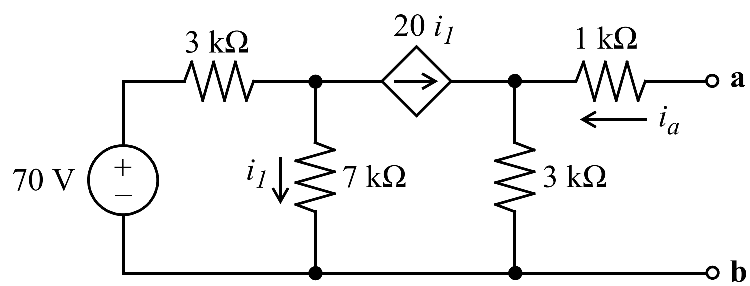
b) In the circuit below, the independent source values and resistances are known.
Use the **nodal analysis technique** to write **3 equations sufficient to solve for V_a, V_b, and V_c**.
To receive credit, you must write your answer in the box below. **[6 pts]**
DO NOT SOLVE THE EQUATIONS!



Write the nodal equations here:

<u>Problem 1</u> (continued)

c) Consider the following circuit:



i) Find the voltage V_{ab}. **[5 pts]**

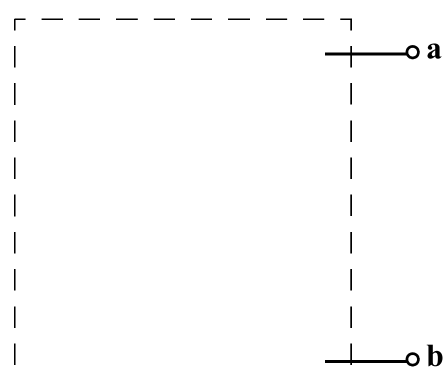
V_{ab} = ___________ V

ii) What is the current i_a when the terminals **a** and **b** are shorted together? **[3 pts]**

i_a = ___________ A

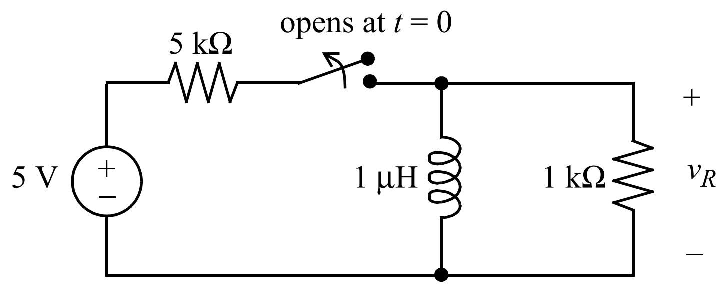
iii) Draw the Thevenin Equivalent Circuit. **[2 pts]**

Thevenin Equivalent Circuit:



<u>Problem 2</u>: Transient Response [30 points]

a) In the circuit below, the switch has been in the closed position for a long time.



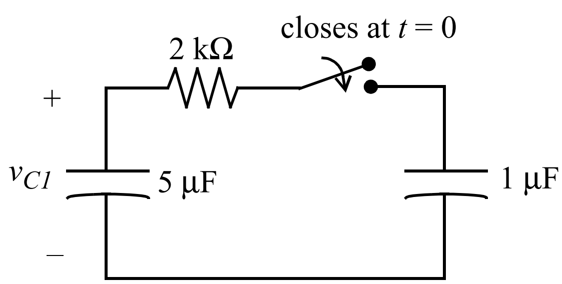
i) Find the value of v_R just after the switch opens ($t = 0^+$). **[3 pts]**

$v_R\ (0^+) =$ __________ V

ii) How much energy is dissipated in the 1 kΩ resistor after the switch is opened? **[2 pts]**

Energy dissipated = __________ J

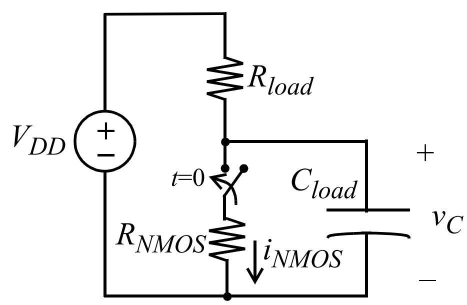
b) In the circuit below, the 5 µF capacitor is initially charged to 5 V ($v_{C1}(0^-) = 5$ V). (The 1 µF capacitor is initially uncharged.) The switch is then closed at time $t = 0$. What is the final value of v_{C1}? **[5 pts]**



Final value of $v_{C1} =$ __________ V

Problem 2 **(continued)**

c) The following is a circuit model for an NMOS inverter, in which the transistor is turned on at time $t = 0$:



$V_{DD} = 5$ V
$R_{load} = 90$ kΩ
$R_{NMOS} = 10$ kΩ
$C_{load} = 10$ nF

i) What is the value of v_C at $t = 0^-$? **[3 pts]**

$v_C(0^-) =$ __________ V

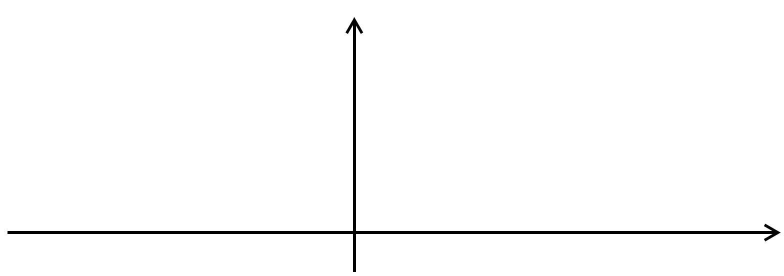
ii) What is the value of i_{NMOS} at $t = 0^+$? **[3 pts]**

$i_{NMOS}(0^+) =$ __________ A

iii) What is the final value of v_C? **[3 pts]**

final value of $v_C =$ __________ V

iv) Neatly sketch the graph of i_{NMOS} **for all** $\boldsymbol{t}$, labelling the axes. **[5 pts]**



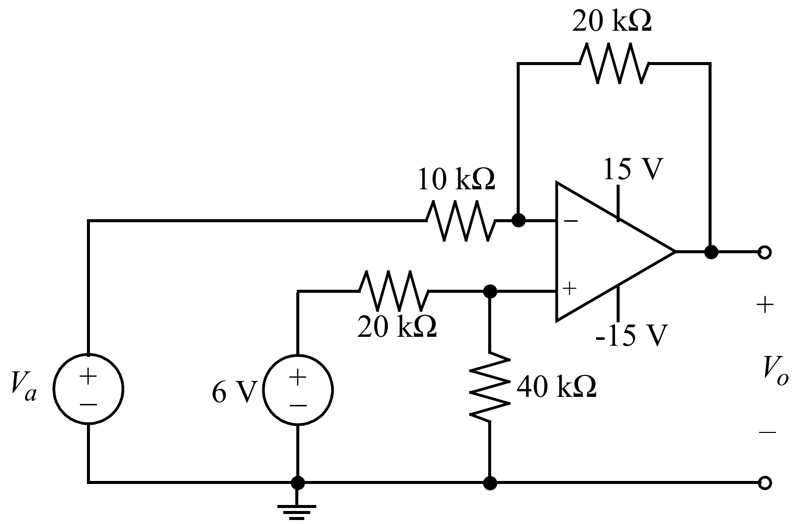
v) Write an equation for i_{NMOS} as a function of time, for $t > 0$. **[6 pts]**

Equation for i_{NMOS}: ____

Problem 3: Op-Amp Circuits [25 points]

Assume the op-amps in this problem are ideal.

a) Consider the following circuit:



i) Find an expression for V_o as a function of V_a. **[6 pts]**

Expression for V_o : ____

ii) Find V_o for V_a = 2 V. **[3 pts]**

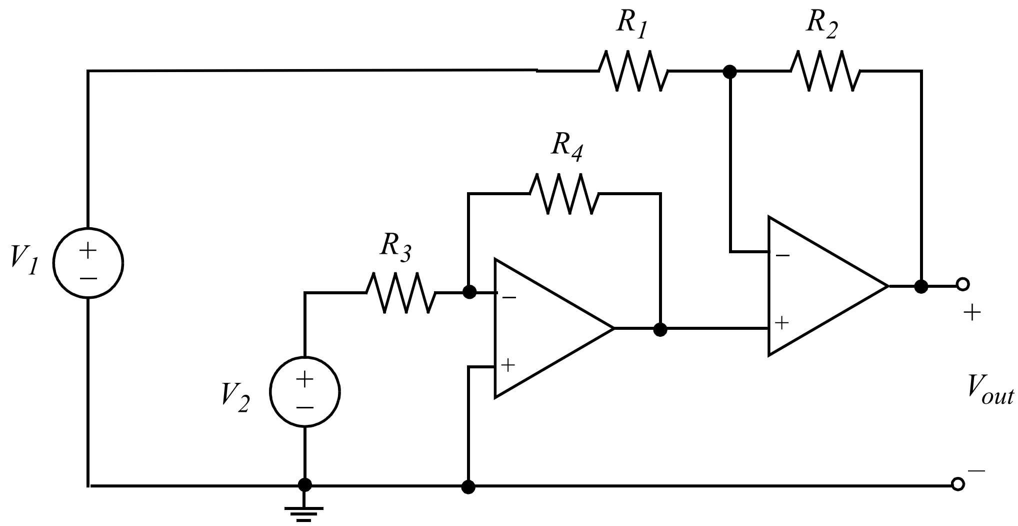
V_o = __________ V

iii) For what values of V_a will the op-amp be saturated? **[6 pts]**

Values of V_a for which the op-amp will be saturated: ________________________________

<u>Problem 3</u> (continued)

b) In the following circuit, the op-amps are operating linearly.

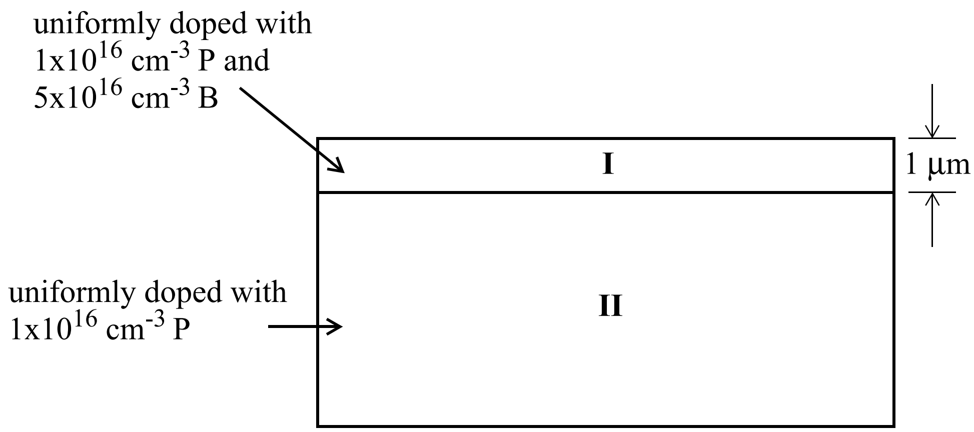


Find V_{out} in terms of V_1, V_2, R_1, R_2, R_3, R_4. **[10 pts]**
(Hint: The superposition method might be helpful here.)

V_{out} = ____

Problem 4: Semiconductor properties; p-n diodes [25 points]

a) Consider a silicon sample maintained at 300K under equilibrium conditions, uniformly doped with 1×10^{16} cm^{-3} phosphorus atoms. The surface region of the sample is **additionally** doped uniformly with 5×10^{16} cm^{-3} boron atoms, to a depth of 1 μm, as shown in the figure below.



Schematic cross-sectional view of silicon sample

i) In the figure above, indicate the type of the regions (I and II) by labelling them as "n" or "p" type. **[2 pts]**

ii) What are the electron and hole concentrations in Region I? **[5 pts]**

n = ________________ cm^{-3}

p = ________________ cm^{-3}

iii) What is the sheet resistance of Region I? **[5 pts]**

R_s = ________________ Ω/square

iv) Suppose any voltage between 0 V and 5 V can be applied to Region I. What fixed voltage ("bias") would you apply to Region II, to guarantee that no current would ever flow between Region I and Region II? **Briefly explain your answer. [3 pts]**

Region II bias voltage = _____ V

Problem 4 (continued)

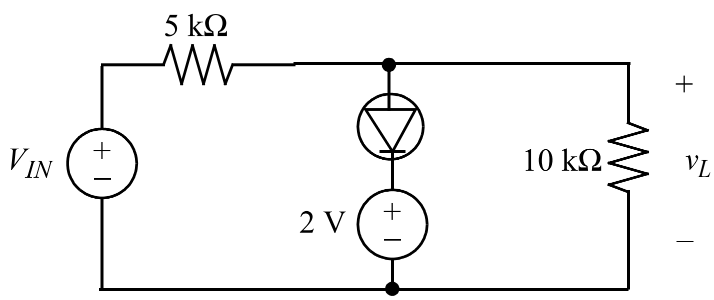
b) If a diode is operated only within a small range of forward-bias voltages, its behavior can be accurately modelled by a resistor, whose value is dependent on the bias voltage. Derive an expression for the diode "small-signal" resistance:

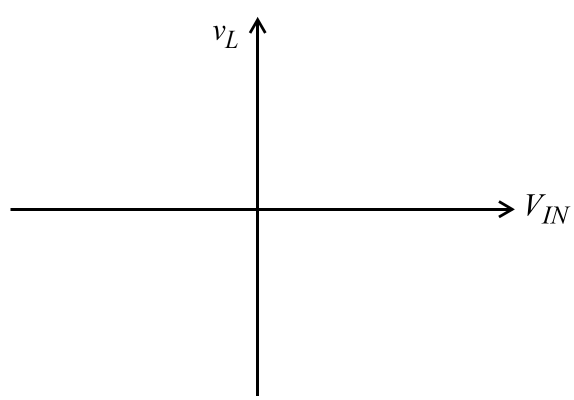
$$R_{diode} = \left(\frac{\partial I}{\partial V}\right)^{-1}$$

in terms of the saturation current I_s, the bias voltage V, and the absolute temperature T. **[5 pts]**

$R_{diode} =$ ______________________________

c) Plot v_L vs. V_{IN} for **-10 V < V_{IN} < 10 V** on the axes provided, for the circuit below. Note that the diode is a perfect rectifier. **Label the axes. [5 pts]**





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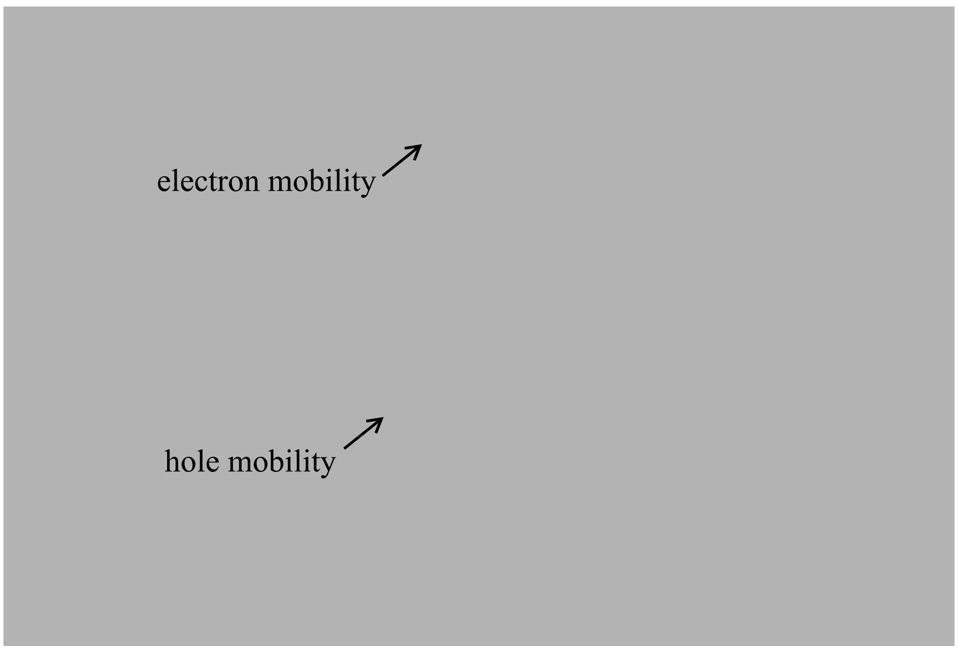

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<u>Problem 1</u> Circuits with Dependent Sources [20 points]

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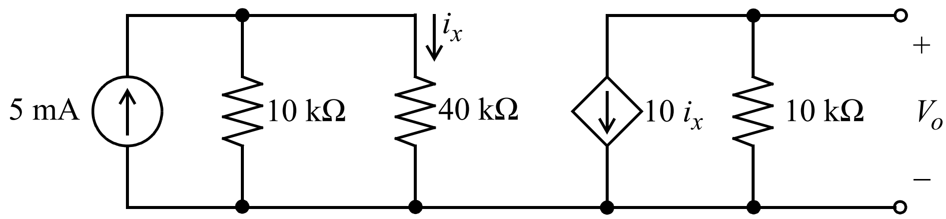

V_o = __________ V

b) In the circuit below, the independent source values and resistances are known.
Use the **nodal analysis technique** to write **3 equations sufficient to solve for V_a, V_b, and V_c.**
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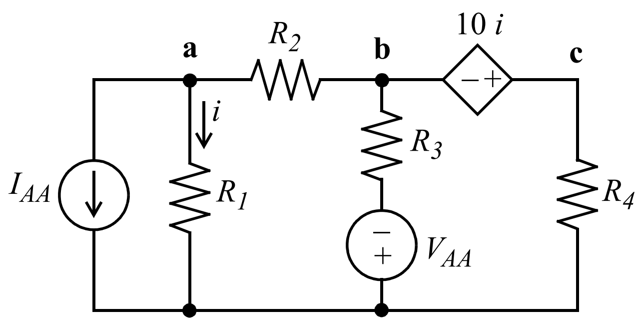


Write the nodal equations here:

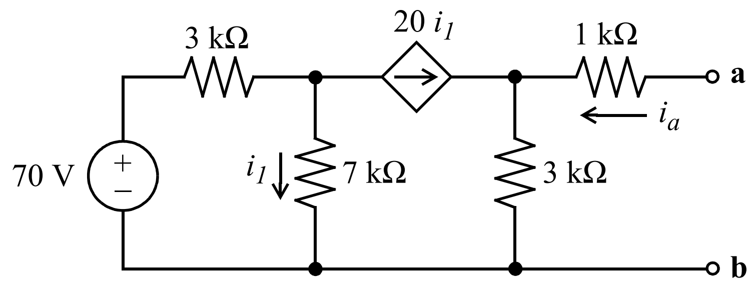
___

___

___

Problem 1 **(continued)**

c) Consider the following circuit:



i) Find the voltage V_{ab}. **[5 pts]**

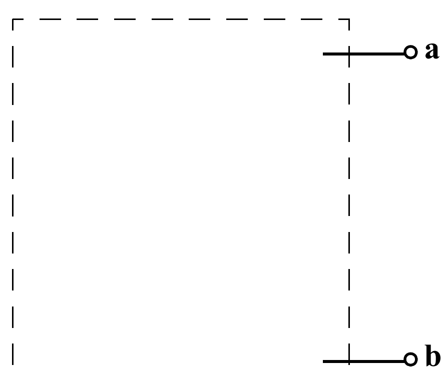
V_{ab} = ___________ V

ii) What is the current i_a when the terminals **a** and **b** are shorted together? **[3 pts]**

i_a = ___________ A

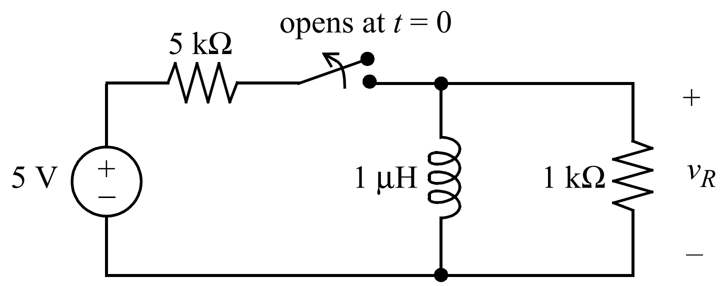
iii) Draw the Thevenin Equivalent Circuit. **[2 pts]**

Thevenin Equivalent Circuit:



Problem 2: Transient Response [30 points]

a) In the circuit below, the switch has been in the closed position for a long time.



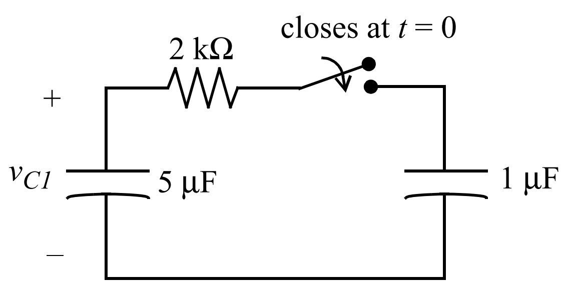
i) Find the value of v_R just after the switch opens ($t = 0^+$). **[3 pts]**

$v_R(0^+) =$ __________ V

ii) How much energy is dissipated in the 1 kΩ resistor after the switch is opened? **[2 pts]**

Energy dissipated = __________ J

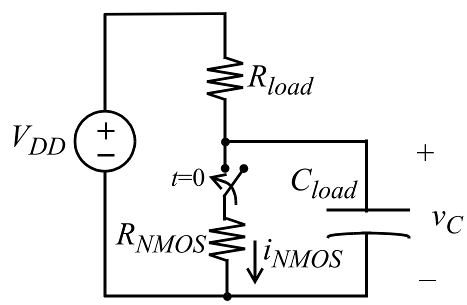
b) In the circuit below, the 5 µF capacitor is initially charged to 5 V ($v_{C1}(0^-) = 5$ V). (The 1 µF capacitor is initially uncharged.) The switch is then closed at time $t = 0$. What is the final value of v_{C1}? **[5 pts]**



Final value of $v_{C1} =$ __________ V

Problem 2 **(continued)**

c) The following is a circuit model for an NMOS inverter, in which the transistor is turned on at time $t = 0$:



$V_{DD} = 5$ V
$R_{load} = 90$ kΩ
$R_{NMOS} = 10$ kΩ
$C_{load} = 10$ nF

i) What is the value of v_C at $t = 0^-$? **[3 pts]**

$v_C(0^-) =$ ___________ V

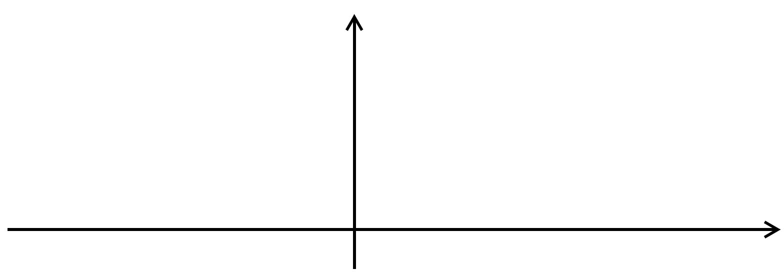
ii) What is the value of i_{NMOS} at $t = 0^+$? **[3 pts]**

$i_{NMOS}(0^+) =$ ___________ A

iii) What is the final value of v_C? **[3 pts]**

final value of $v_C =$ ___________ V

iv) Neatly sketch the graph of i_{NMOS} **for all** t, labelling the axes. **[5 pts]**



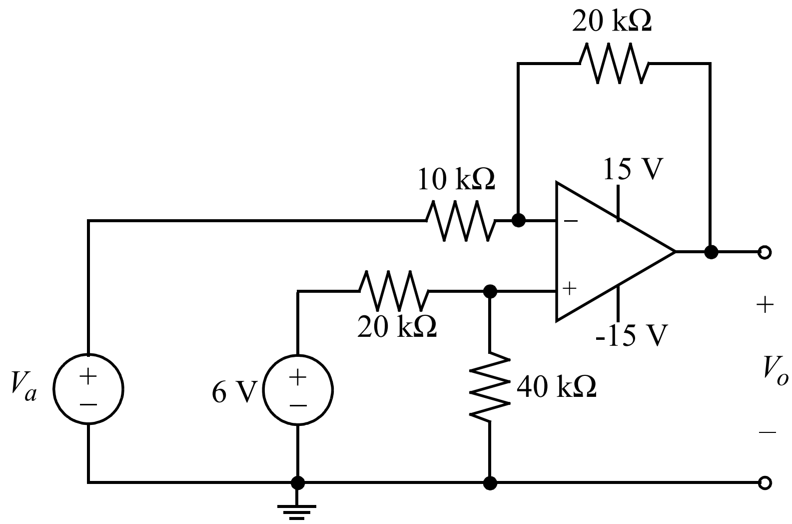
v) Write an equation for i_{NMOS} as a function of time, for $t > 0$. **[6 pts]**

Equation for i_{NMOS}: ____

<u>Problem 3</u>: Op-Amp Circuits [25 points]

Assume the op-amps in this problem are ideal.

a) Consider the following circuit:



i) Find an expression for V_o as a function of V_a. **[6 pts]**

Expression for V_o : ____

ii) Find V_o for $V_a = 2$ V. **[3 pts]**

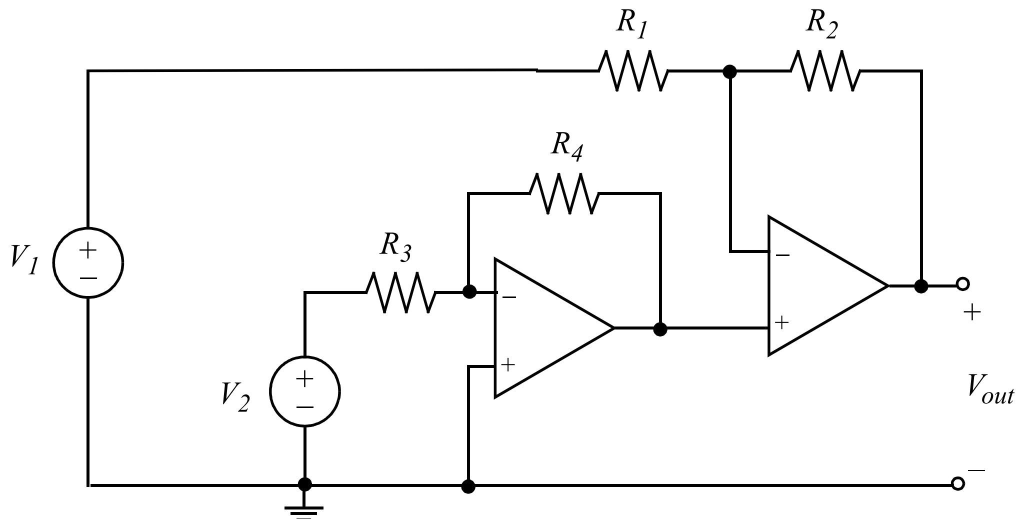
V_o = ___________ V

iii) For what values of V_a will the op-amp be saturated? **[6 pts]**

Values of V_a for which the op-amp will be saturated: ___________________________________

<u>Problem 3</u> (continued)

b) In the following circuit, the op-amps are operating linearly.

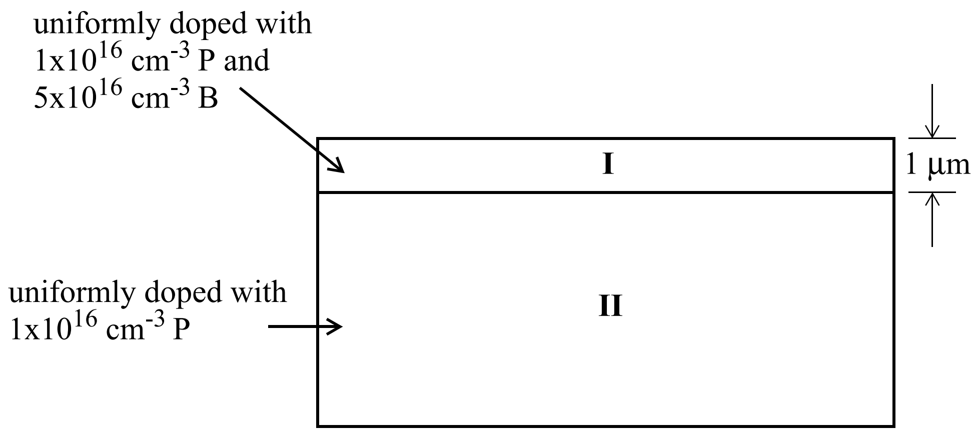


Find V_{out} in terms of V_1, V_2, R_1, R_2, R_3, R_4. **[10 pts]**
(<u>Hint</u>: The superposition method might be helpful here.)

V_{out} = ____

<u>Problem 4</u>: Semiconductor properties; p-n diodes [25 points]

a) Consider a silicon sample maintained at 300K under equilibrium conditions, uniformly doped with $1\text{x}10^{16}$ cm^{-3} phosphorus atoms. The surface region of the sample is **additionally** doped uniformly with $5\text{x}10^{16}$ cm^{-3} boron atoms, to a depth of 1 μm, as shown in the figure below.



<u>Schematic cross-sectional view of silicon sample</u>

i) In the figure above, indicate the type of the regions (I and II) by labelling them as "n" or "p" type. **[2 pts]**

ii) What are the electron and hole concentrations in Region I? **[5 pts]**

n = ________________ cm^{-3}

p = ________________ cm^{-3}

iii) What is the sheet resistance of Region I? **[5 pts]**

R_s = ________________ Ω/square

iv) Suppose any voltage between 0 V and 5 V can be applied to Region I. What fixed voltage ("bias") would you apply to Region II, to guarantee that no current would ever flow between Region I and Region II? **Briefly explain your answer. [3 pts]**

Region II bias voltage = _____ V

Problem 4 **(continued)**

b) If a diode is operated only within a small range of forward-bias voltages, its behavior can be accurately modelled by a resistor, whose value is dependent on the bias voltage. Derive an expression for the diode "small-signal" resistance:

$$R_{diode} = \left(\frac{\partial I}{\partial V}\right)^{-1}$$

in terms of the saturation current I_s, the bias voltage V, and the absolute temperature T. **[5 pts]**

$R_{diode} =$ ____

c) Plot v_L vs. V_{IN} for **-10 V <** $\boldsymbol{V_{IN}}$ **< 10 V** on the axes provided, for the circuit below. Note that the diode is a perfect rectifier. **Label the axes. [5 pts]**