Name Solutions + Grading

EE 40

Midterm 3

April 24, 2003

PLEASE WRITE YOUR NAME ON EACH ATTACHED PAGE

PLEASE SHOW YOUR WORK TO RECEIVE PARTIAL CREDIT

PLEASE DO NOT LEAVE UNTIL EXAM PERIOD IS OVER

Problem 1: 15 Points Possible _____

Problem 2: 20 Points Possible _____

Problem 3: 15 Points Possible _____

Problem 4: 20 Points Possible _____

Problem 5: 20 Points Possible _____

Problem 6: 10 Points Possible _____

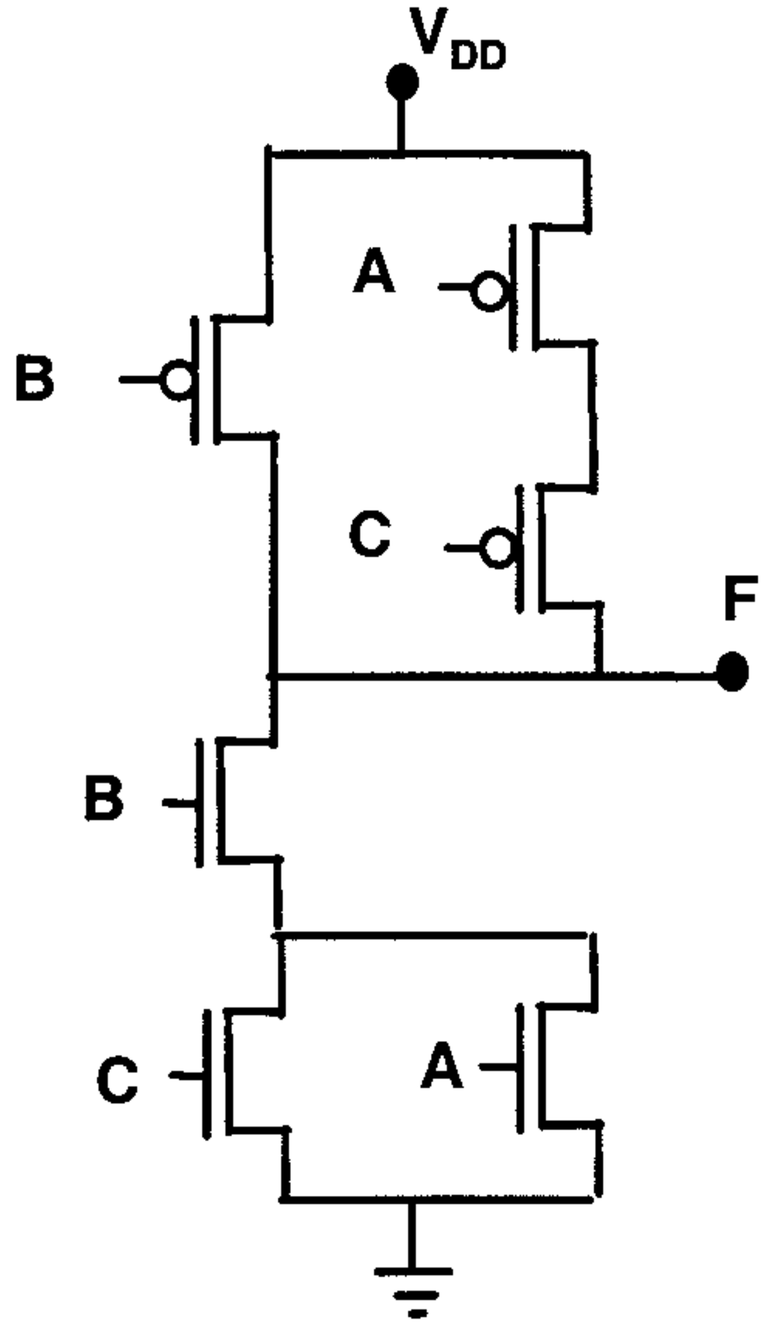
TOTAL: 100 Points Possible _____

Name Solutions

Problem 1: 15 Points Possible

Determine whether the circuit below performs a logical operation. If it does, give the Boolean function it computes. If not, give a set of inputs that results in an invalid output.

For your convenience, 8 copies of this circuit are given on the next page. Assume that all PMOS transistors have source terminal on top, and all NMOS transistors have source terminal on the bottom.



From looking at PMOS half: $F = V_{DD}$ if B conducts OR (A conducts AND C conducts)

$\overline{F} = B + AC$

From looking at NMOS half: $F = 0$ if B conducts AND (A conducts OR C conducts)

$\overline{F} = B(A+C)$

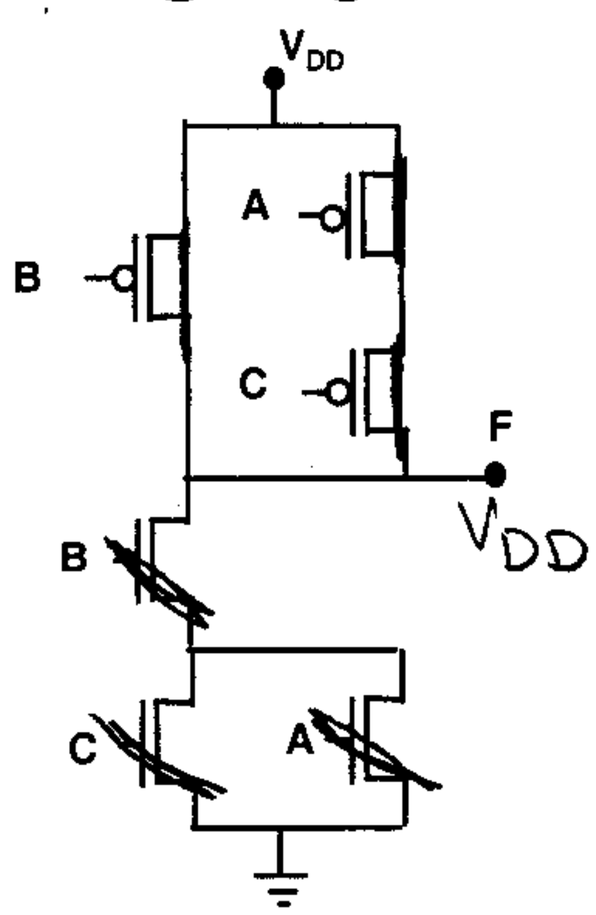
These agree by DeMorgan's law; it is a logic circuit.

Name Solutions

Problem 1 Workspace

Do switches for each ABC combo

A BC
0 00



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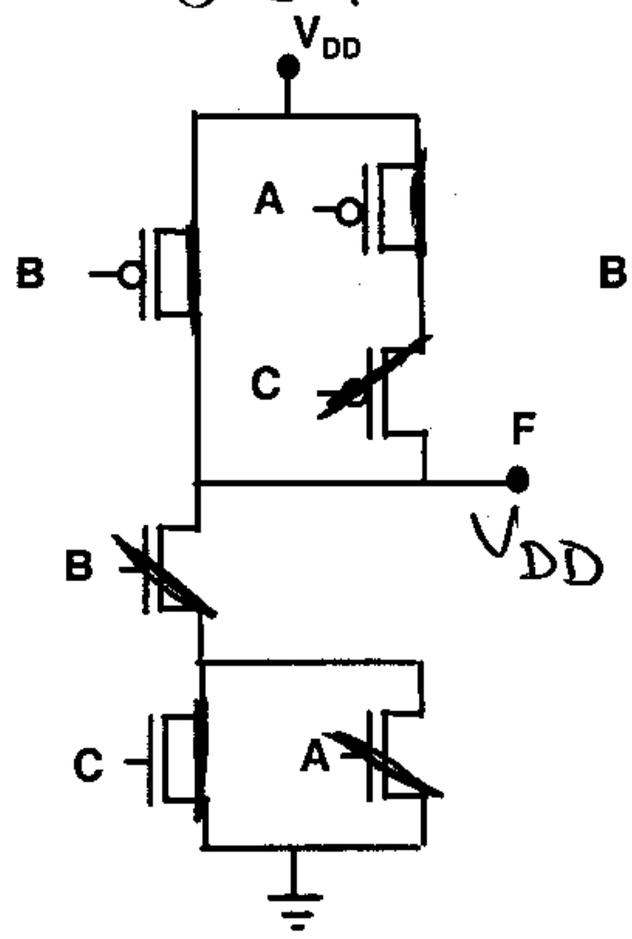
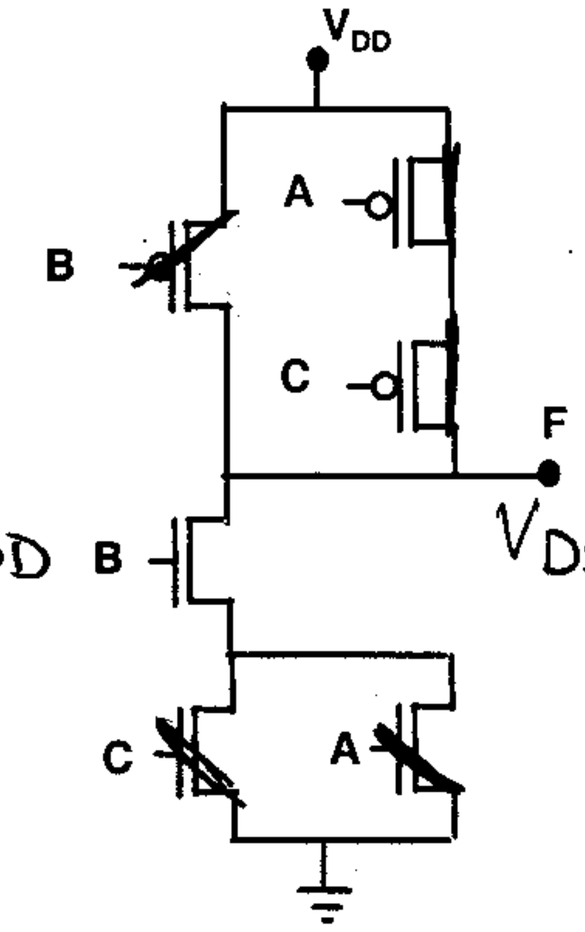


010



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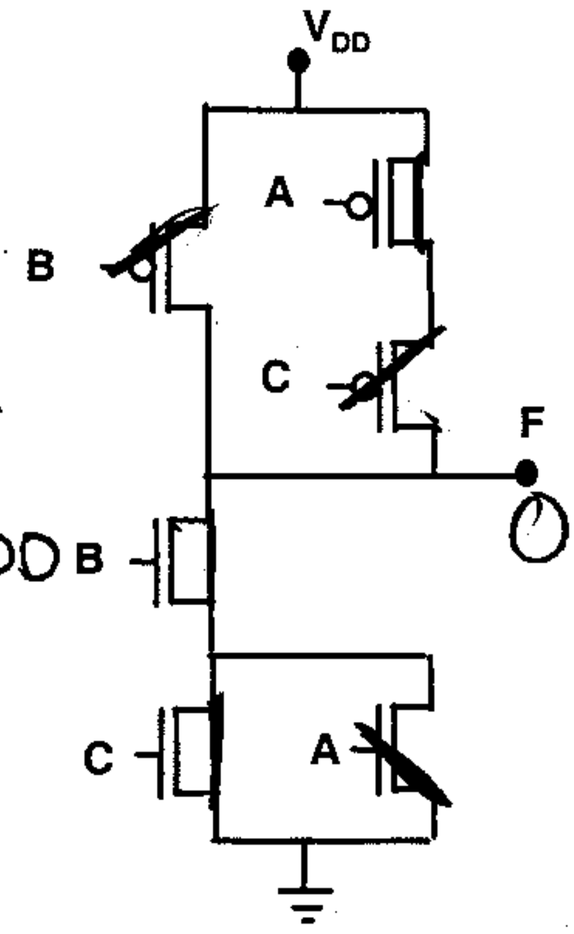

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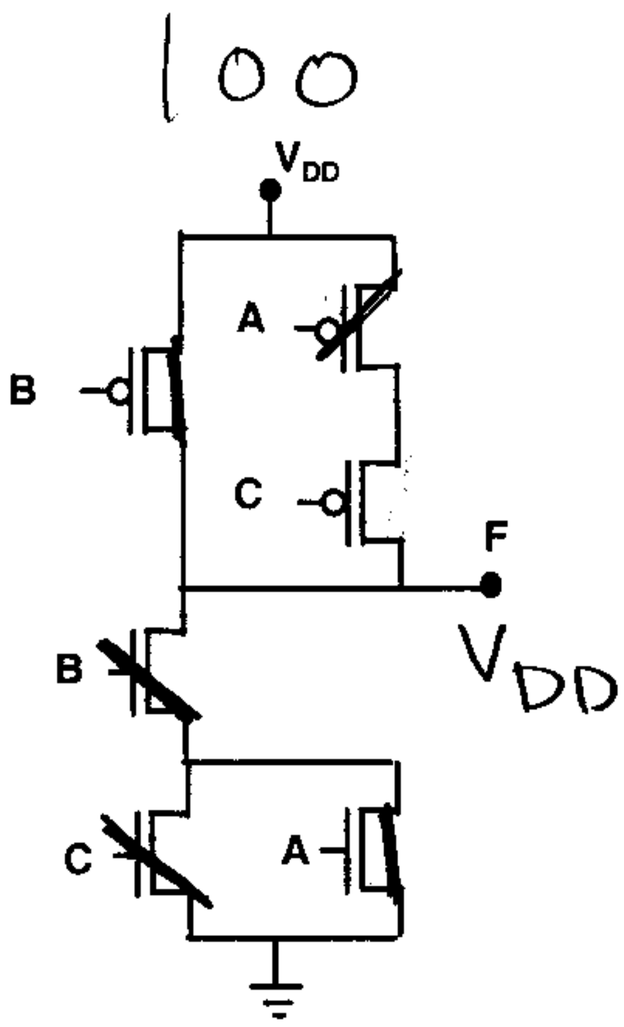

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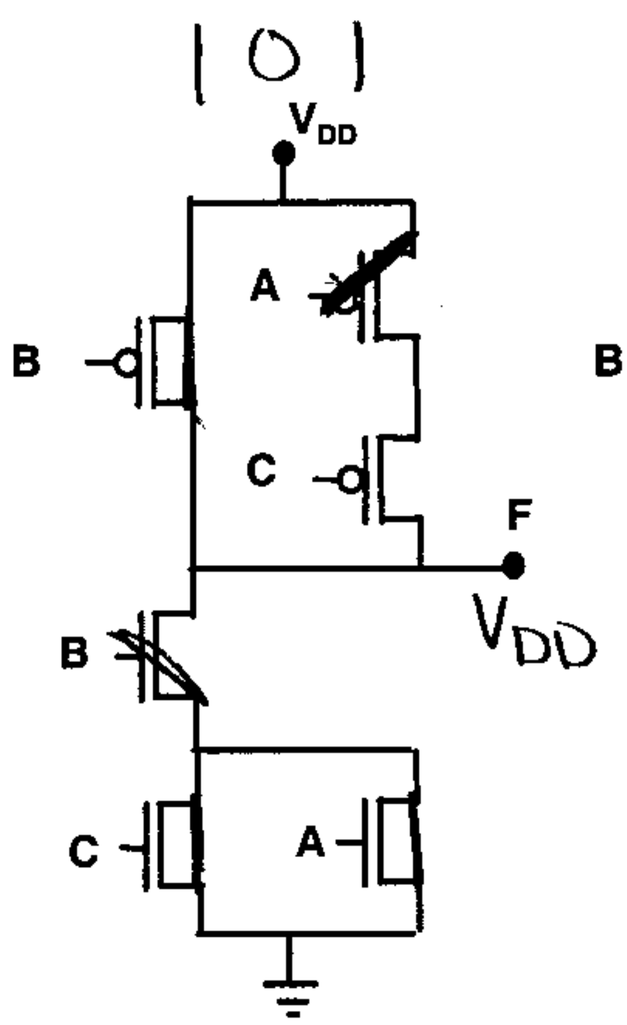

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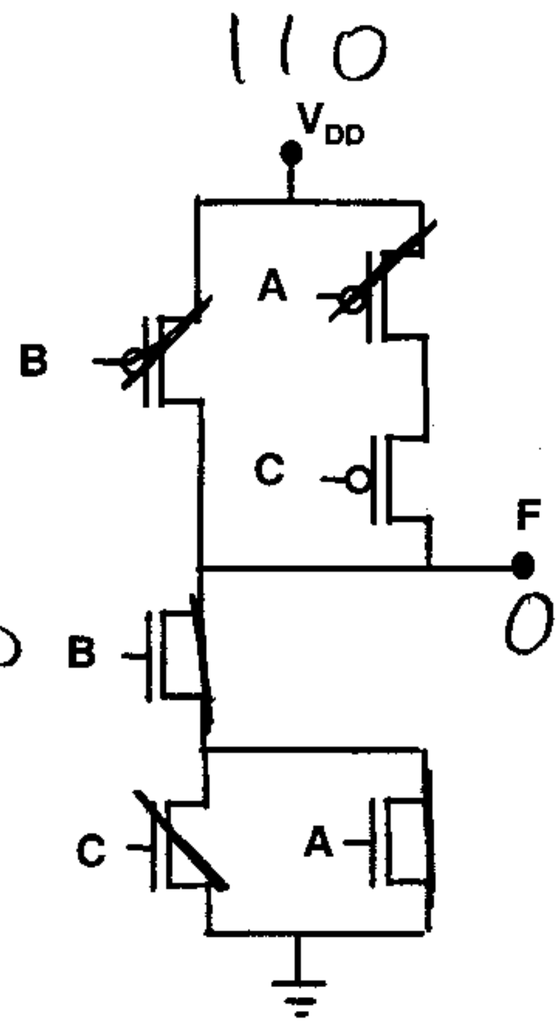

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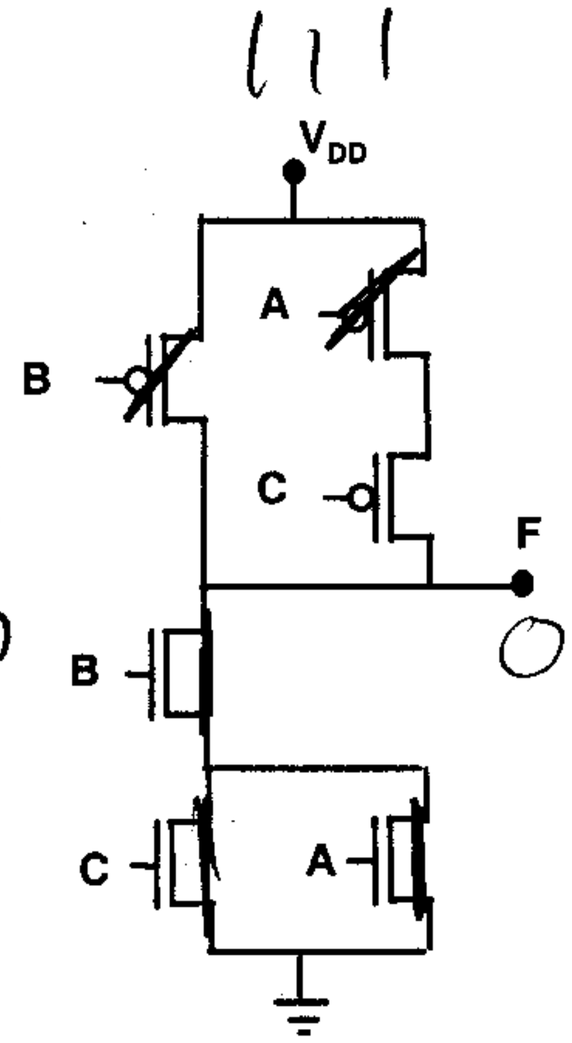


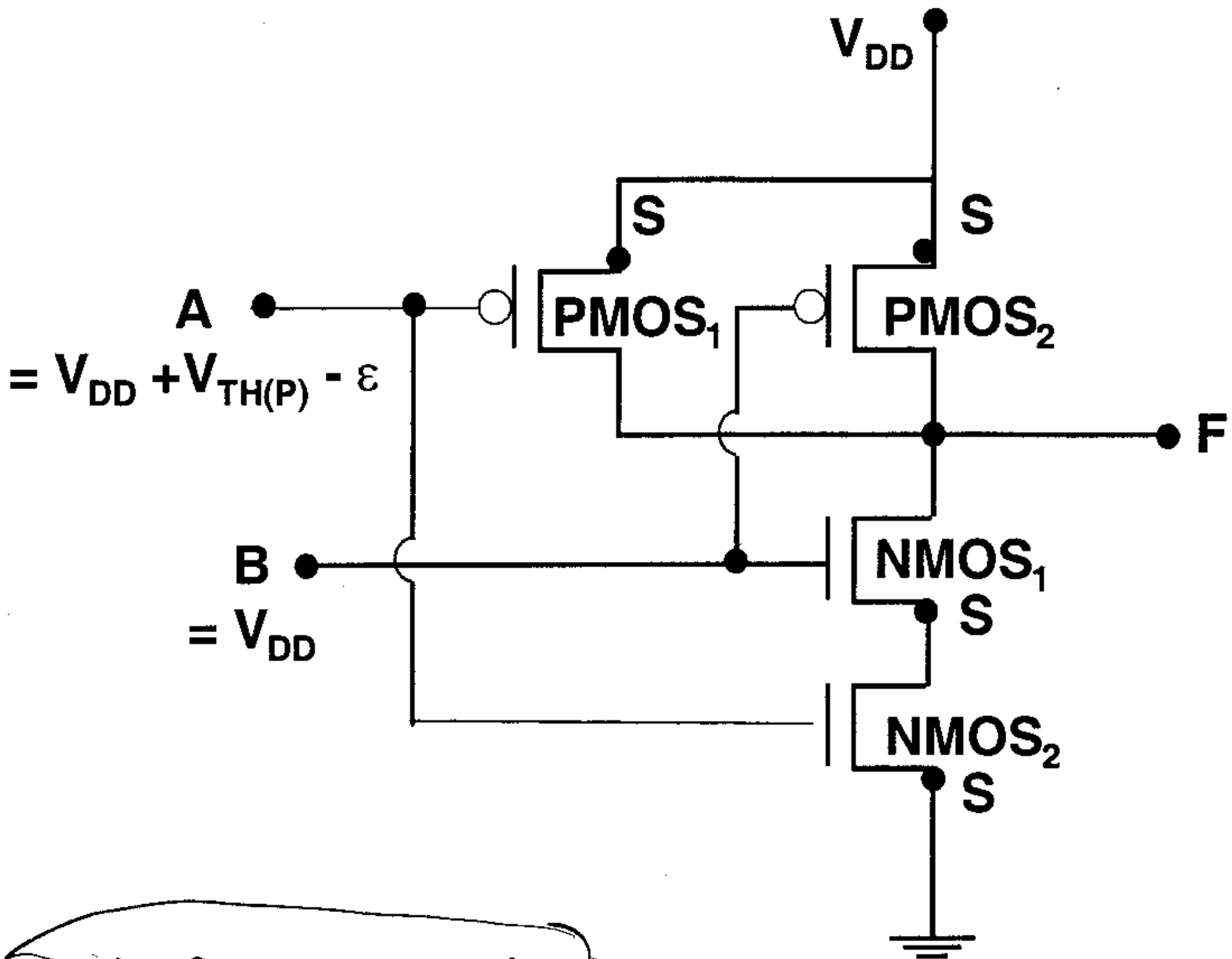
$$F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C$$

(Equivalent to previous results).

Name Solotions

Problem 2: 20 Points Possible

For the CMOS logic circuit below, determine the most probable mode of operation for each transistor. Assume that ε is a very small positive number, and V_{DD} is much larger in magnitude than either V_{TH}.



$PMOS_2$ cutoff ($V_{GSP2} = V_{DD} - V_{DD} = 0\,V$)

$PMOS_1$ barely on ($V_{GSP_1} = V_{DD} + V_{THP} - \varepsilon - V_{DD} = V_{THP} - \varepsilon$)

I_D shared by $PMOS_1$, $NMOS_1$, $NMOS_2$ is small

$V_{GSN_2} = V_{DD} + V_{THP} - \varepsilon$ for $NMOS_2$ is not small and is positive, since V_{DD} is much larger in magnitude than V_{THP} or ε (by assumption).

$NMOS_2$ fully on with small $I_D \Rightarrow$ $NMOS_2$ triode

$NMOS_2$ therefore also has small V_{DSN2},

so $V_{GSN1} = V_{DD} - V_{DSN2}$, the gate-source voltage for $NMOS_1$, is not small. $NMOS_1$ fully on, small $I_D \Rightarrow$ $NMOS_1$ triode

Name Solutions

Problem 2 Workspace

$NMOS_1$ therefore has small V_{DSN_1}.

$$V_{DD} = \underbrace{V_{DSN_1}}_{\text{small}} + \underbrace{V_{DSN_2}}_{\text{small}} - V_{DSP_1}$$

$\Rightarrow$ V_{DSP_1} negative with large magnitude

V_{GSP_1} negative with small magnitude & V_{DSP_1} negative with large magnitude $\Rightarrow$ PMOS, saturation

Name Solutions

Problem 3: 15 Points Possible

Consider the inverter at right, which turns on an LED when the output voltage is high.

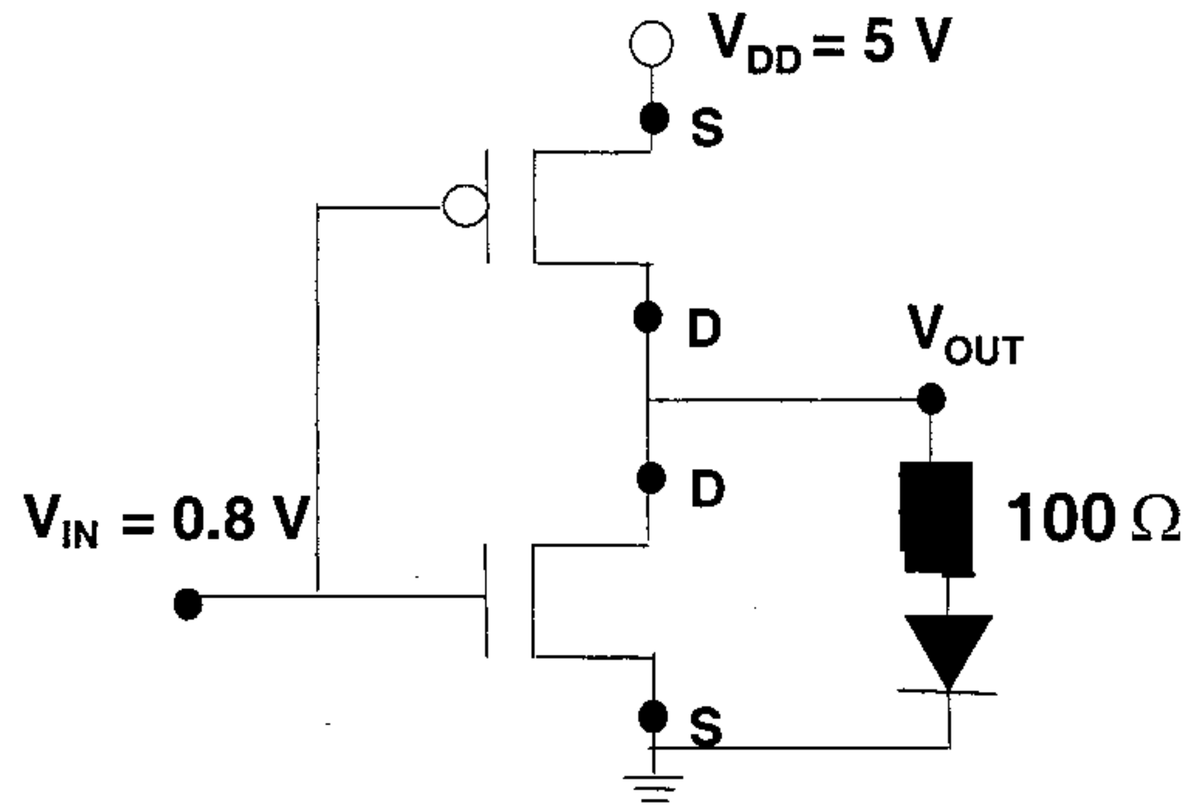
I have put a resistor in series with the LED to limit the current so the LED doesn't burn.

But, the LED needs a current of at least 20 mA to light up.

I want the LED to light up for an input voltage as high as 0.8 V.

Will the LED light up for an input of 0.8 V?

$W/L\ \mu C_{OX} = 100\ mA/V^2$ for both transistors,
$V_{TH(N)} = -V_{TH(P)} = 1\ V$,
$\lambda = 0\ V^{-1}$ for both transistors,
$V_F = 2\ V$ for the LED (use large-signal model).



NMOS cutoff ($V_{GS_N} = V_{IN} = 0.8\ V$) $\Rightarrow I_{D_N} = 0A$

PMOS triode (will show PMOS sat. is wrong)

① $I_{Dp} = -100\,mA/V^2 \left(\underbrace{0.8\ V - 5\ V}_{V_{GSp}} - 1\ V - \frac{V_{DSp}}{2}\right) V_{DSp}$

By KVL, ② $V_{DSp} = V_{OUT} - V_{DD} = V_{OUT} - 5$

By KCL, ③ $I_{Dp} = -\frac{V_{OUT} - V_F}{100} = -\frac{V_{OUT} - 2V}{100}$

Put ③ and ② into ① and solve for Vout:

$V_{out} = \{-1.51\ V,\ 4.91\ V\}$

impossible! keep.

$V_{DSp} = -0.09\ V$ OK for triode mode.

$I_{diode} = \frac{V_{out} - 2\ V}{100\ \Omega} = 29.1\ mA.$

LED Lights up!

Solutions

If guessed saturation for PMOS,

$$I_{Dp} = -\tfrac{1}{2} \cdot 100\,mA\,(0.8V - 5V - -1V)^2$$
$$= -512\,mA$$

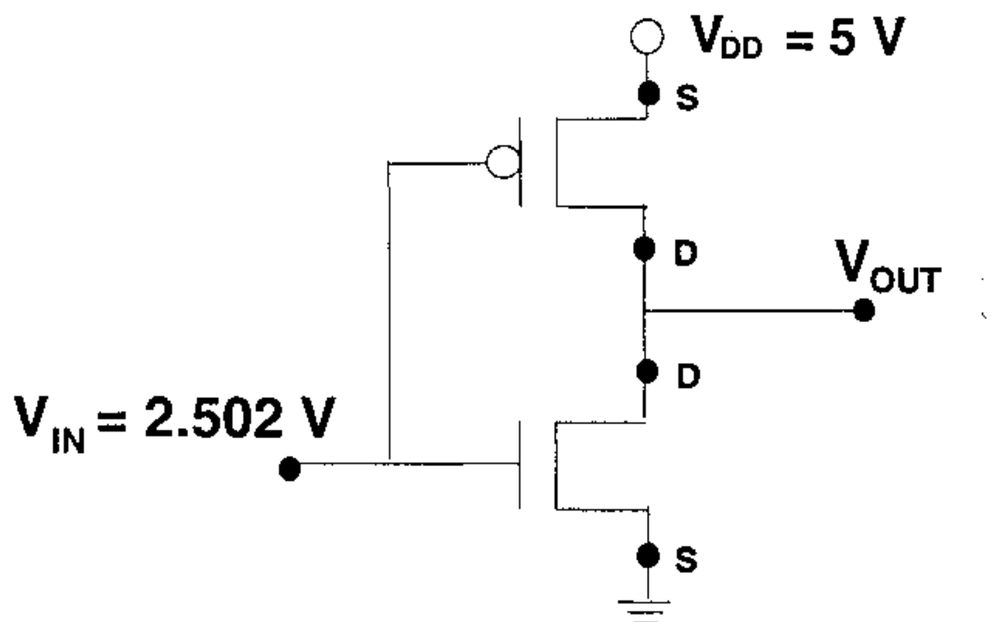
$$V_{DSp} = V_{out} - V_{DD} = -100 I_{Dp} + 2V - 5V$$
$$= 48.2\,V \quad \text{whoa! impossible.}$$

Name Solutions

Problem 4: 20 Points Possible

Consider the CMOS inverter at right, with

W/L μC_{OX} = 1 mA/V^2 for both transistors,
$V_{TH(N)} = -V_{TH(P)}$ = 1 V,
λ = **0.01 V^{-1} for both transistors.**
→ negative for PMOS!
For this inverter, V_M = 2.5 V.



a) Find V_{OUT} for V_{IN} = 2.502 V. Hint for guessing modes: Notice that V_{IN} is close to V_M.

b) Find the slope of the V_{OUT} vs. V_{IN} curve in this region, given by

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{V_{OUT}(\text{for } V_{IN} = 2.502 \text{ V}) - V_M}{2.502 \text{ V} - V_M}$$

Since we have unloaded inverter with V_{in} close to V_M, assume "region C" with both transistors in saturation.

$I_{DN} = 1/2 \cdot 1mA/V^2 (2.502V - 1V)^2 (1 + 0.01 V_{DSN})$

$I_{DP} = -1/2 \cdot 1mA/V^2 (2.502V - 5V - -1V)^2 (1 - 0.01 V_{DSP})$

KVL: $V_{DSP} = V_{DSN} - V_{DD} = V_{DSN} - 5V$

KCL: $I_{DP} + I_{DN} = 0 \Rightarrow I_{DN} = -I_{DP}$

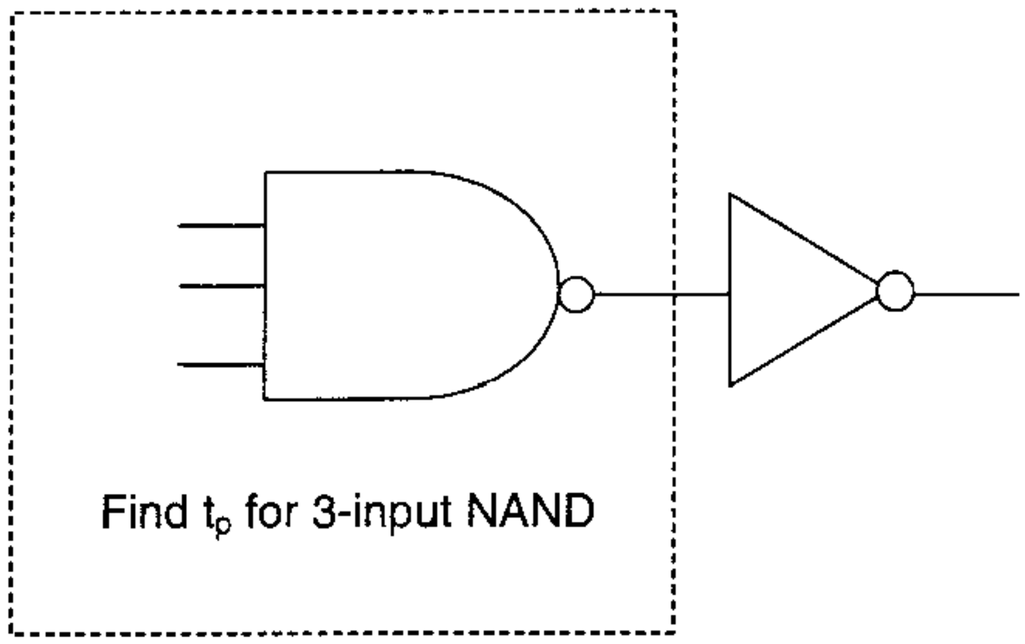
Solve the above to get $V_{DSN} = \boxed{V_{OUT} = 2.23 \text{ V}}$

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{2.23V - 2.5V}{2.502V - 2.5V} = \boxed{-135}$$

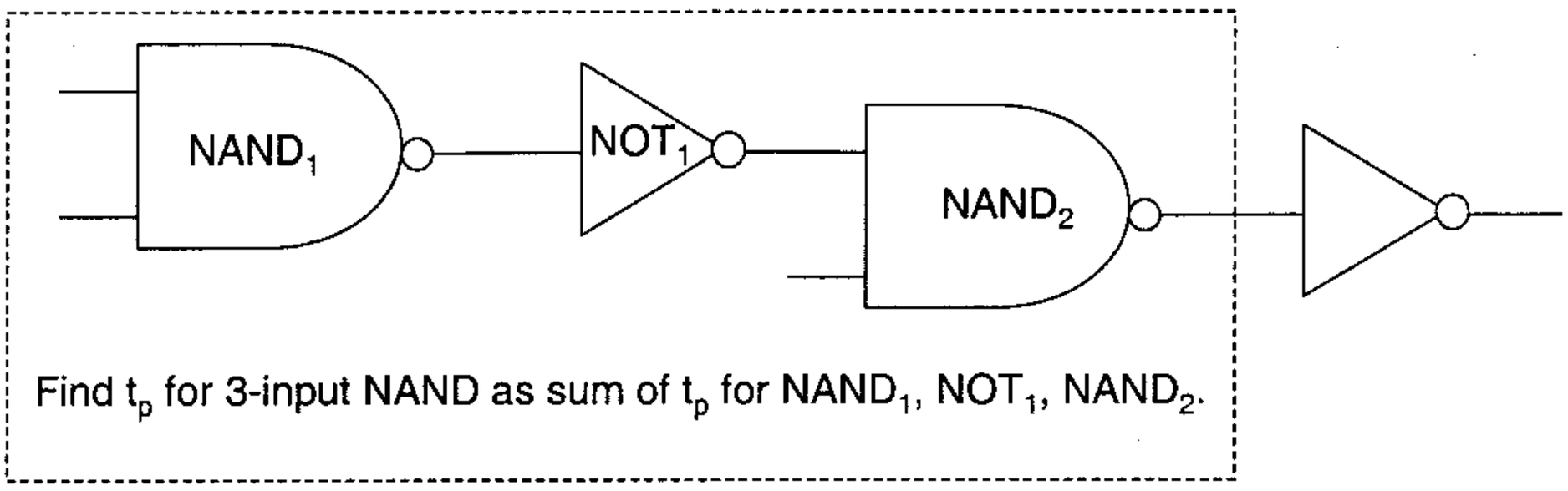
Name Solutions

Problem 5: 20 Points Possible

Find the propagation delay for this 3-input NAND gate with inverter load,



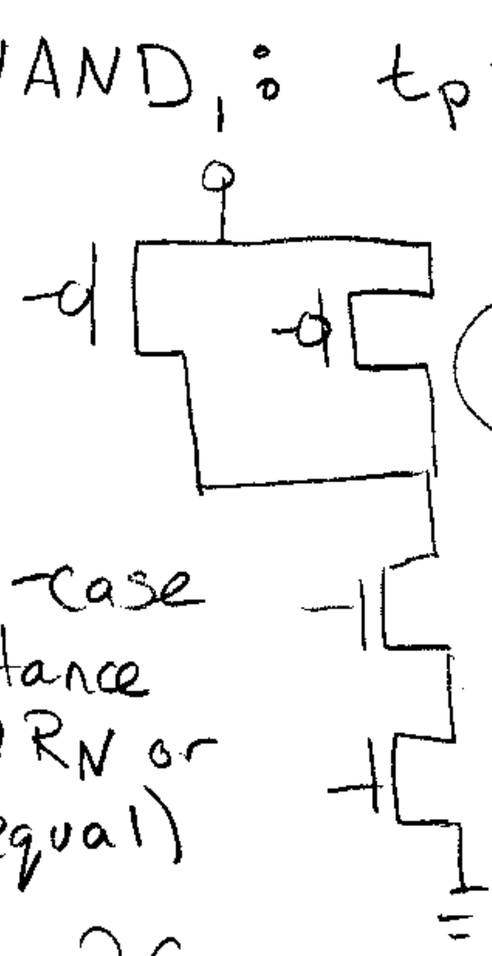
where the 3-input NAND is implemented using two 2-input NAND gates and an inverter:



Compute the propagation delay t_p for the 3-input NAND as the sum of the worst-case propagation delays of the individual gates inside.

Use R_N = 1 kΩ, R_P = 2 kΩ, and C_G = 10 fF per transistor. Ignore interconnect capacitance.

$NAND_1$: $t_p = 0.69 R_p (2C_G)$
$= 27.6$ ps



Same for $NAND_2$.

Worst-case resistance is $2R_N$ or R_P (equal)

$C_{out} = 2C_G$
(inverter has 2 transistors)

NOT_1: $t_p = 0.69 R_p (2C_G)$
$= 27.6$ ps

Total t_p for 3-input NAND: $3(27.6\text{ ps}) = 82.8$ ps

Worst-case resistance is R_p.
$C_{out} = 2C_G$
(output goes to one input of NAND: 2 of the 4 transistors)

Name Solutions

Problem 6: 10 Points Possible

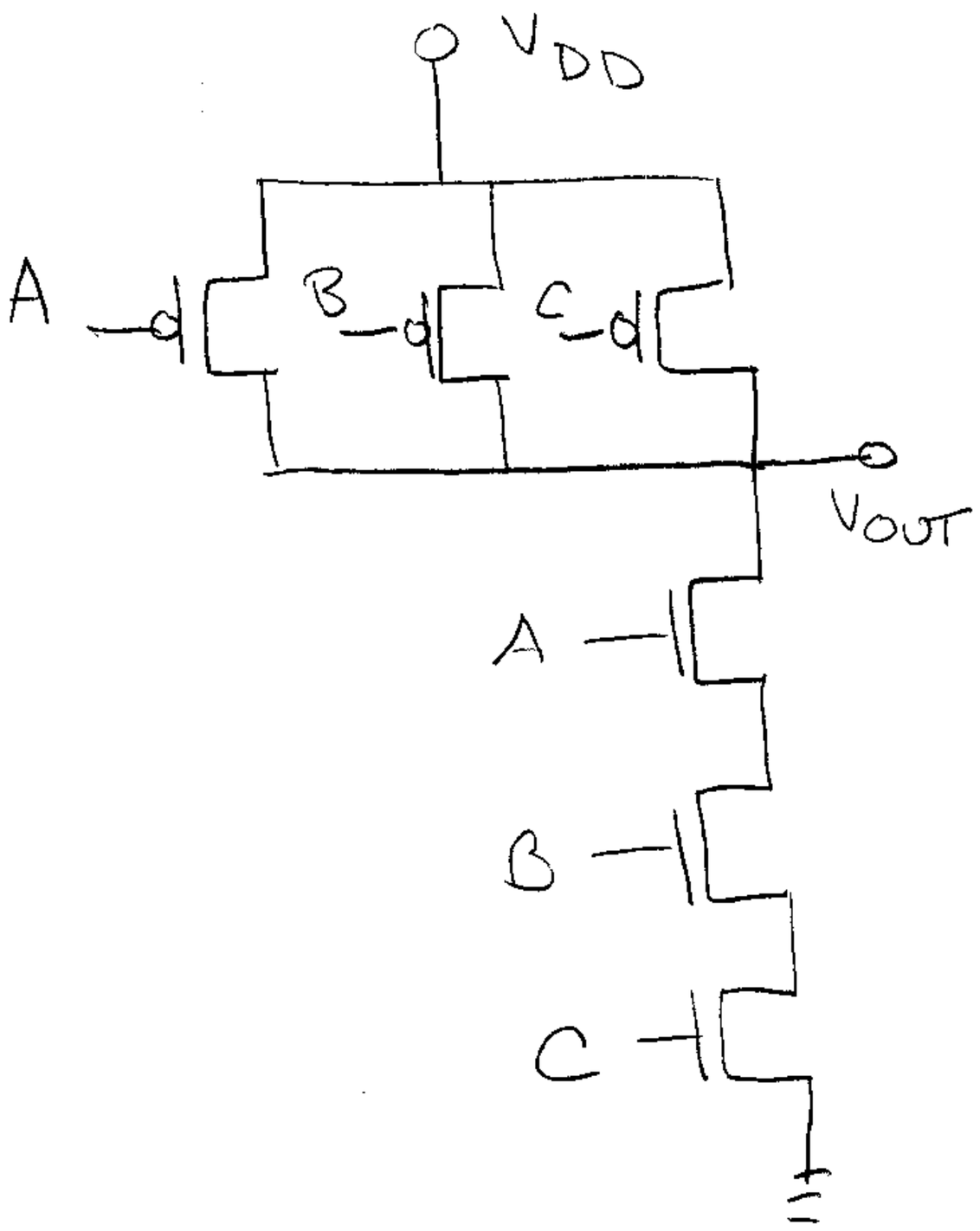
Design a circuit, using only NMOS and PMOS transistors (and a power supply), that performs the 3-input NAND function with **shorter** worst-case propagation delay than the implementation given in Problem 5, when a single inverter is attached as the output load.

Assume that your transistors have the same characteristics as those in Problem 5:

Use $R_N = 1\ k\Omega$, $R_P = 2\ k\Omega$, and $C_G = 10\ fF$ per transistor. Ignore interconnect capacitance.

Provide your design and its worst-case propagation delay with single inverter output load.

Popular Solution:



Worst-case resistance:
$3R_N$ (pull-down)
If attached to inverter,
$C_{OUT} = 2C_G$

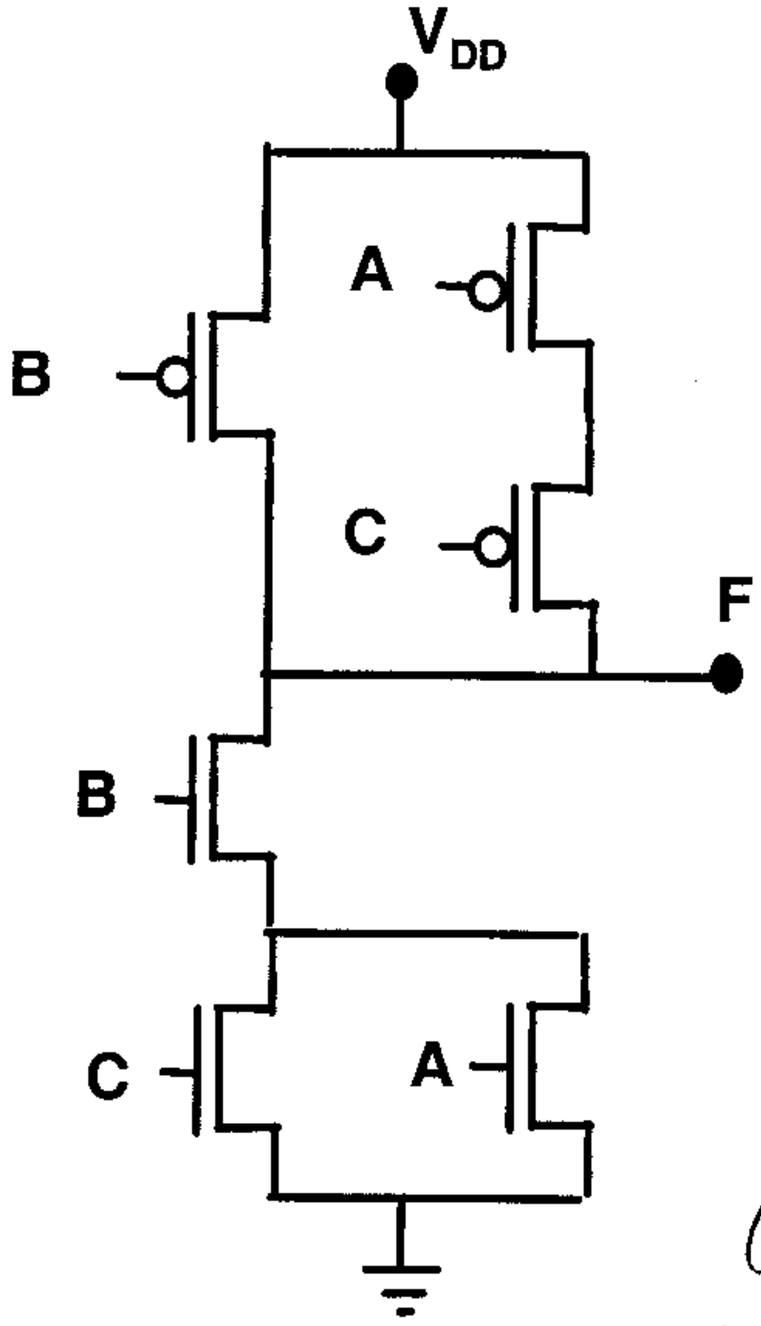
$t_p = 0.69(3R_N)(2C_G)$
$= 41.4\ ps$
(half the delay of the Problem 5 analysis)

Name Grading

Problem 1: 15 Points Possible

Determine whether the circuit below performs a logical operation. If it does, give the Boolean function it computes. If not, give a set of inputs that results in an invalid output.

For your convenience, 8 copies of this circuit are given on the next page. Assume that all PMOS transistors have source terminal on top, and all NMOS transistors have source terminal on the bottom.

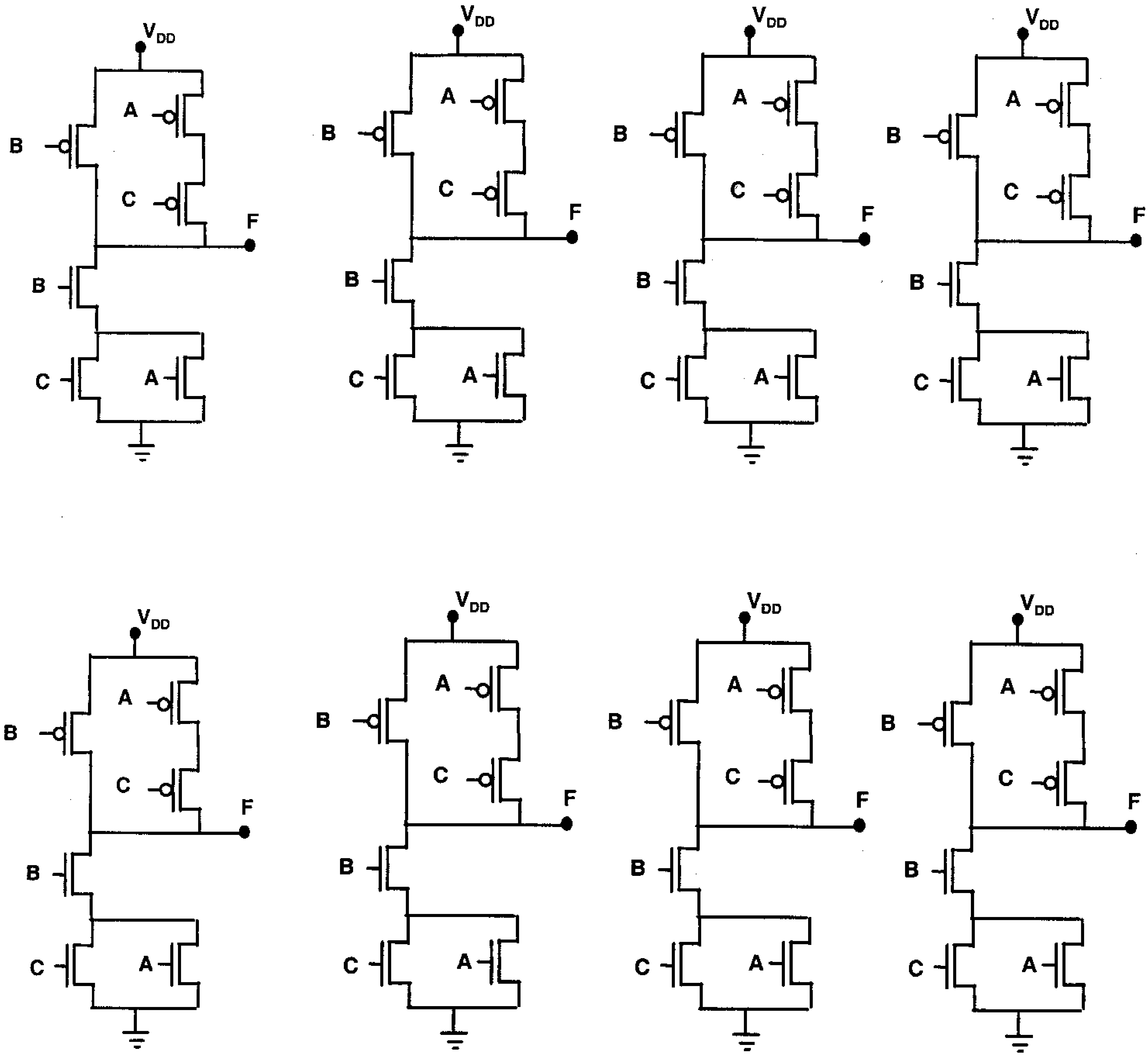


15 points for Correct function (any form)

-5 for various major errors (De Morgan applied wrong, things inverted or and/or ed where they shouldn't be, etc).

Name Grading

Problem 1 Workspace



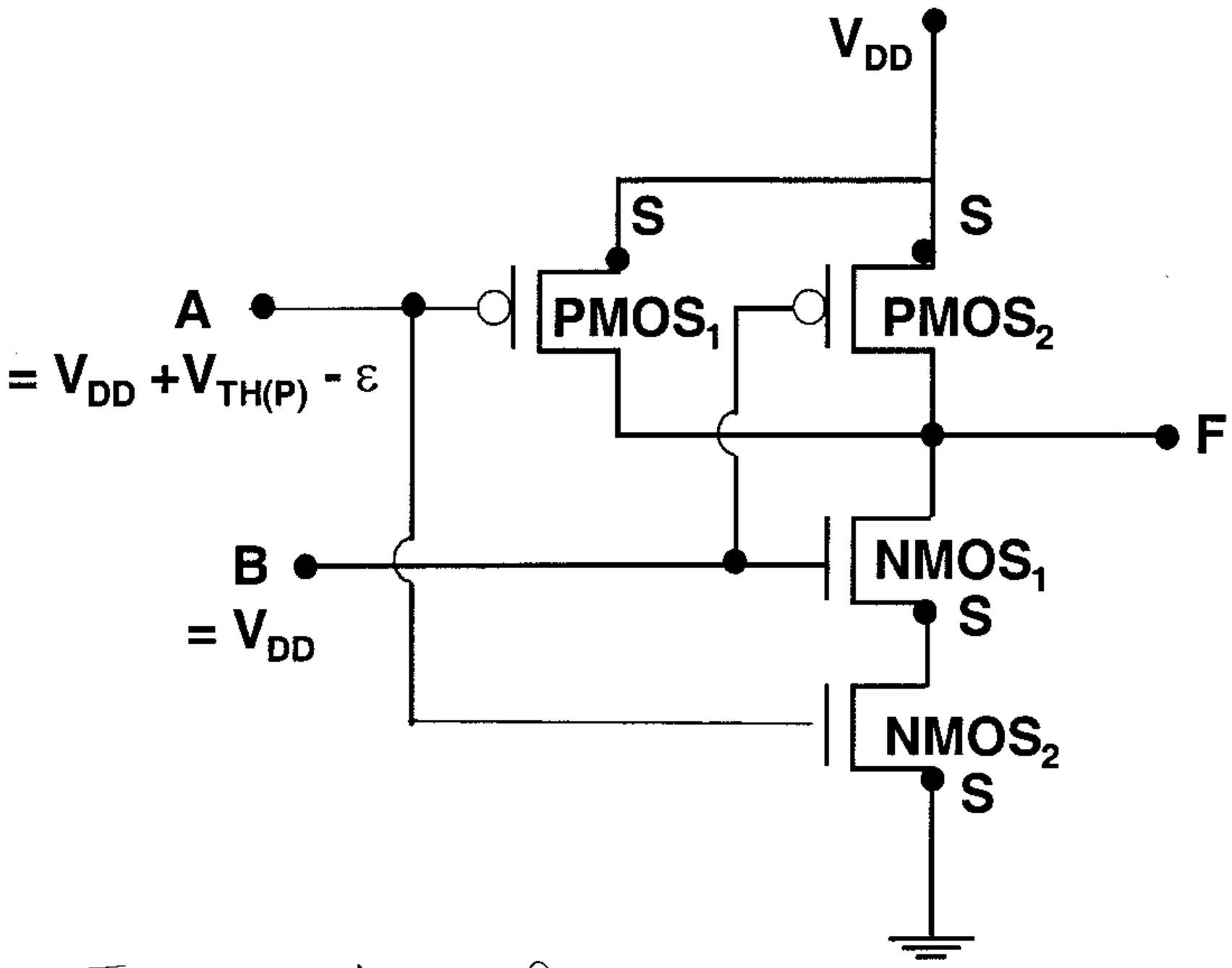
1.5 points for each correct output, all or nothing

3 points for corresponding Boolean function (award 1.5 points if it has a very small error)

Name Grading

Problem 2: 20 Points Possible

For the CMOS logic circuit below, determine the most probable mode of operation for each transistor. Assume that ε is a very small positive number, and V_{DD} is much larger in magnitude than either V_{TH}.



5 points for each transistor

Mostly all-or-nothing, but if complete & correct information about a transistor is provided and the mode is accidentally recorded wrong, subtract only 2 points.

Also, if mode is wrong, but would be correct given the previous wrong assumptions/conclusions, do not subtract points.

Name Grading

Problem 3: 15 Points Possible

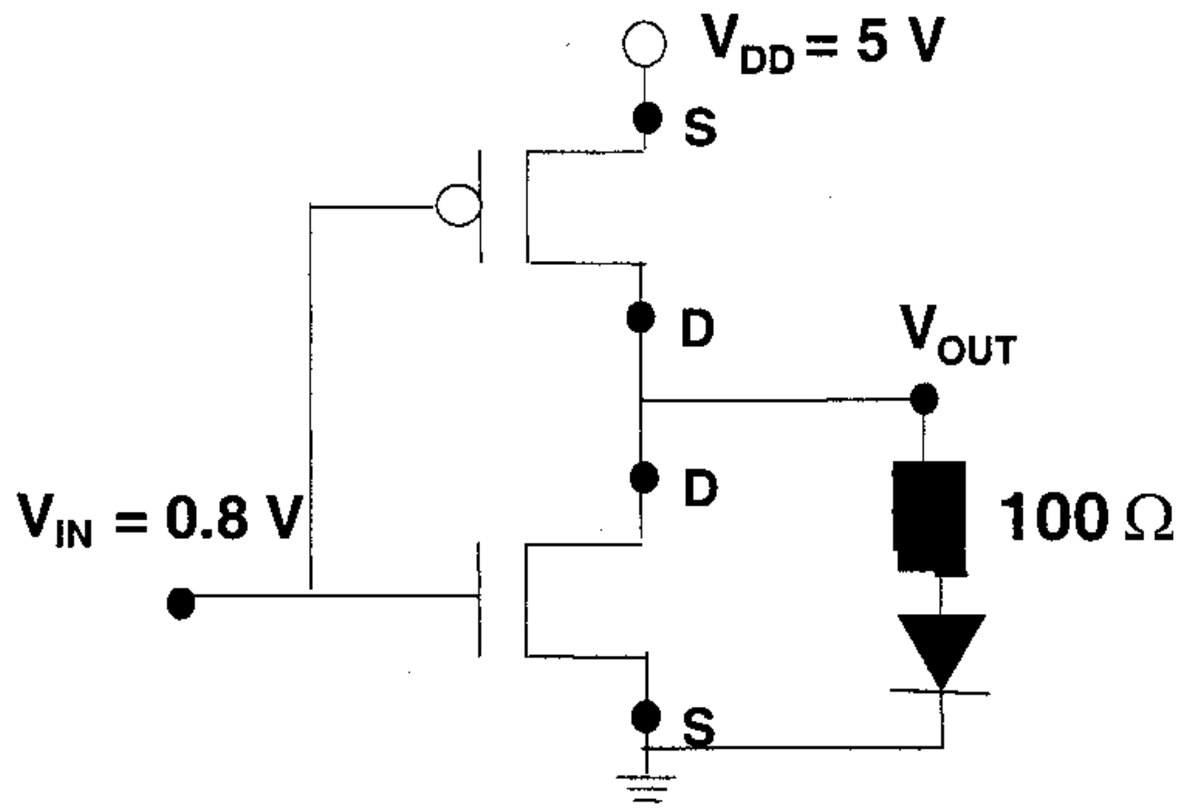
Consider the inverter at right, which turns on an LED when the output voltage is high.

I have put a resistor in series with the LED to limit the current so the LED doesn't burn.

But, the LED needs a current of at least 20 mA to light up.

I want the LED to light up for an input voltage as high as 0.8 V.

Will the LED light up for an input of 0.8 V?



$W/L\ \mu\ C_{OX} = 100\ mA/V^2$ for both transistors,
$V_{TH(N)} = -V_{TH(P)} = 1$ V,
$\lambda = 0\ V^{-1}$ for both transistors,
$V_F = 2$ V for the LED (use large-signal model).

Grading based on reasoning as well as yes/no answer.

-2 if math error -3 for minor error

-7 if answer is just "Yes" or based on saturation mode

Other errors graded accordingly.

-4 for various major errors,

-6 if assumed $I_{D_p} = -20\,mA$

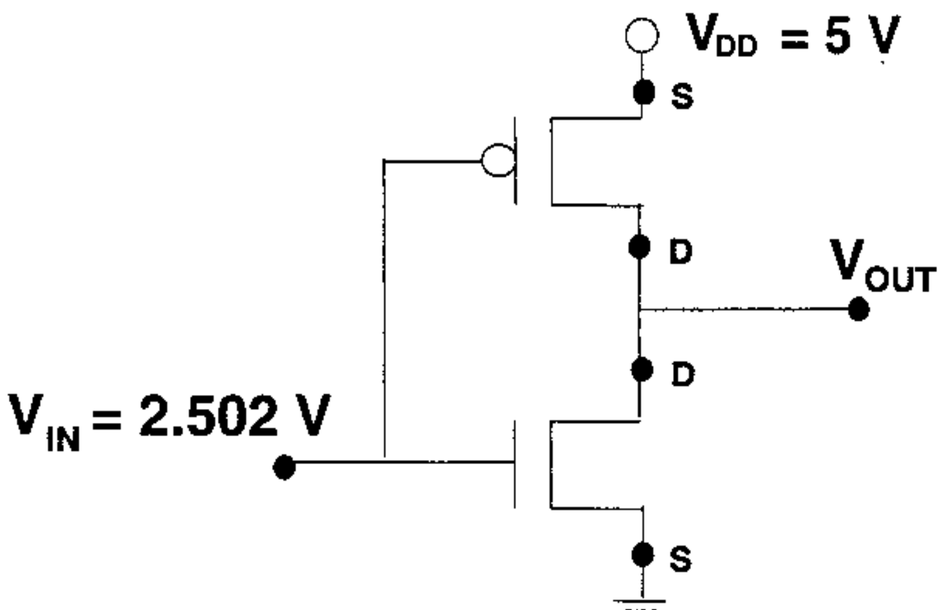
Name Grading

Problem 4: 20 Points Possible

Consider the CMOS inverter at right, with

W/L μ C_{OX} = 1 mA/V^2 for both transistors,
$V_{TH(N)} = -V_{TH(P)}$ = 1 V,
λ = 0.01 V^{-1} for both transistors.

For this inverter, V_M = 2.5 V.



a) Find V_{OUT} for V_{IN} = 2.502 V. Hint for guessing modes: Notice that V_{IN} is close to V_M.

b) Find the slope of the V_{OUT} vs. V_{IN} curve in this region, given by

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{V_{OUT}(\text{for } V_{IN} = 2.502 \text{ V}) - V_M}{2.502 \text{ V} - V_M}$$

a) 5 points for correct modes
5 points for correctly written equations
5 points for Solution

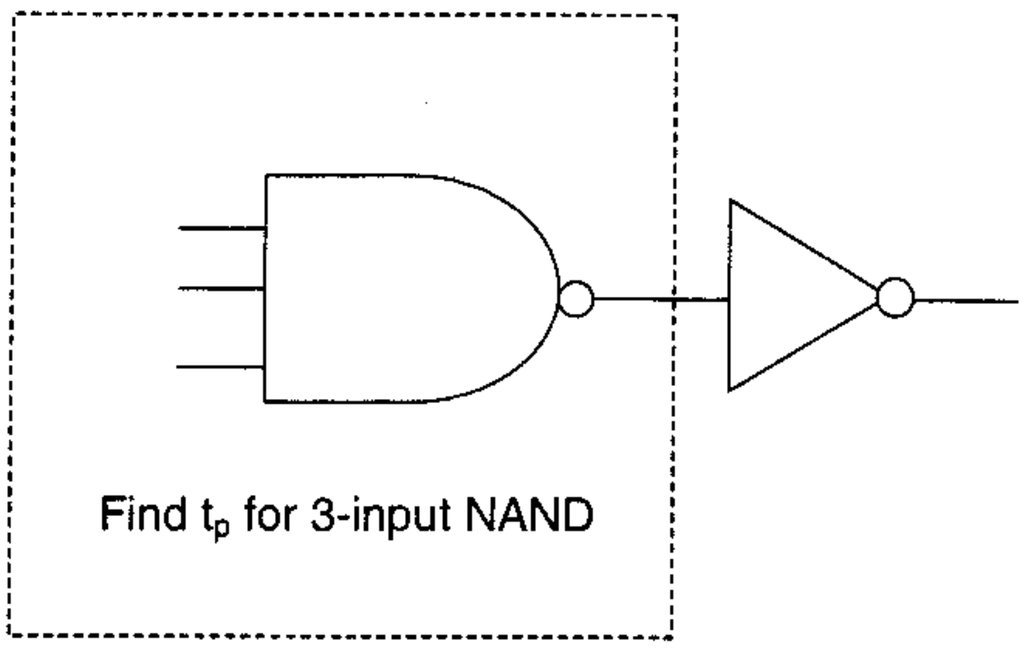
b) 5 points for correct computation

Possibility of -2 for math errors or -3 to -4 for other relatively minor errors.

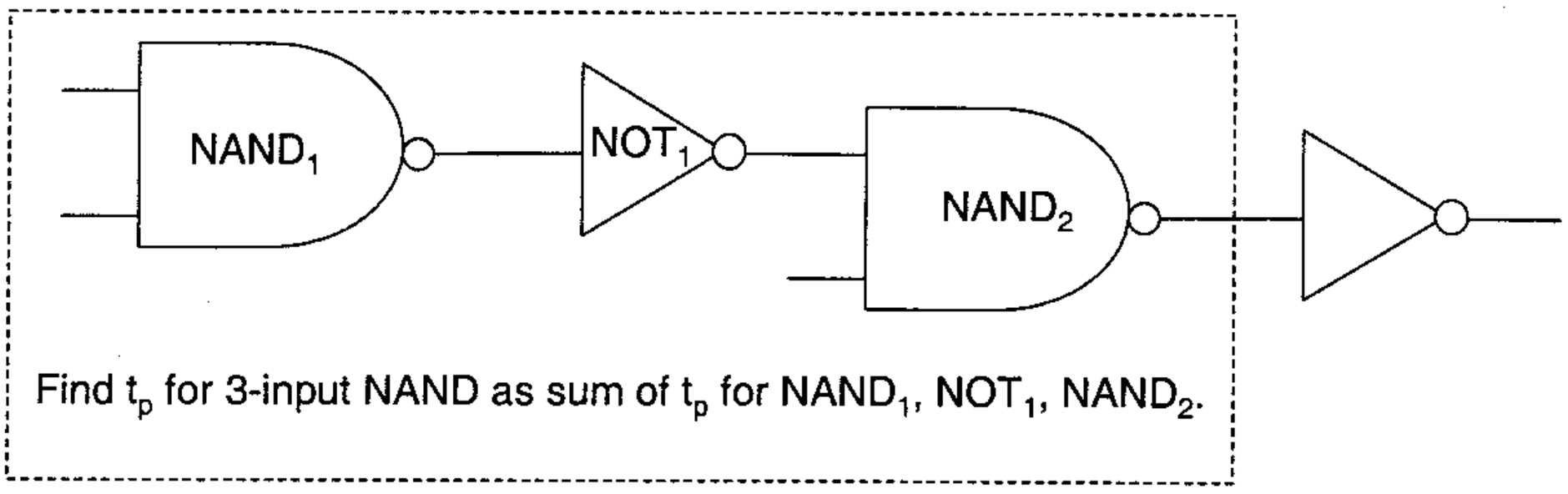
Name Gradins

Problem 5: 20 Points Possible

Find the propagation delay for this 3-input NAND gate with inverter load,



where the 3-input NAND is implemented using two 2-input NAND gates and an inverter:



Compute the propagation delay t_p for the 3-input NAND as the sum of the worst-case propagation delays of the individual gates inside.

Use R_N = 1 kΩ, R_P = 2 kΩ, and C_G = 10 fF per transistor. Ignore interconnect capacitance.

- 4 for wrong worst-case resistance
- 4 for wrong output capacitance
Don't double-count same mistake
(i.e. only -4 for wrong resistance for NAND$_1$ & NAND$_2$)
-2 for math error (incl. powers of 10 error)

Name Grading

Problem 6: 10 Points Possible

Design a circuit, using only NMOS and PMOS transistors (and a power supply), that performs the 3-input NAND function with **shorter** worst-case propagation delay than the implementation given in Problem 5, when a single inverter is attached as the output load.

Assume that your transistors have the same characteristics as those in Problem 5:

Use R_N = 1 kΩ, R_P = 2 kΩ, and C_G = 10 fF per transistor. Ignore interconnect capacitance.

Provide your design and its worst-case propagation delay with single inverter output load.

If design does 3-input NAND but is not correctly proven to have shorter t_p, - 9 points.

Otherwise,

If design only has very small error, -3 points.

(If propagation delay calculated incorrectly, -4 points.