Final Exam
May 18, 2004
Time Allowed: 3 Hours

Solutions

Name:____________________, ____________________
Last First

Student ID #:______________, Signature:____________________

Discussion Section:______________________________

This is a closed-book exam, except for use of three 8.5 x 11 inch sheets of your notes. Show all your work to receive full or partial credit. Write your answers clearly in the spaces provided.

	Problem #:	Points:
Dennis ~~Jack~~	1	/10
Mervin	2	/10
Siddharth	3	/10
Arko	4	/15
Arko	5	/10
Steve	6	/10
Jack	7	/15
	Total	/80

1. (10 points)

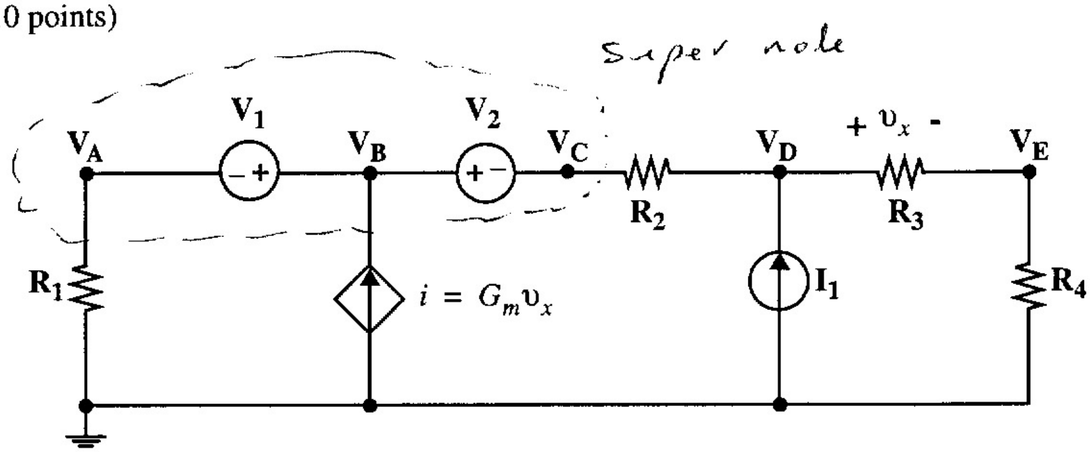


Figure 1

In the circuit of Figure 1, all voltage sources, current sources and resistors are known. Write a set of node equations sufficient to solve the circuit. You must use the labeled node potentials $\mathbf{V_A}$, $\mathbf{V_B}$, $\mathbf{V_C}$, $\mathbf{V_D}$ and $\mathbf{V_E}$. Do **not** solve your equations.

$$\frac{V_A}{R_1} - G_m (V_D - V_E) + \frac{V_C - V_D}{R_2} = 0$$

$$V_A - V_C = -V_1 + V_2$$

$$\frac{V_D - V_C}{R_2} + \frac{V_D - V_E}{R_3} = I_1$$

$$\frac{V_E - V_D}{R_3} + \frac{V_E}{R_4} = 0$$

4 eq's in 4 unknowns

$\{V_A, V_C, V_D, V_E\}$

2. (10 points)

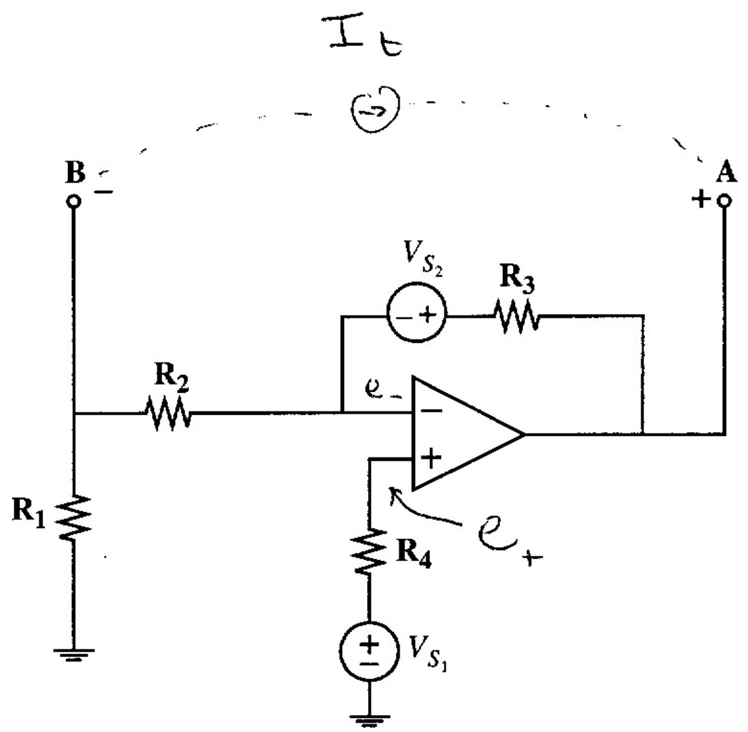


Figure 2

The op-amp in Figure 2 is ideal. Determine the Thevenin Equivalent Circuit with respect to the two terminals A and B.

$$V_{oc} = \frac{R_2+R_3}{R_1+R_2} V_{s_1} + V_{s_2}$$

$$R_{th} = \frac{R_3+R_2}{R_2}(R_1 // R_2)$$

(i) V_{oc} by superposition:

V_{s_1} only: $e_+ = e_- = V_{s_1}$

$$V_B = \frac{R_1}{R_1+R_2} V_{s_1} \quad ; \quad V_A = \frac{R_1+R_2+R_3}{R_1+R_2} V_{s_1}$$

$$V_{oc}\Big|_{V_{s_1}} = V_A - V_B = \frac{R_2+R_3}{R_1+R_2} V_{s_1}$$

V_{s_2} only: $e_+ = e_- = 0 \Rightarrow V_B = 0$; $V_A = V_{s_2}$

(ii): Apply I_t with $V_{s_1} = V_{s_2} = 0$

$$V_B = -I_t(R_1 // R_2) \quad ; \quad V_A = -\frac{R_3}{R_2} V_B \Rightarrow V_t = V_A - V_B = \frac{R_3+R_2}{R_2}(R_1 // R_2) I_t$$

3. (10 points)

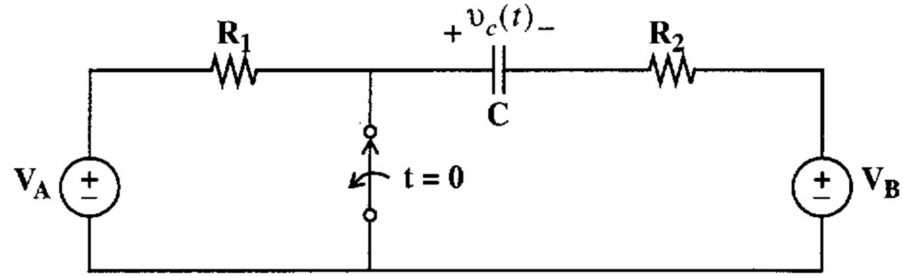


Figure 3

The circuit of Figure 3, is in equilibrium for $t < 0$. The switch is opened at $t = 0$.

a) (5 points)
Determine the capacitor voltage $v_c(t)$ for $t > 0$.

$v_c(0) = -V_B$; $V_c(\infty) = V_A - V_B$

$\tau = (R_1 + R_1)C$ for $t > 0$

$v_c(t)\Big|_{t>0} = (V_A - V_B) + (-V_A)\, e^{-\frac{t}{(R_1+R_2)C}}$

b) (5 points)
Determine the total energy dissipated in $\mathbf{R_1}$ and $\mathbf{R_2}$ combined, during the transient after the switch is opened at t = 0.

$\frac{1}{2} C V_A^2$

4. (15 points)

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

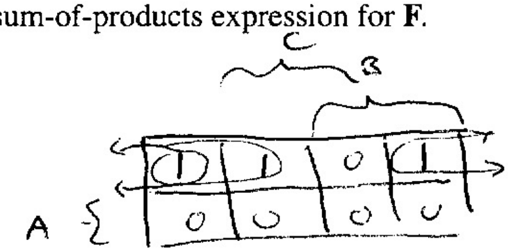
Figure 4

a) (5points)
In the truth table of Figure 4, consider **A**, **B** and **C** as inputs and **F** as output. Write **F** as a sum-of-products expression.

$$F = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

b) (5 points)
Generate a minimal sum-of-products expression for **F**.

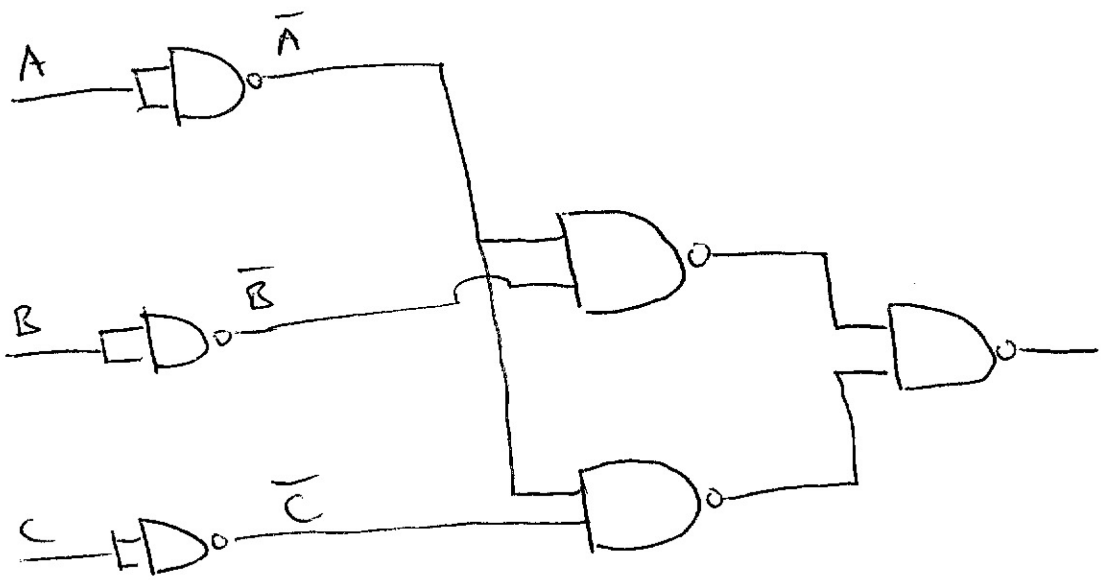
Karnough Map



$$F = \bar{A}\bar{B} + \bar{A}\bar{C}$$

4. (continued)

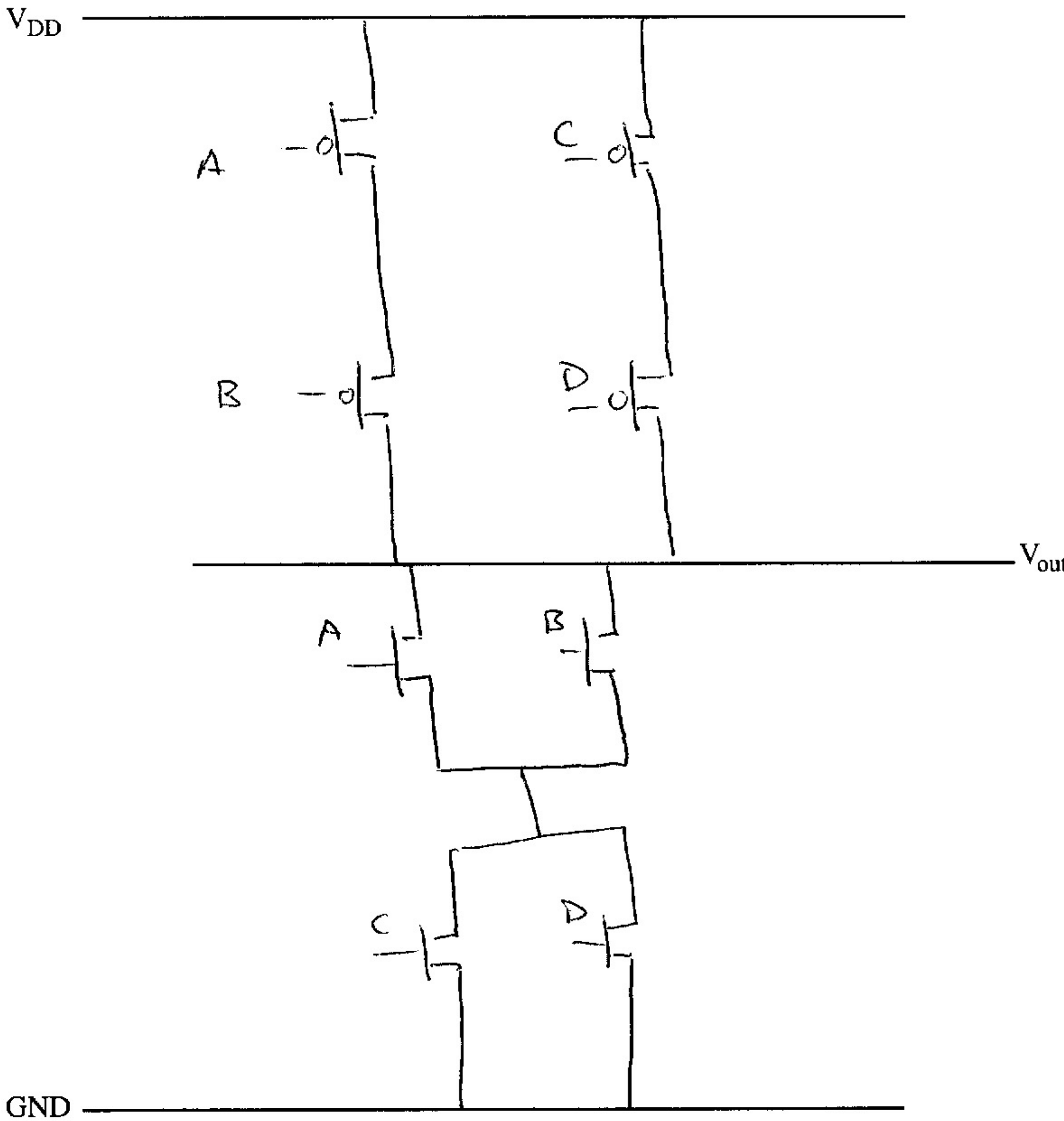
c) (5 points)
Draw a logic implementation of your minimal sum-of-products from part (b), using only NAND gates.



5. (10 points)

Consider the logic expression $F = \overline{(A+B)} + \overline{(C+D)}$.

Draw a CMOS implementation of this logic function in the diagram below. You will need to specify the pull-up network and the pull-down network.



$\overline{F} = (A+B) \cdot (C+D)$

6. (10 points)

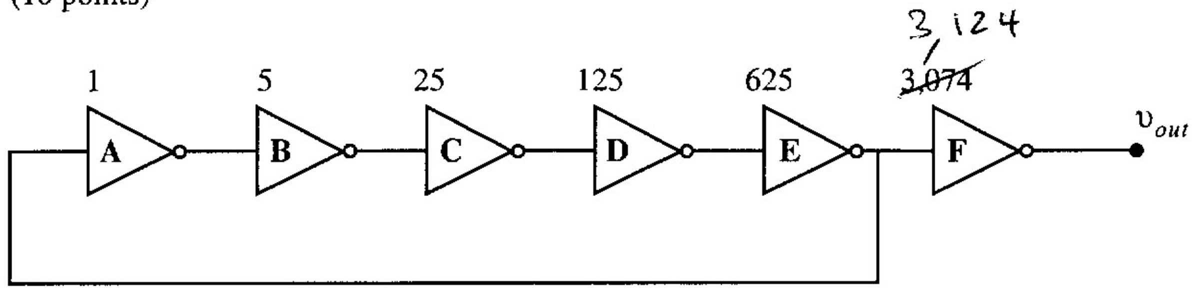


Figure 6

Figure 6 shows a ring oscillator implemented with a buffer structure. Inverter **A** on the far left is a basic inverter with $R_p = 6k\Omega$, $R_n = 4k\Omega$ and $C_G = 5fF$. We only consider gate capacitance in this problem. Inverter **B** is exactly five times bigger (i.e. $W_{n_B} = 5W_{n_A}$; $W_{p_B} = 5W_{p_A}$) than inverter **A**. Analogously, the relative sizes of inverters **C, D, E** and **F** are shown in Figure 6. Suppose $V_{iL} = \frac{1}{e}V_{DD}$ and $V_{iH} = \left(1 - \frac{1}{e}\right)V_{DD}$.

Determine the frequency of oscillation for the ring oscillator of Figure 6.

For each stage, $\tau_{V_{DD} \to V_{iL}} = 5 \cdot 20\,ps = 100\,ps$

$\tau_{0 \to V_{iH}} = 5 \cdot 30\,ps = 150\,ps$

$T = 5 \cdot \{ \tau_{V_{DD}-V_{iL}} + \tau_{0-V_{iH}} \} = 5 \cdot 250\,ps$

$= 1.25\,ns$

$f = 800\ MHz$

7. (15 points)

A process for fabrication of a diffusion resistor is as follows:

0) Begin with lightly doped p-type Si substrate.

1) Grow SiO_2 to a thickness of 500 nm.

2) Pattern SiO_2 with a dark field mask that defines the resistor pattern.

3) Implant donors with a concentration of 10^8 ions/cm^2 and anneal uniformly to a depth of 500 nm.

4) Deposit SiO_2 to a thickness of 625 nm.

5) Pattern SiO_2 with a dark field mask that defines the contacts.

6) Deposit Al to a thickness of $1\mu m$.

7) Pattern Al with a clear field mask.

Masks for this problem are shown in Figure 7.

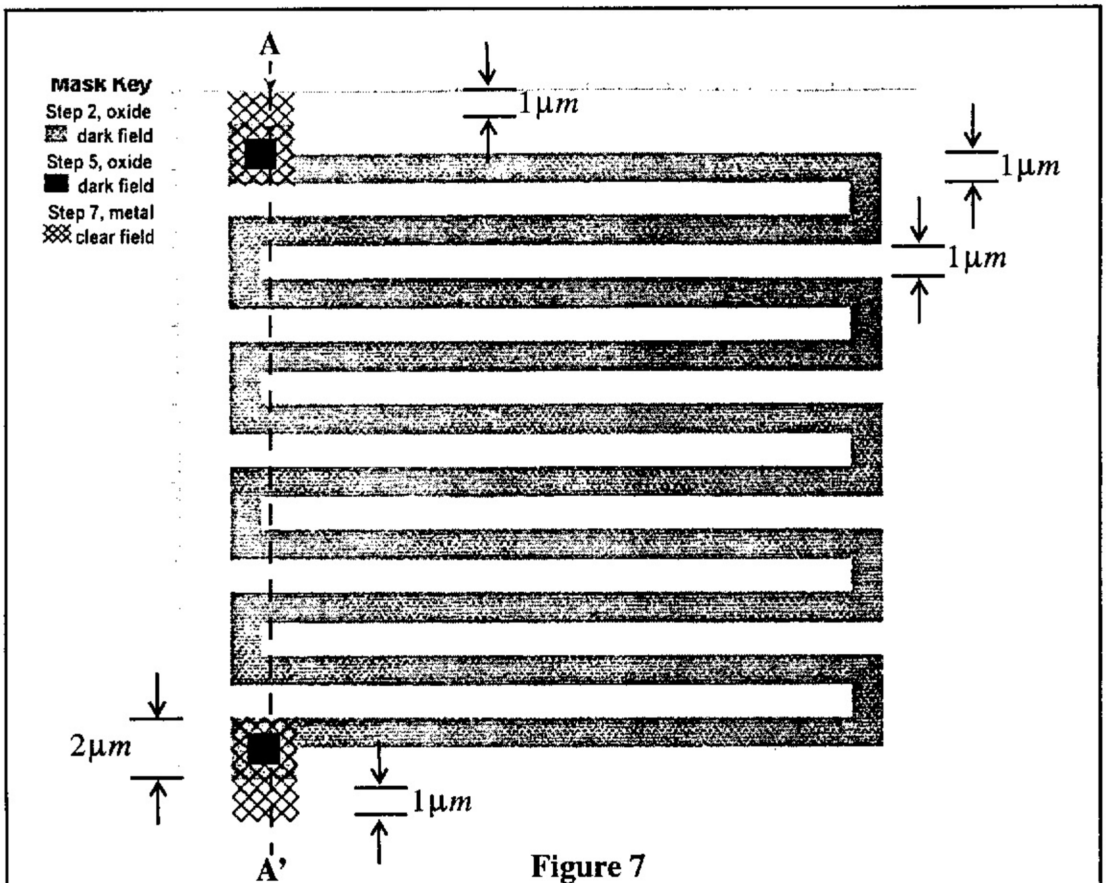
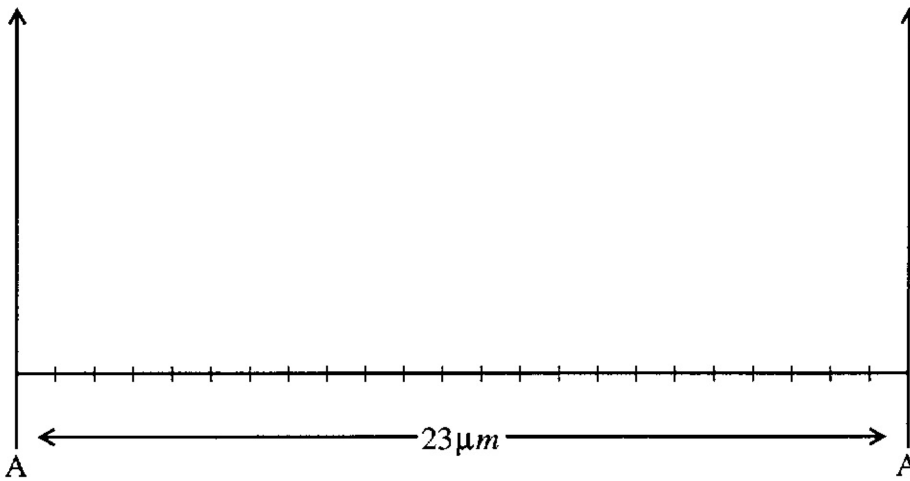


Figure 7

a) (10 points)
Draw a <u>neat</u> cross-section of the fabricated device for the cross-section **A-A'** shown in the figure.



b) (5 points)

Determine the sheet resistance of the diffusion layer in this technology.

Take $\mu_n = 300 \frac{cm^2}{v-s}$ and the charge of an electron as $-1.6 \times 10^{-19} C$. Make and explain approximations as necessary.

$R_s = \frac{\rho}{t} = \frac{1}{\sigma t}$ t = depth

$\sigma \cong \mu_n q N_D$ (ignore acceptor conc.)

$N_D = \frac{10^8/cm^2}{t}$ t = depth

$\sigma t = 300 \frac{cm^2}{V-S} \cdot (1.6 \cdot 10^{-19} C) \cdot 10^8/cm^2$

$= 4.8 \cdot 10^{-9} \Rightarrow R_s \simeq 0.2 \cdot 10^9 = 2 \cdot 10^8 \Omega$

7(a)

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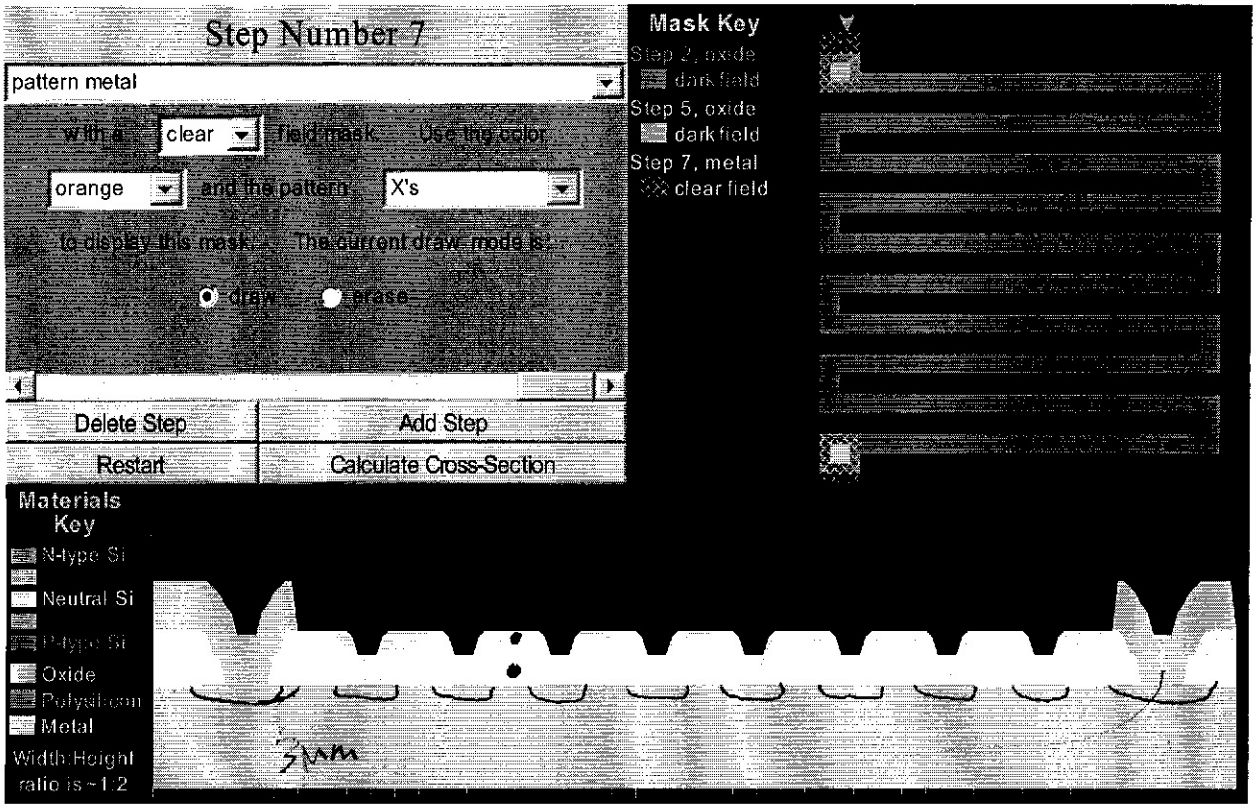

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