UNIVERSITY OF CALIFORNIA AT BERKELEY
EECS Department

EECS 40, Summer 2005
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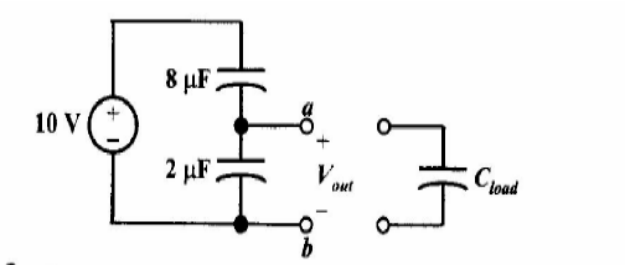
Homework #3

Due Tuesday, 7/12 at 6PM in HW Box (2nd floor lounge)
Total Points:

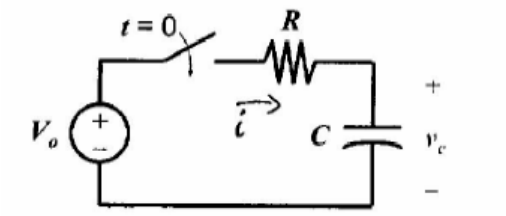
First Order Circuits

Problem 1

a) Consider the capacitive voltage-divider circuit below. Find V_{out}. How will V_{out} change if a small load capacitance $C_{Load} < 2\,\mu$F is connected between terminals a and b?

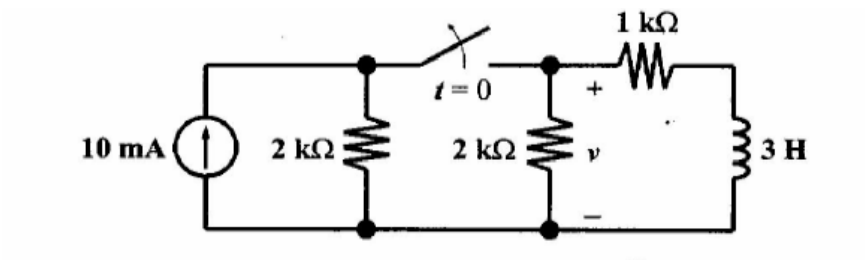


b) Consider the following RC circuit



Provide a physical reason why it takes longer for Vc to reach its final value if R is increased. (Why is the characteristic time constant proportional to R)

c) Assume that the circuit below is operating in steady state with the switch open for t < 0. Find and accurately sketch v(t) for all t.



Problem 2: P4.20 in the textbook.
Problem 3: P4.26 in the textbook
Problem 4: P4.33 in the textbook
Problem 5: P4.35 in the textbook

Second Order Circuits:

Problem 6: P4.48 in the textbook

Complex Impedances:

Problem 7: P5.41 from the textbook
Problem 8: P5.42 from the textbook
Problem 9: P5.43 from the textbook
Problem 10: P5.44 from the textbook