UNIVERSITY OF CALIFORNIA AT BERKELEY
EECS Department

EECS 40, Summer 2005
Octavian Florescu
Homework #7

Due Wed. 8/10 at 5P in HW Box (2nd floor lounge)
Total Points:

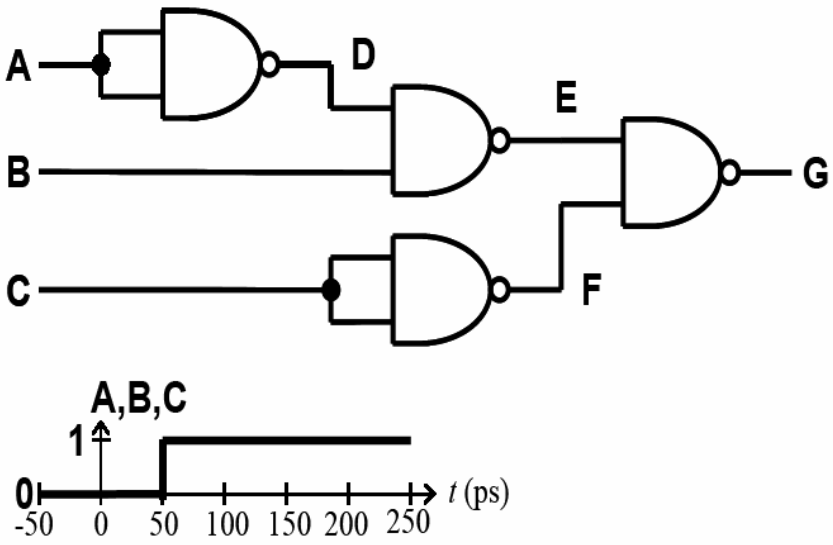
Representation of Numerical Data in Binary Form
Problem1: P7.5 in the textbook
Problem2: P7.6 in the textbook
Problem3: P7.8 in the textbook

Combinatorial Logical Circuits
Problem4: P7.24 in the textbook
Problem5: P7.27 in the textbook
Problem6: P7.29 in the textbook

Synthesis of Logic Circuits
Problem7: P7.42 in the textbook
Problem8: P7.43 in the textbook

Minimization of Logic Circuits
Problem9: P7.47 in the textbook
Problem10: P7.48 in the textbook

Propagation Delay
Problem11:
Assume each NAND gate in the logic circuit below has the propagation delay of ***tp* = 50 ps.** Note that the logic input signals **A**, **B** and **C** each change from 0 to 1 at time *t* = 50ps. Draw the timing diagram for the signals **D**, **E**, **F** and **G**, for times in the range *t* =0 to *t* =250ps .


A
B
C
D
E
F
G

A,B,C
1
0
t (ps)
-50
0
50
100
150
200
250