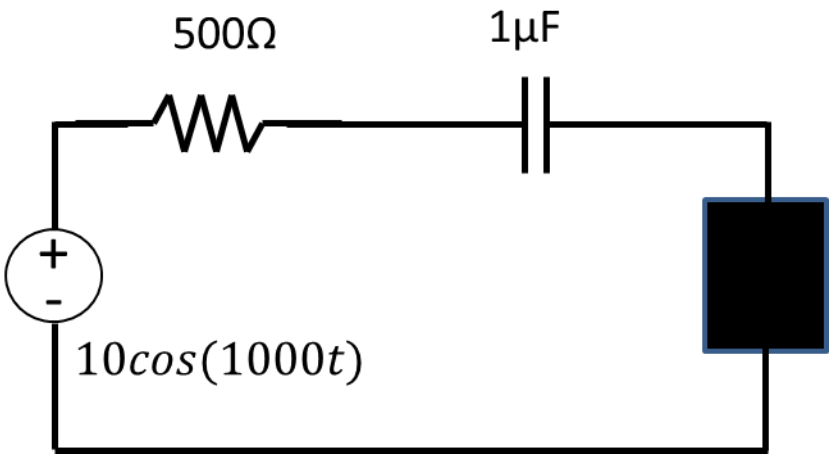
HW7, due July 3rd 2010 at 2 PM (Due in 240 Cory in the HW box)

1. Consider the circuit below. In this problem we'll analyze how much power is consumed by various circuit elements in the spot where the black box appears.



a. Assume that there is a 500Ω resistor inside the box.
   i. Find the voltage and current phasors for the voltage and current across the resistor in the box.
   ii. Find an expression for the power delivered to the box as a function of time (you will need to separately find $i(t)$ and $v(t)$ using your answer to part i)
   iii. Using your answer to part a.ii, find the average power delivered to the resistor (Calculus Hint: You can take as given that the average of the product of two cosines of magnitude 1 is 1/2)
   iv. Using the formula on page 759 of the book [13.151], calculate the average power through the resistor. (Formula is $avg(p) = \frac{1}{2}|V_i||I_i|\cos(\theta)$, where θ is the angle difference between the voltage and the current phasor, and the two quantities in the middle are the magnitude of the voltage and current phasors)
   v. Convert your voltage and current phasors for part i. into rectangular form, and calculate the average power through the resistor using formula 13.152 or 13.153. (Formula is $p = \frac{1}{2}Real[V_i I_i^*]$, where I_i^* is the complex conjugate of the current phasor)
   Your answer to parts iii, iv, and v should all be the same

b. Assume there is a 1H inductor in the box.
   i. Calculate the maximum amount of energy stored in the inductor in any way you choose.

ii. Calculate the average power consumed by the inductor in any way you choose. This is how much net energy you'd be getting from the power company.
iii. Calculate the average reactive power in the inductor in any way you choose. This is how much energy you're borrowing on average (but which you always give back to the power source)
iv. Calculate the average power consumed by the resistor in the original circuit (right next to the voltage source). This represents the resistance of the distribution equipment at the power company. This is how much energy is wasted in the process of you taking and giving back energy to the source
v. Extra (not for a grade): Note the maximum voltage in the inductor. Does the max voltage surprise you?

c. Choose a load (which you'll put in the box) that will draw the maximum average power. (Hint: You will need two components). How much power does it draw? (It should be more than your answer to part a.iii) [Hint: The load should be the conjugate of the impedance that the source sees in the open circuit case]

d. Choose a purely resistive load that will draw the maximum average power possible with only a resistor. How much power does it draw? (It will be greater than or equal to your answer to part a.iii, but less than your answer to part c) [Hint: to come]

e. What load would you connect to maximize the total power provided by the sources?

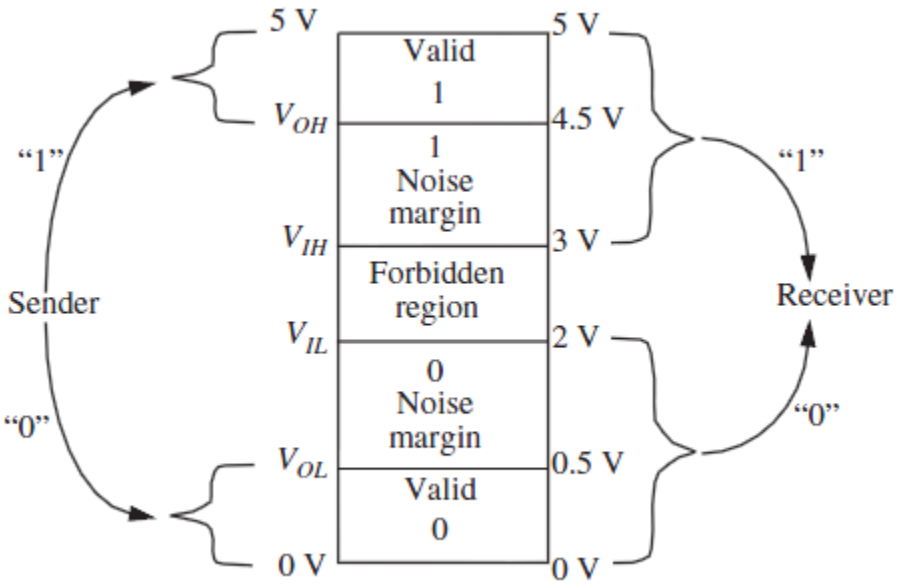
2. In this problem we'll analyze how we can compensate for inductive loads to avoid drawing large amounts of reactive power. A motor can be modeled as a resistor in series with an inductor.

a. Suppose we have a motor with resistance 5Ω and inductance $0.1H$. Assuming the motor is plugged directly into a 60Hz $(w = 377)$ 110 V outlet, how much average real power does the motor consume? How much average reactive power does the motor consume?
b. Now suppose we have 100 such motors in parallel. What is the average real and reactive power consumed in total by all 100 motors?
c. The power company will charge you for your large reactive power, because, as you saw in part a, the reactive power of your load means that they're still producing and dissipating energy as heat, even if you're not actually keeping the energy that they give you.

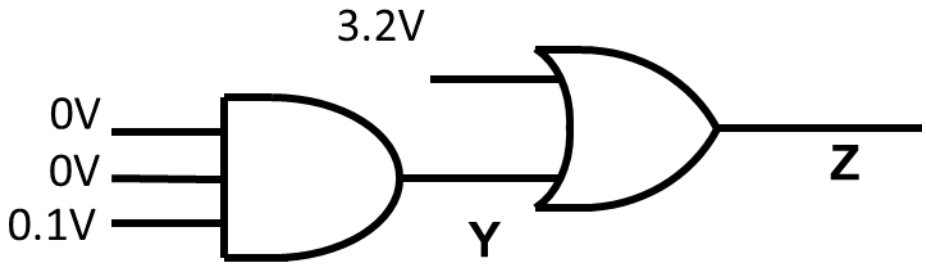
You can reduce your total reactive power by adding the correct load. In this case, you can place a single capacitor in series with your motor bank such that the reactive power is zero.

i. Find a capacitance such that the total reactive power is zero.
ii. What is the new average real power consumed total by all 100 motors added together? Compare your answer to the real power consumed in part b.

3. Suppose we have the static discipline as specified below:

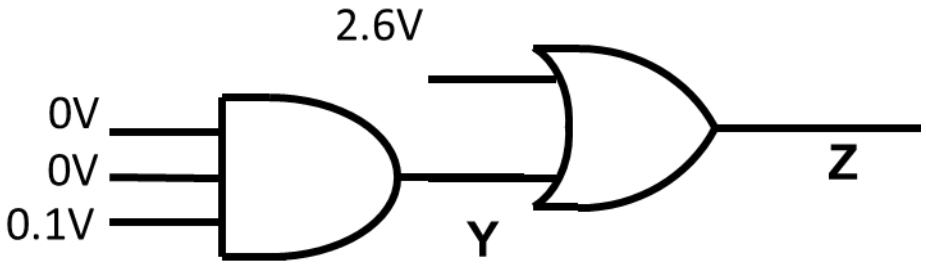


Suppose we have the network of logic gates with voltages as shown below. Recall that logic gates are a technology independent schematic of a circuit which is supposed to compute a logical function. By "technology independent", I mean that there are infinitely many circuits of {resistors, capacitors, inductors, op-amps, transistors, source, etc} that we can use to build a logic gate. The only thing that matters is that our circuit follows the rules set forth above. Thie static discipline is the contract that the logic gate designer must follow.

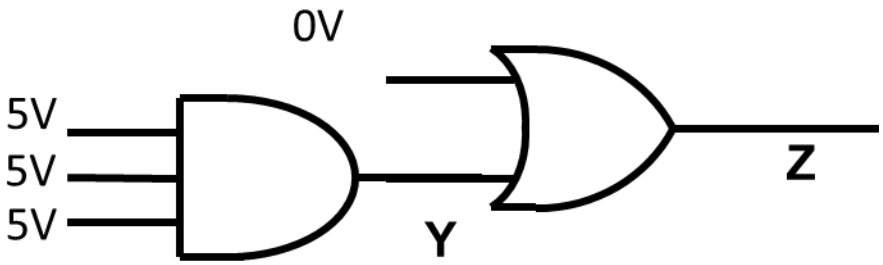


a. Given these input values and assuming this circuit obeys the static discipline above, what are the possible output voltages of Y and Z?

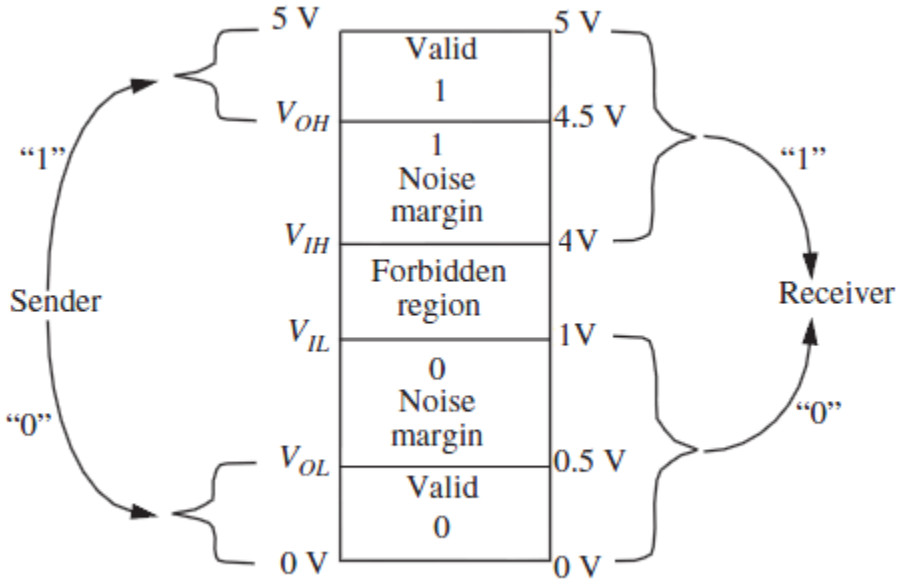
b. Now assume we have the following input voltages with the same circuit that follows the static discipline. What are the possible output voltages of Y and Z?



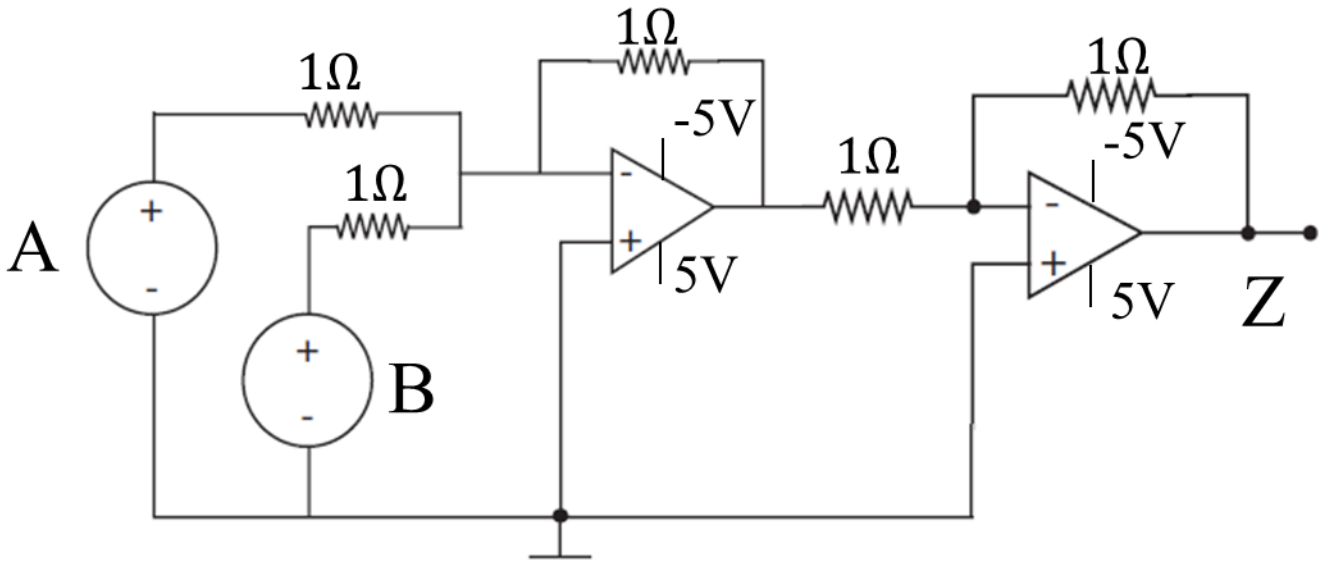
c. Lastly, given the following input voltages and the same circuit that follows the static discipline, what are the possible output voltages of Y and Z?



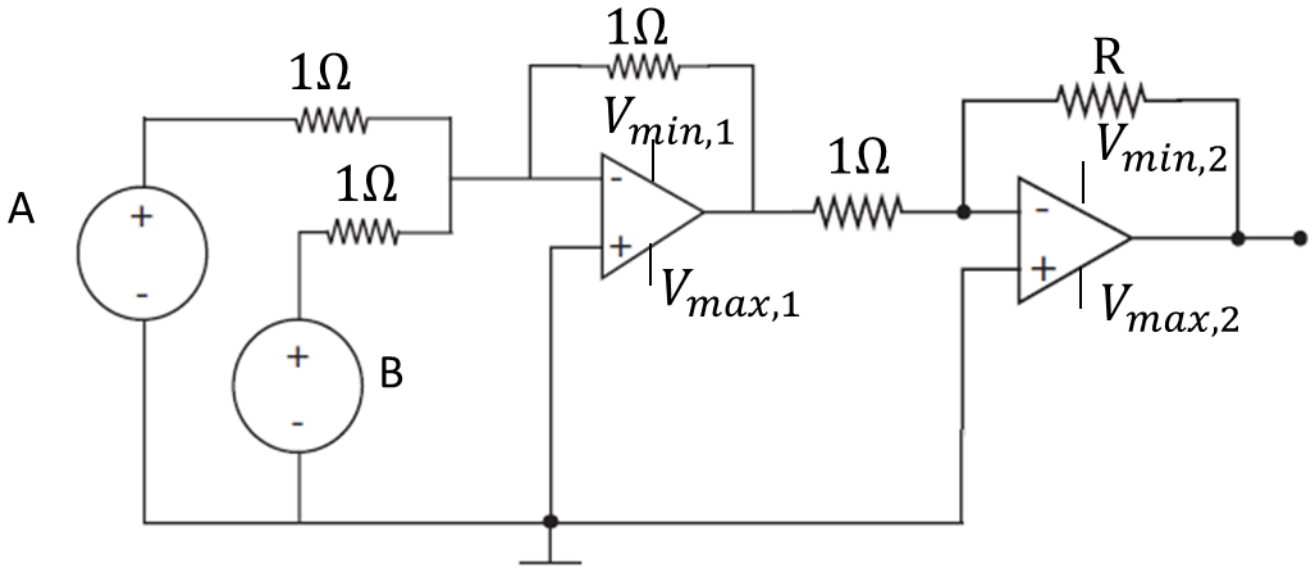
4. In this problem, use the following static discipline:



Consider the OR gate circuit that we discussed in class, which is supposed to implement $Z = A + B$:



a. The circuit above which we discussed in class is highly intolerant of noise. Show that this circuit violates the static discipline if $A = 0.9V$, $B = 0.9V$. What is the output voltage Z? What logic level [0, 1, or neither] does this correspond to in our static discipline? Why is this output voltage a violation?



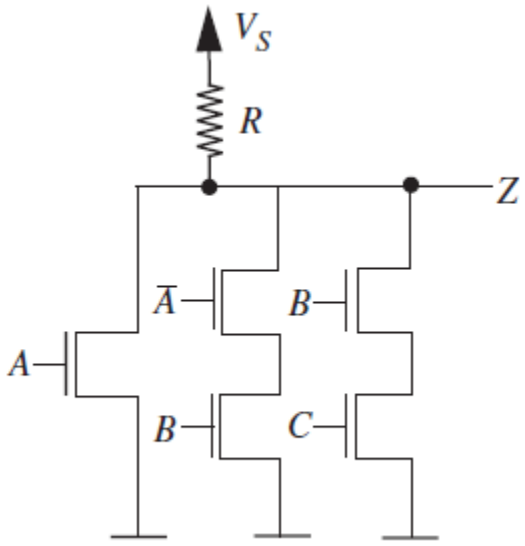
b. Now consider the circuit above. Find values of R, $V_{min,1}$, $V_{max,1}$, $V_{min,2}$,and $V_{max,2}$ such that this OR gate obeys the static discipline. This may take a few iterations of R and V values until you can meet all the constraints.

Interlude: As we discussed in class, MOSFETs make for a way simpler implementation of a logic gate than using op-amps, and indeed, this is pretty much how almost all logic gates are implemented! **For all of these problems, use the SR model of a MOSFET (on page 300 in the book), not the S model**.

5.

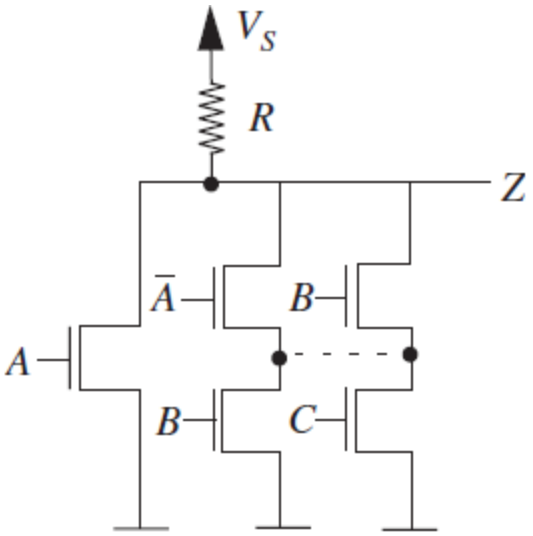
a. Write a truth table and a boolean equation relating the output Z to A, $\overline{A}$, B, and C, when these are input to the circuit shown in Figure 6.61.

For this problem, you can assume our pull-up resistor R is very large.



b. What is the role of the pull-up resistor? What would happen if we made it much much smaller?

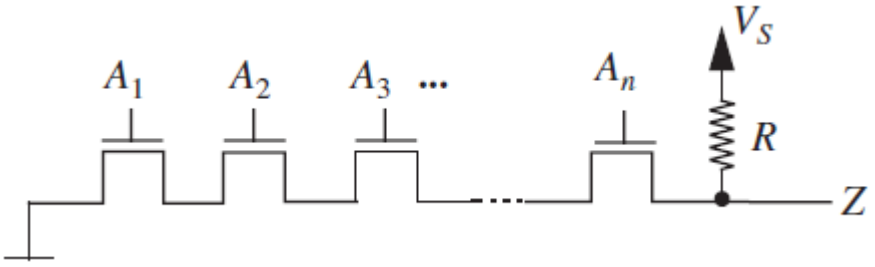
c. Suppose the circuit in Figure 6.61 suffers a manufacturing error that results in a short between the pair of wires depicted in Figure 6.62. Write a truth table and a boolean equation relating the output Z to A, $\overline{A}$, B, and C, for the resulting circuit.



We'll talk about everything you need for the next 5 problems on Friday. If you read ahead, chapter 6, section 10 covers questions 6 and 7. Chapter 11, section 4 covers question 8, and Chapter 11, section 5 covers questions 9 and 10. Finally, Chapter 10, section 4 covers problem 11. You should already be able to do 12 (and it should take you 5 minutes tops)

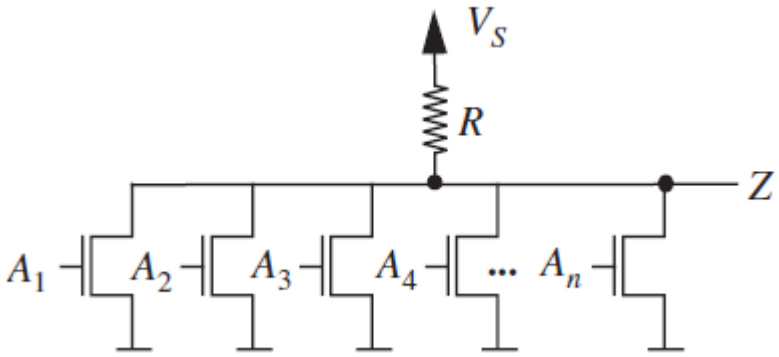
6. [The book forgot to mention that $V_s = 5$] for these problems

a) Consider a family of logic gates that operate under the static discipline with the following voltage thresholds: $V_{OL} = 1$ V, $V_{IL} = 1.3$ V, $V_{OH} = 4$ V, and $V_{IH} = 3$ V. Consider the N-input NAND gate design shown in Figure 6.63. In the design $R = 100k$ and R_{ON} for the MOSFETs is given to be $1k$. V_T for the MOSFETs is 1.5 V. What is the maximum value of N for which the NAND gate will satisfy the static discipline? What is the maximum power dissipated by the NAND gate for this value of N?



(fig 6.63)

b) Consider the N-input NOR gate shown in Figure 6.64. Assume that the on-state resistance of each of the MOSFETs is R_{ON}. For what set of inputs does this gate consume the maximum amount of power? Compute this worst-case power.



(fig 6.64)

7.

PROBLEM 11.2 Implement the logic function $Z = \overline{A + B + CD}$ using NMOS transistors alone. In other words, use an NMOS transistor in place of the pull-up resistor. Your implementation must satisfy a static discipline with low and high voltage thresholds given by $V_{IL} = V_{OL} = V_L$ and $V_{IH} = V_{OH} = V_H$, where $0 < V_L < V_T < V_H < V_S$. V_S is the power supply voltage. As your answer, specify the W/L values for the pullup and the pulldown transistors.

For what combination of inputs does the circuit dissipate the greatest amount of static power? Determine the static power dissipation for this combination of inputs.

Recall from class and page 305 that $R_{ON} = R_n \frac{L}{W}$ [You don't actually need R_n but if you get stuck you can pick an arbitrary R_n and that's fine. Hint1: What should be bigger, the resistance of the "pullup" or "pulldown" transistors? Hint2: All you need to do is pick $W_{up}, L_{up}, W_{down}, L_{down}$ to match your answer from Hint1]

8.

a. Implement the following functions using CMOS (i.e. only NMOS and PMOS in a complementary arrangement), assuming R_{ON} is $3{,}000\Omega$, with Logic $1 = 5V$ and Logic $0 = 0V$

i. $A + B$

ii. $\overline{A+B}$

iii. $(A+B)(C+D)$

iv. $\overline{(A+B)(C+D)}$

v. $\overline{A+B+CD}$

b. Did you actually need to know the on resistance of the MOSFETs to do this problem? Why or why not?

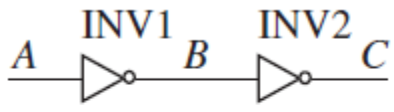
9. Take your network from problem 8 part v.

a. What is the static power dissipation? [Hint: This is really easy]
b. Assume that $A=0$, $B=0$, $C=0$, $D=1$ for a long time. If $A=1$, how much energy is dissipated as Z transitions from 1 to 0, assuming that your network is driving a gate capacitance of $30nF$?
c. **Extra not for a grade:** Now assume A switches between 0 and 1 every nanosecond. New problem: Explain why the dynamic power is very small ;.
d. Extra [not for a grade]: To make part c easier, calculate the rise and fall times.

10. What are the advantages and disadvantages of implementing a logic gate using CMOS vs. an implementation that uses only NMOS?

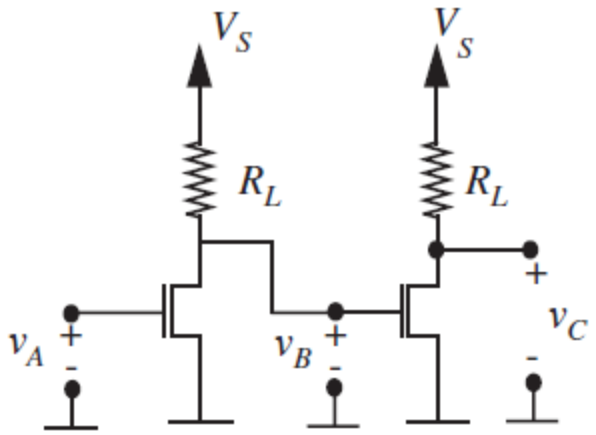
11. [Note this problem might get moved to HW8 depending on how far we get Friday]

PROBLEM 10.1 Figure 10.92a illustrates an inverter *INV*1 driving another inverter *INV*2. The corresponding equivalent circuit for the inverter pair is illustrated in Figure 10.92b. A, B, and C represent logical values, and v_A, v_B, and v_C represent voltage levels. The equivalent circuit model for an inverter based on the SRC model of the MOSFET is depicted in Figure 10.93.



(a)

FIGURE 10.92



(b)

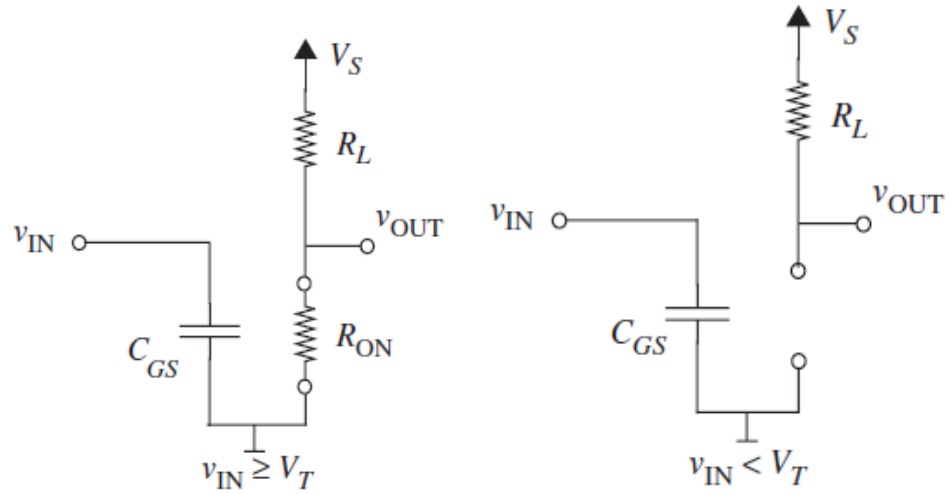


FIGURE 10.93

Assume $R_{on} = 1K\Omega, R_L = 10K\Omega, C_{GS} = 1nF, V_S = 5V$ and the circuit is supposed to obey a static discipline where $V_L = 1V, V_H = 3V$.

i. What is the rise time of INV1?
ii. What is the fall time of INV1?
iii. What is the propagation delay of INV?

12. Do the magnitude bode plot of the following transfer function, labeling your y axis in dB $[|H(jw)|_{in\ db} = 20\log_{10}(|H(jw)|)]$:

$$H(j\omega) = \frac{j\omega}{1 + j\omega}$$