# EE40
# Lecture 15
# Josh Hug

7/30/2010

# Logistics

- HW7 due Tuesday
- HW8 will be due next Friday
- Homeworks will be less mathematically intense starting with the second half of HW7
- Details on Project 2 demo and Mini-Midterm 3 details on Monday

# Midterm 2

- I can show you your midterm 2 grade, but problem 5 needs regrading [most people will get 3 to 6 more points]
- At the moment, mean is 102 and standard deviation is 24
- First midterm was mean 103, standard deviation 20
- Some oochness will happen here

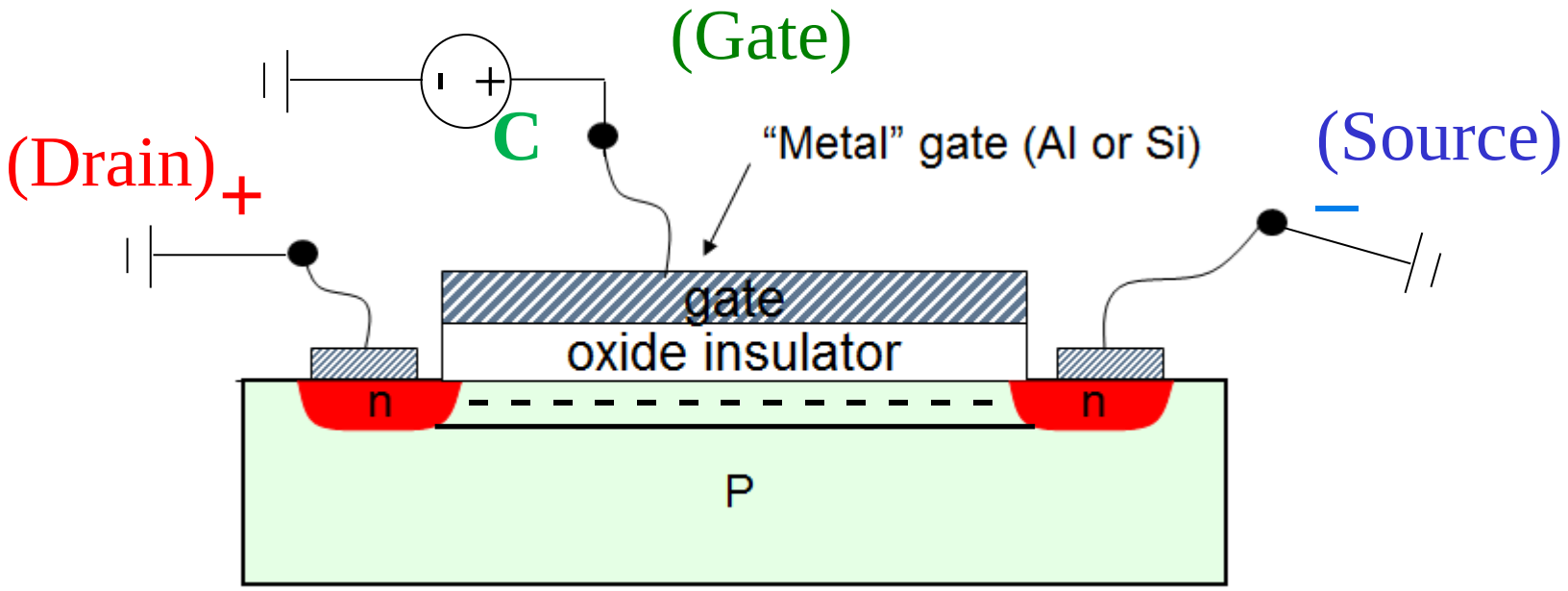
# Logic Gates and Static Discipline

- (On the board before we started)

# iClicker Warmup

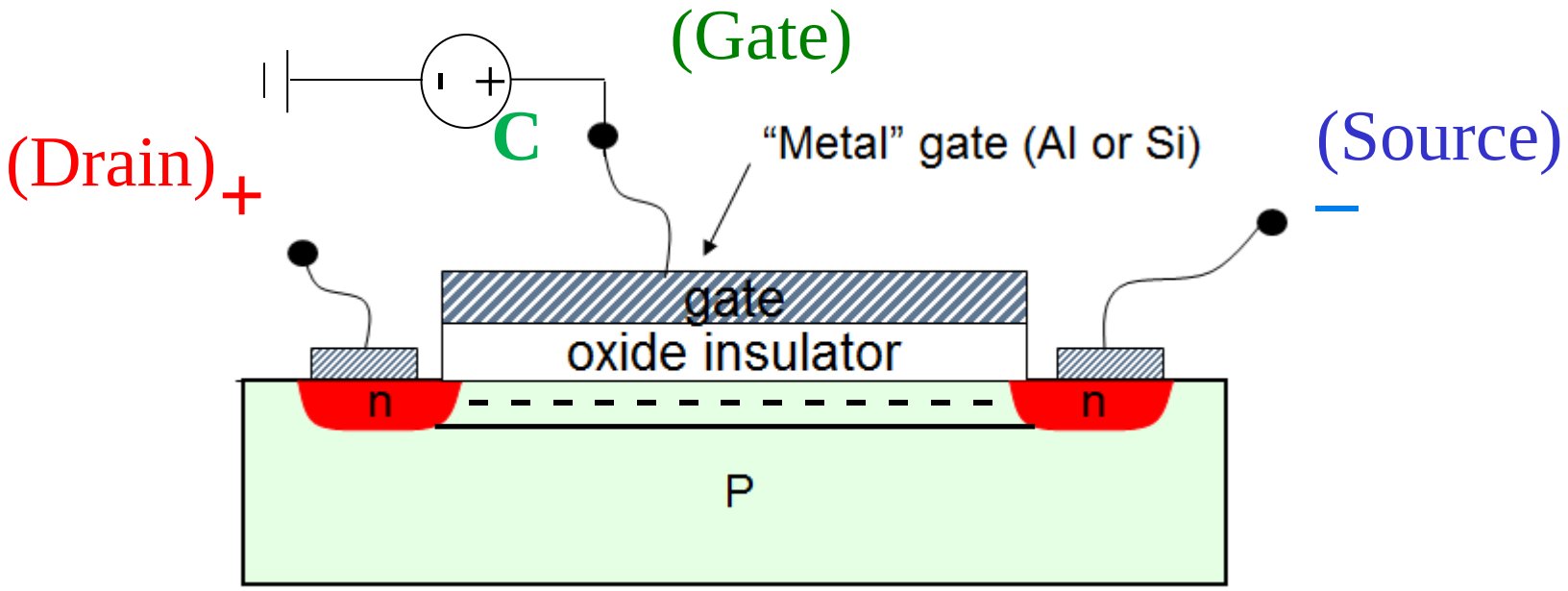
- We're going to have a ton of iClicker questions today
- A quick warmup. Have you played Starcraft 2?
  A. Yes
  B. No
  C. Starwhat?

# Field Effect Transistor



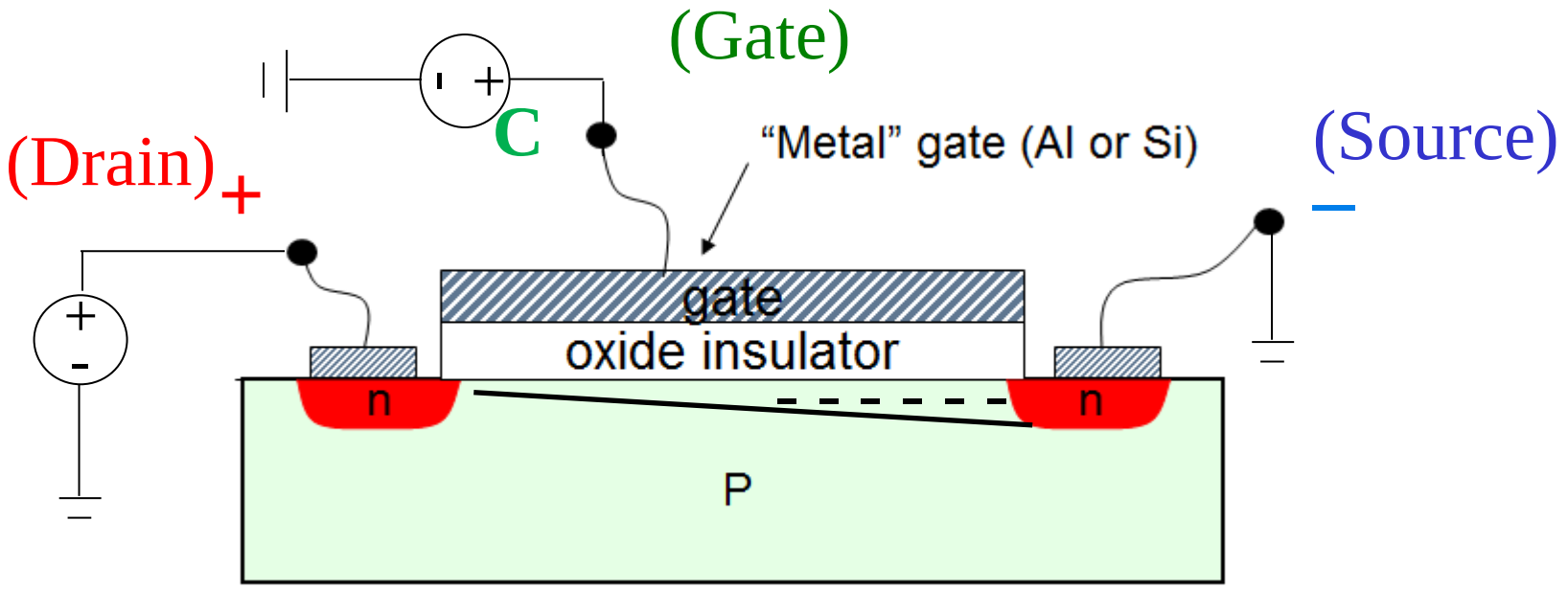

- P is (effectively) a high resistance block of material, so current can barely flow from **+** to **–**
- The n region is a reservoir of extra electrons (we will discuss the role of the n region later)
- When **C** is "on", i.e. $V_c$ is relatively positive, then electrons from inside the P region collect at bottom of insulator, forming a "channel"

# Field Effect Transistor




- When the channel is present, then effective resistance of P region dramatically decreases
- Thus:
  - When **C** is "off", switch is open
  - When **C** is "on", switch is closed

# Field Effect Transistor




- If we apply a positive voltage to the plus side
  - Current begins to flow from + to –
  - Channel on the + side is weakened
- If we applied a different positive voltage to both sides?

# Field Effect Transistor Summary

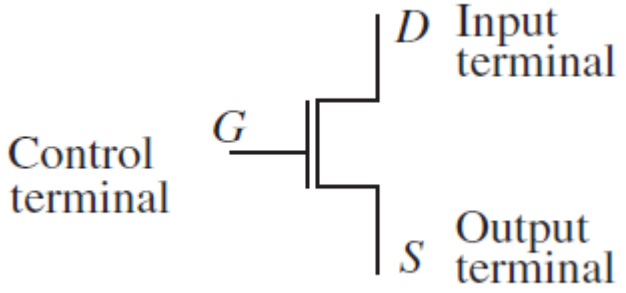
- “Switchiness” is due to a controlling voltage which induces a channel of free electrons
- Extremely easy to make in unbelievable numbers
- Ubiquitous in all computational technology everywhere

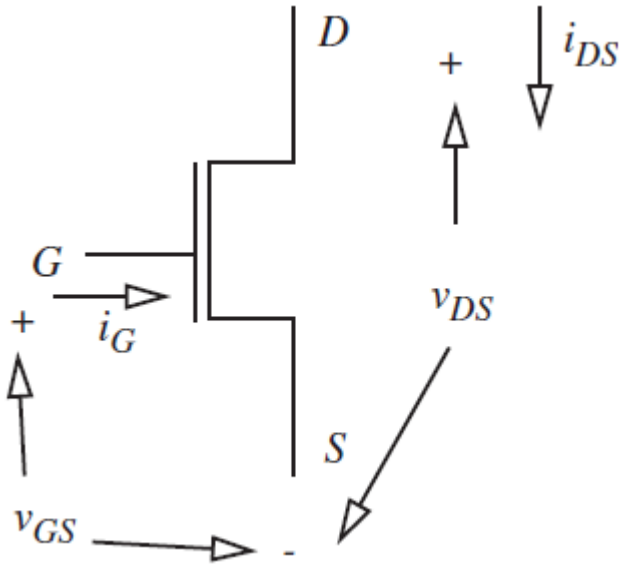
# Discussion Today

- In discussion today, we'll go over the physics of MOSFETs for those of you who are curious
- Time permitting, we'll discuss at a future date in class as well (so yeah, it will be slightly redundant)

# MOSFET Model

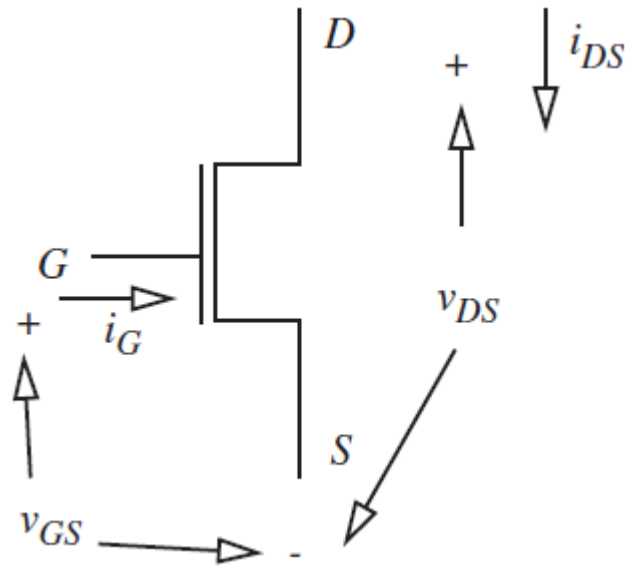
- Schematically, we represent the MOSFET as a three terminal device
- Can represent all the voltages and currents between terminals as shown to the right

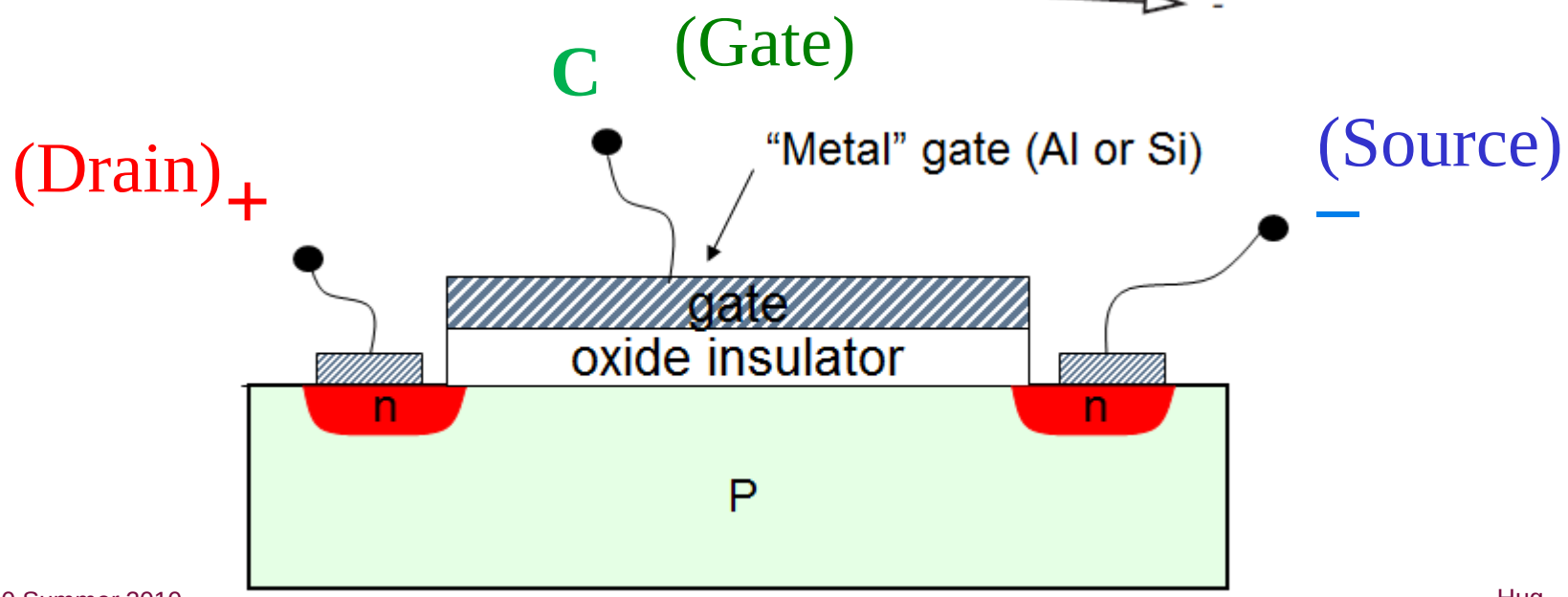


# MOSFET Model

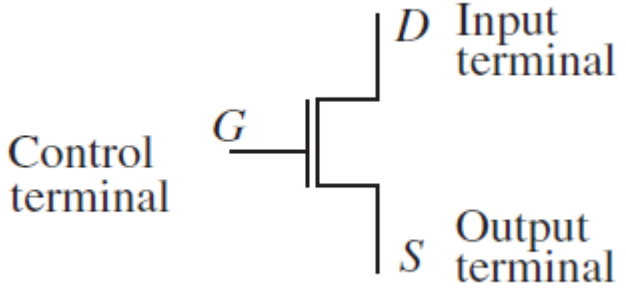
- What do you expect $i_G$ to be?

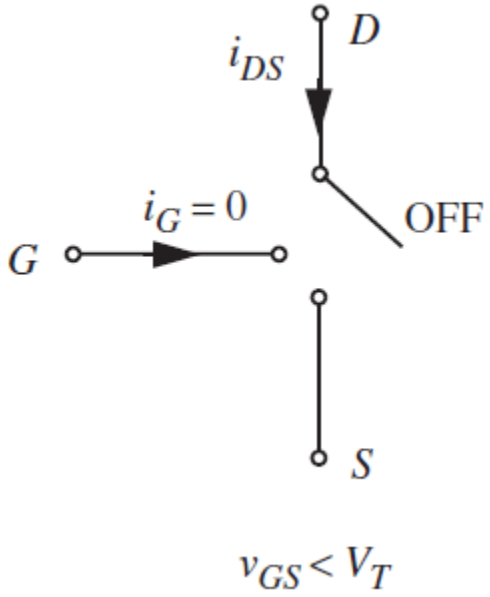


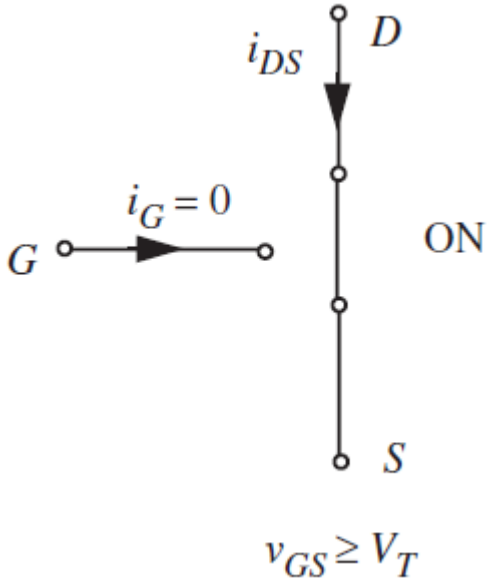



# S Model of the MOSFET

- The simplest model basically says that the MOSFET is:
  - Open for $V_{GS} < V_T$
  - Closed for $V_{GS} > V_T$

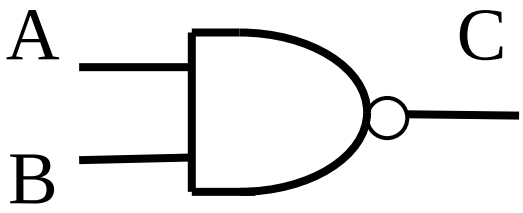


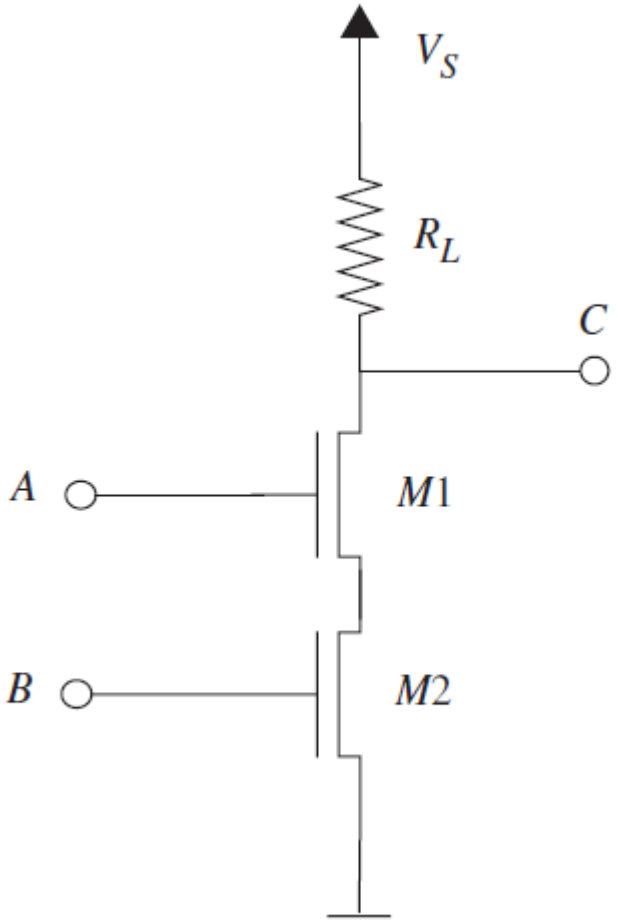



# Building a NAND gate using MOSFETs

- Consider the circuit to the right where $V_S$
- On your worksheet, we'll show that $C = \overline{AB}$
- Demonstration also on page 294 of the book

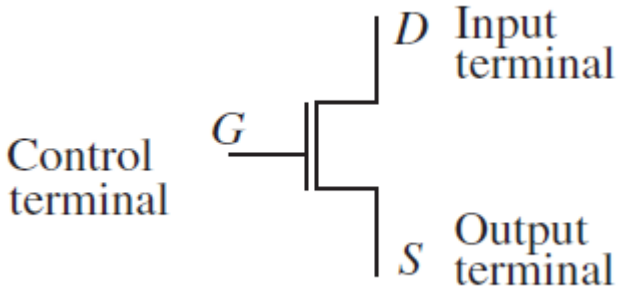


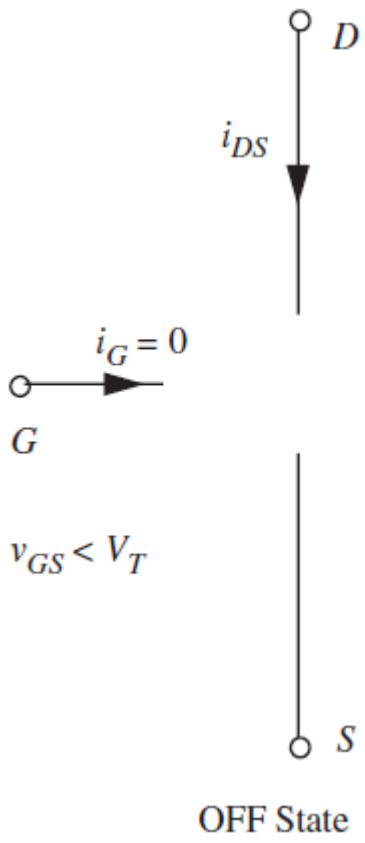



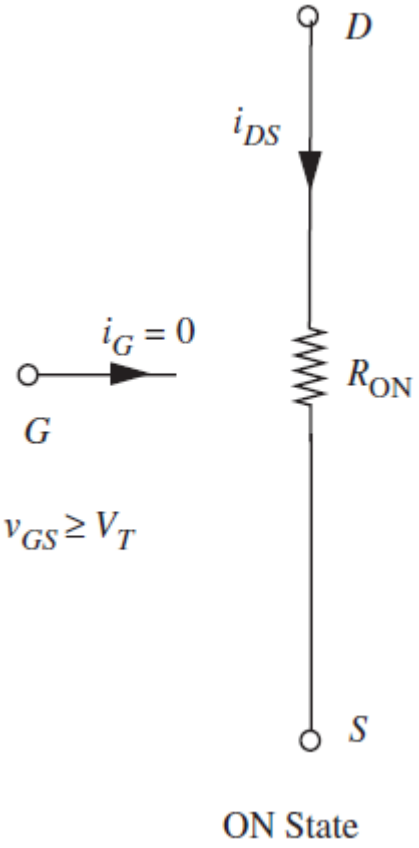
# MOSFET modeling

- MOSFET models vary greatly in complexity
- For example, an “ON” MOSFET has some effective resistance (not an ideal switch)
- We will progressively refine our model of the MOSFET
  - Will add capacitance later today
  - If we have time in the next 2 weeks, we will also talk about using MOSFETs as analog amplifiers which will necessitate an even better model

# SR Model of the MOSFET




$$i_{DS} = \frac{V_{DS}}{R_{ON}}, V_{GS} \geq V_T$$
$$= 0, \quad V_{GS} < V_T$$

[Has nothing to do with SR flip-flop]

# NAND with the SR Model

- What is $V_C$ when either of the inputs is low?
- Draw the equivalent circuit when both inputs are high. What is $V_C$?

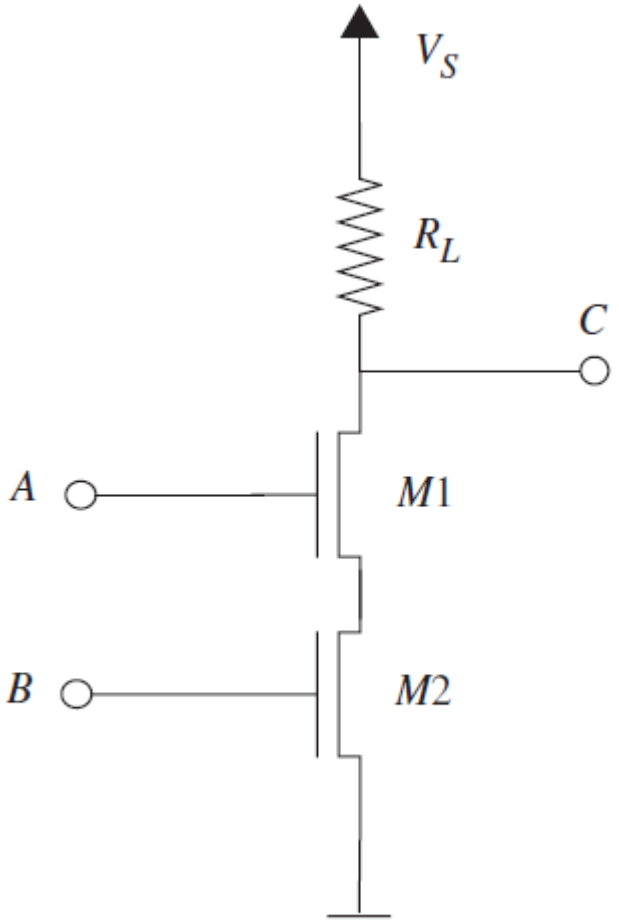
*A.* $V_S$

*B.* $0$

*C.* $V_S/R_L$

*D.* $V_S \dfrac{2R_{ON}}{R_L+2R_{ON}}$

*E.* $V_S \dfrac{R_L}{R_L+2R_{ON}}$




Q2

# NAND with the SR Model

- Assume static discipline requires $0 < V_{OL} < 0.5\text{V}$ and $4.5\text{V} < V_{OH} < 5V$
- Assume $R_L$ is $100k\Omega$
- Choose a $V_S$ such that the static discipline for $V_{OH}$ is met:

  A. $5V$

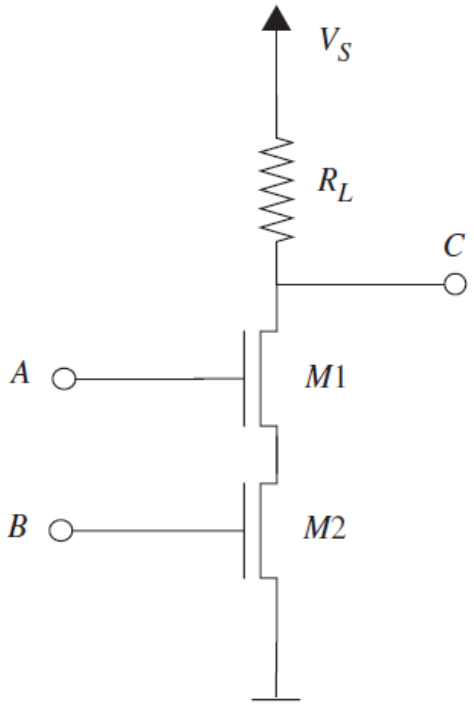
  B. $4.5V$

  C. $0.5V$

  D. $0V$

$$\text{O}_{\text{High}}: V_C = V_S$$

$$\text{O}_{\text{Low}}: V_C = V_S \frac{2R_{ON}}{R_L + 2R_{ON}}$$



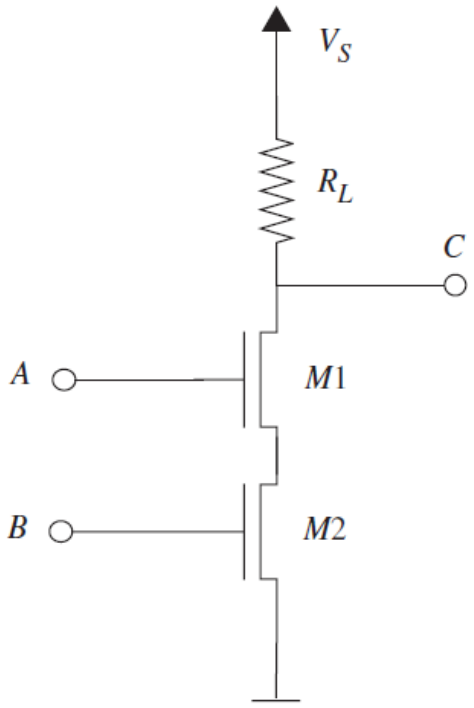

Q3

# NAND with the SR Model

- Assume static discipline requires $0 < V_{OL} < 0.5\text{V}$ and $4.5\text{V} < V_{OH} < 5V$
- Assume $R_L = 10k\Omega$ and $Vs = 5V$
- Choose an $R_{ON}$ and $R_L$ such that $V_{OL}$ meets the static discipline

$$\text{O}_{\text{High}}: V_C = V_S$$

$$\text{O}_{\text{Low}}: V_C = V_S \frac{2R_{ON}}{R_L + 2R_{ON}}$$




**Note: $R_L$ is usually called a "Pull-up resistor"**

Q4

# Another SR Model Example

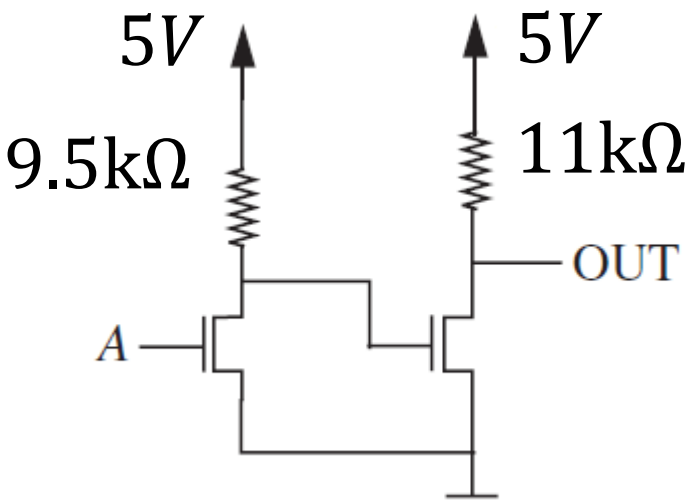
- Replace the left MOSFET with the equivalent circuit when A is high
- What is $V_{GS}$ on the right NMOS if A is high?

A. $5V$

B. $5\frac{1}{1+9.5}$

C. $5\frac{1}{1+11}$

D. $0$




$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

Q5

# Another SR Model Example

- When A is on,

  $V_{GS,right} = 5\frac{1}{1+9.5} = 0.476V$

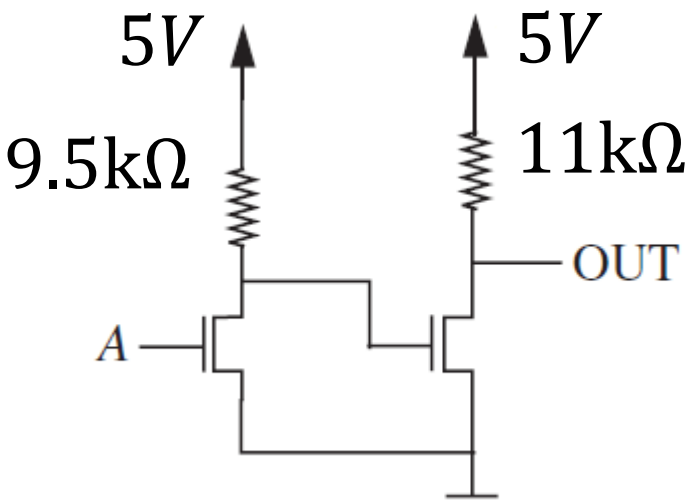
- What is $V_{OUT}$ when A is high?

  A. $5V$

  B. $5\frac{1}{1+9.5}$

  C. $5\frac{1}{1+11}$

  D. $0$



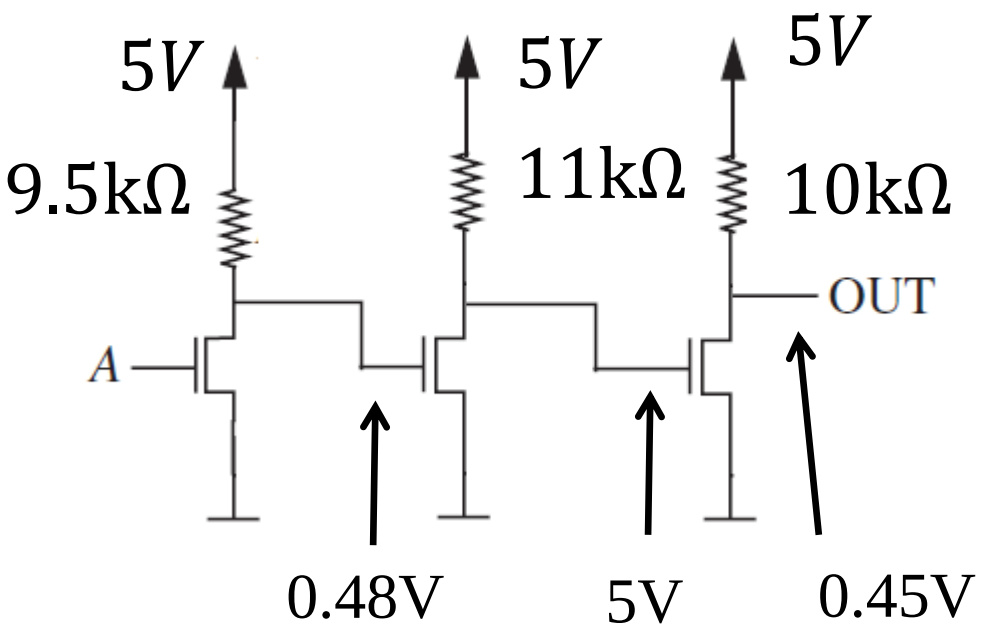

$R_{on} = 1k\Omega$

$V_T = 1V$

Q6

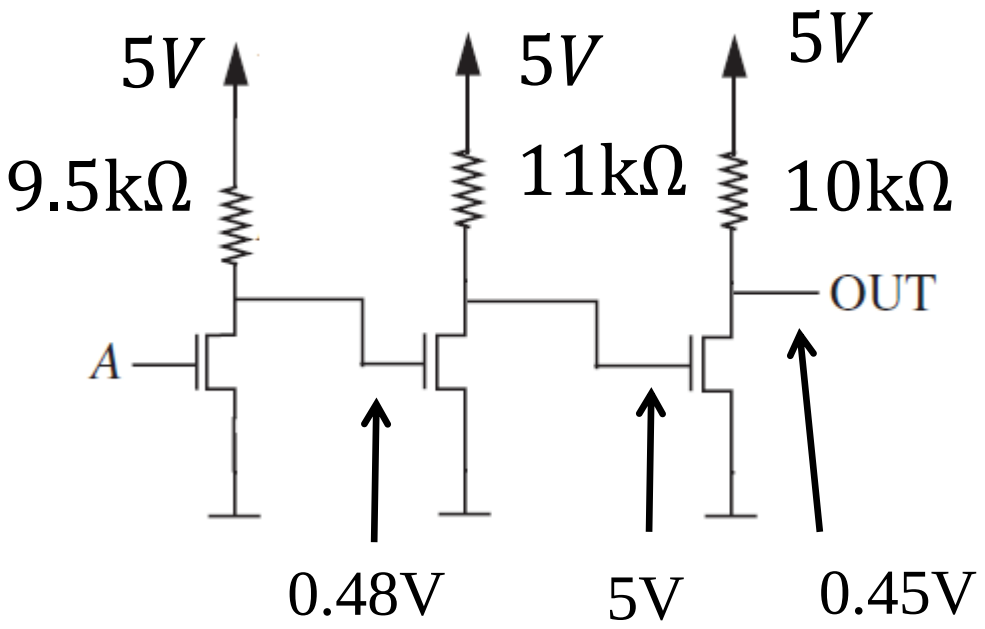
# The power of digital circuits

- At each stage, circuit **restores** the signal
- Can think of each MOSFET as diverting the 5V or 0V power supply into the next gate
- Tolerant to noise and manufacturing error

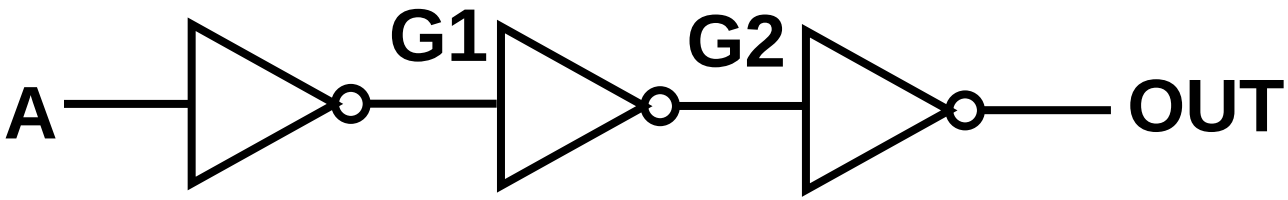


# The power of digital circuits

- How much noise could we tolerate on the input of the 2nd gate?
- On the input of the 3rd gate?




$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

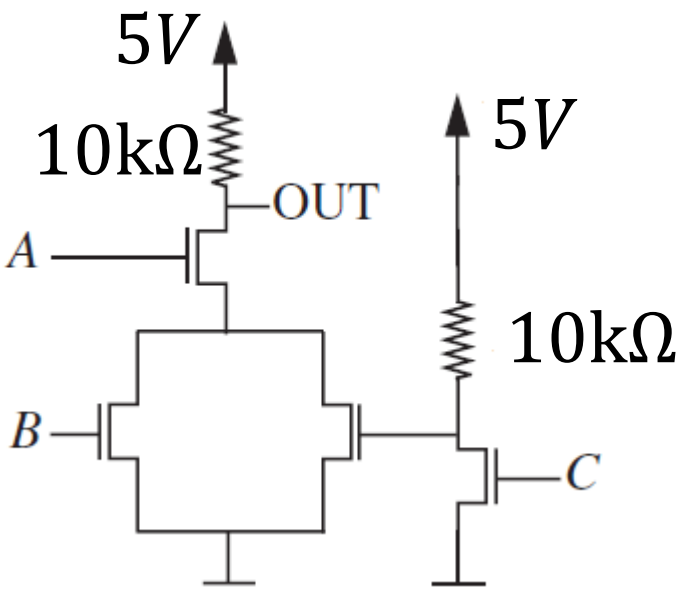


# The power of digital circuits (literally)

- Like all circuits, digital circuits consume power
- Amount of power will be dependent on state of our MOSFET switches

# Power Example

- What is the power dissipation when A=1, B=1, C=0?
- First, draw circuit with ON MOSFETS replaced with resistors
- Then, calculate $P_s$

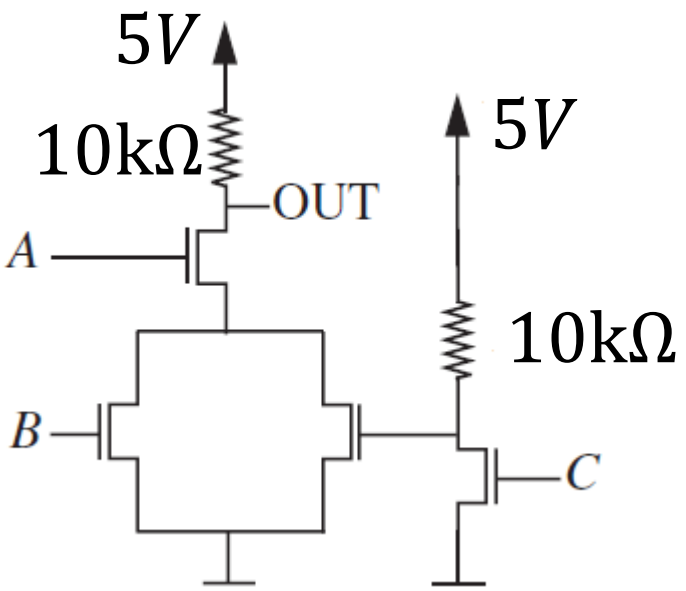



$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

Q7

# Power Example

- In general, power consumption will depend on which inputs are high and which are low
- "Worst case analysis" is when we pick the set of inputs which consumes the most power



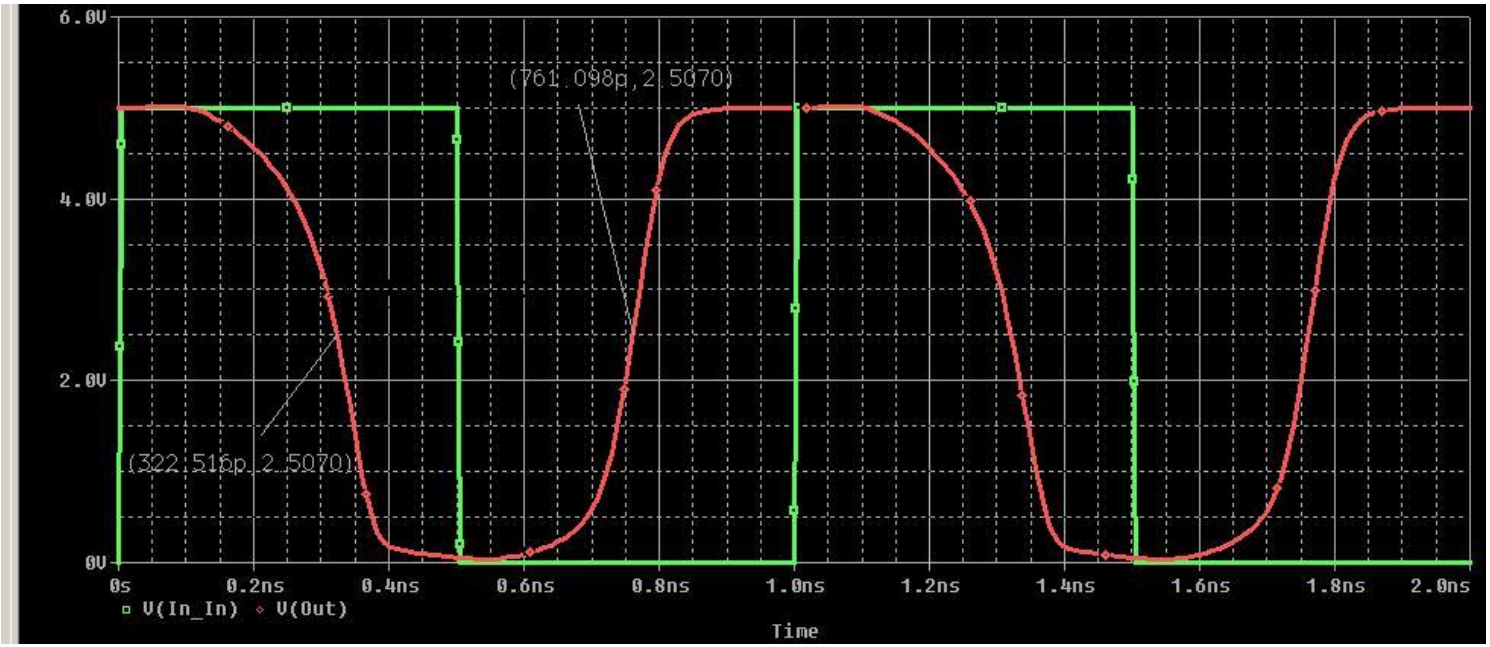

$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

# Static Power

- Using only NMOS to implement our gates will result in a gate which constantly eats up power
  - If you wire such a gate up on a breadboard, it will hum along using power all day
- Later today, we will see a technique called CMOS to avoid this static power dissipation
- But first, let's discuss delay

# The SRC Model of an NMOS Transistor

- So far, our NMOS implementation of logic gates allow for instantaneous switching
- In real life, of course, an NMOS implementation will take some non-zero time to switch

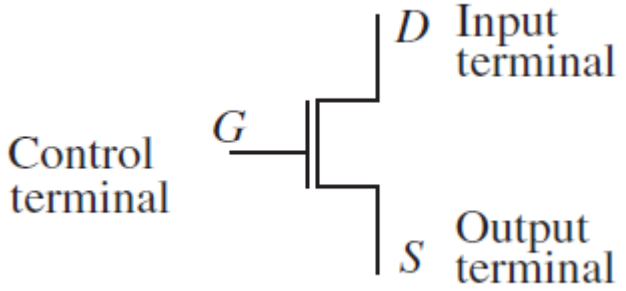


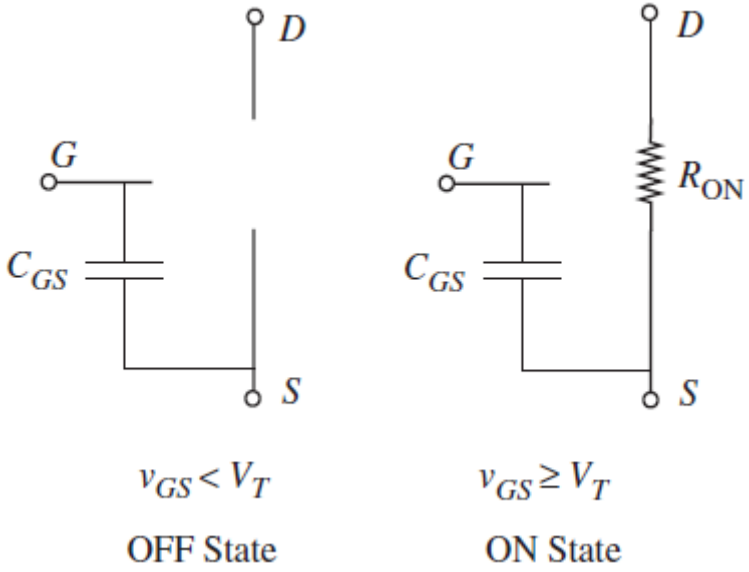

Green: Inverter Input

Red: Inverter Output

# The SRC Model

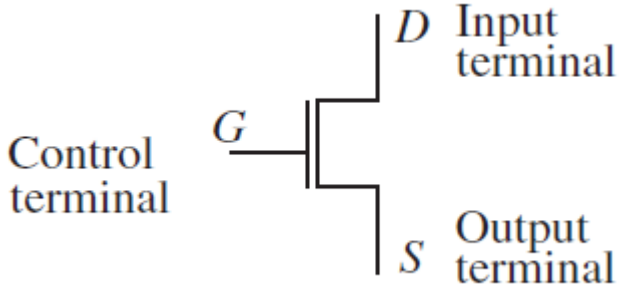
- The SRC Model is almost identical to the SR model, except that each gate node has a capacitance
- Like SR model: open when OFF and resistive when ON
- Note that now $i_G$ is non-zero!

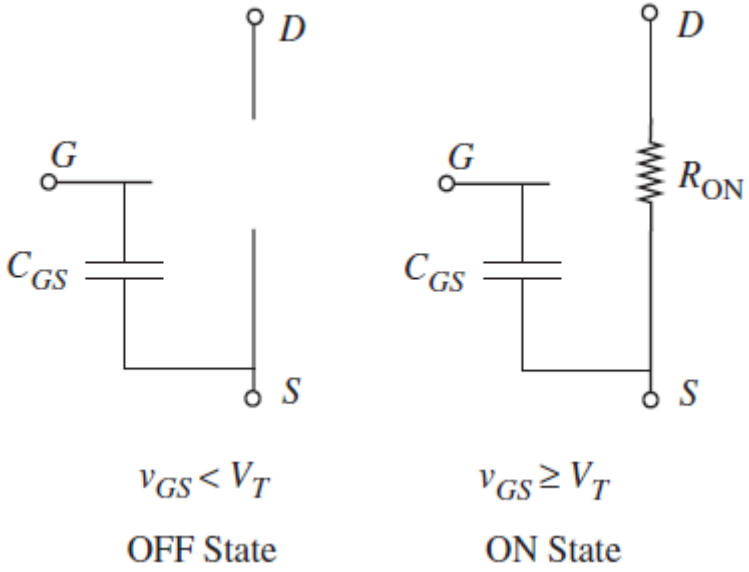


# The SRC Model

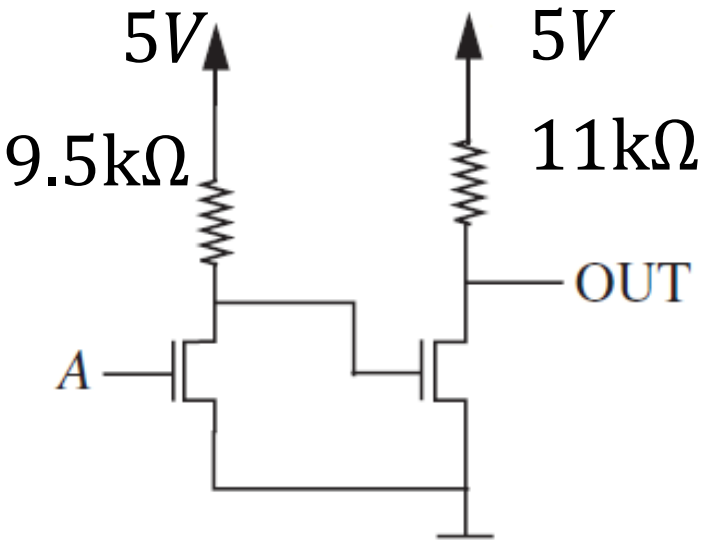
- Useful for modeling:
  - Gate delay: Takes time to charge up
  - Dynamic power: $i_G \neq 0$



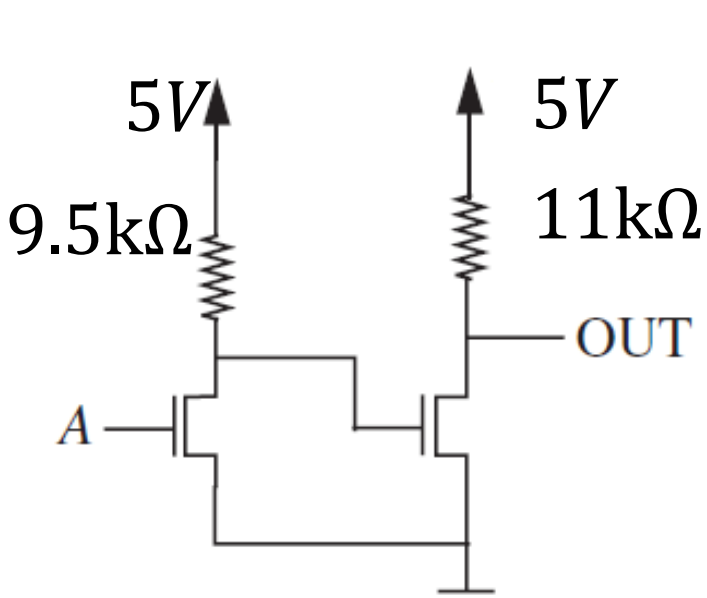



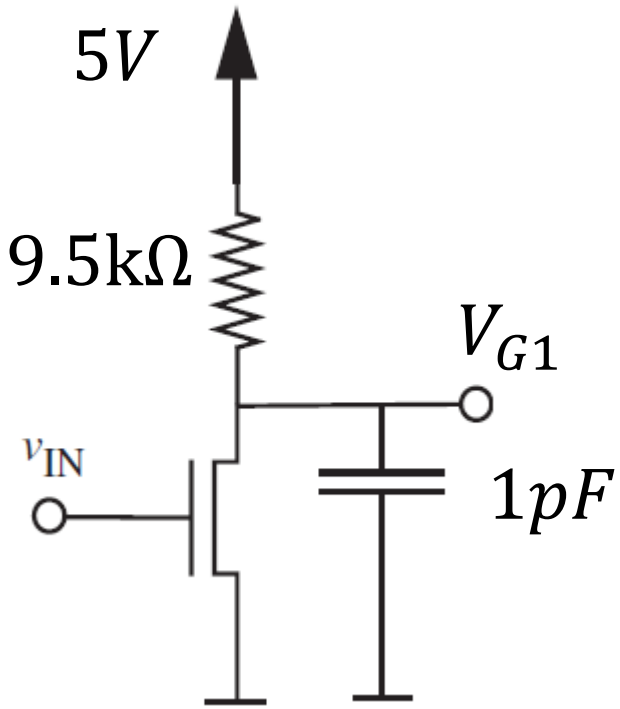
# SRC Model

- Consider our familiar pair of inverters
- We're going to focus on the behavior of our left inverter
- Let's assume that both MOSFETs have a gate capacitance of $1pF$ or $10^{-12}F$



# SRC Model of our 2 Inverters

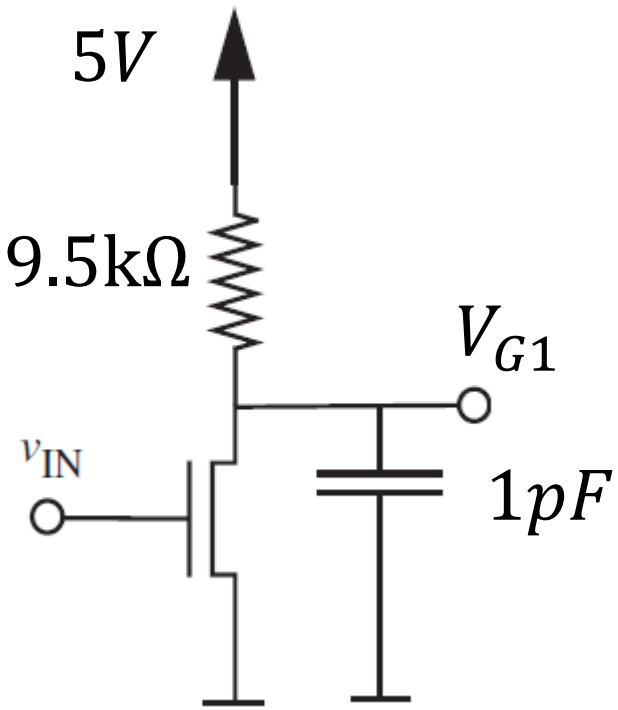



- We decide to ignore the function of the gate on the right, keeping it in mind only because we know we'll have to charge it

# Analysis of SRC Model

- When the gate voltage $V_{IN}$ has been less than $V_T$ (i.e. the gate capacitor is not charged) for a long time, what is $V_{G1}$?
  - A. $0V$
  - B. $5V$
  - C. $5\frac{1}{1+9.5}V$
  - D. $5\frac{1}{(1+9.5)10^{-12}}V$



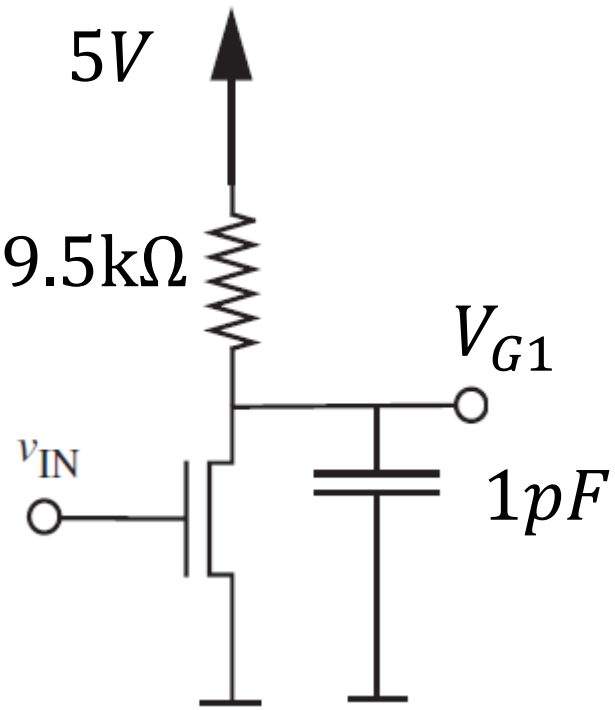

$R_{on} = 1k\Omega$

$V_T = 1V$

Q8

# Analysis of SRC Model

- Now assume $V_{in}$ has been low for a long time and thus $V_{G1} = 5V$
- If the logic gate upstream of $V_{in}$ rises above 1V, the SRC model of the left MOSFET says it should instantly switch to “ON”
- Draw the equivalent circuit on the MOSFET worksheet

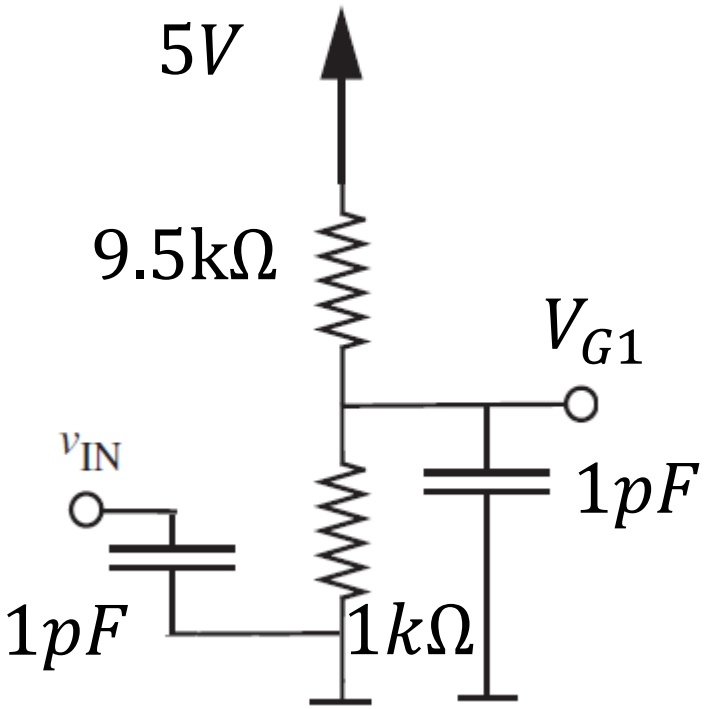



$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

Q9

# Analysis of SRC Model

- If $V_{G1} = 5V$, and the $1k\Omega$ resistor suddenly appears at t=0
- What is $V_{G1}(\infty)$?
  - A. $0V$
  - B. $5V$
  - C. $5\frac{1}{1+9.5}V$
  - D. $5\frac{1}{(1+9.5)10^{-12}}V$



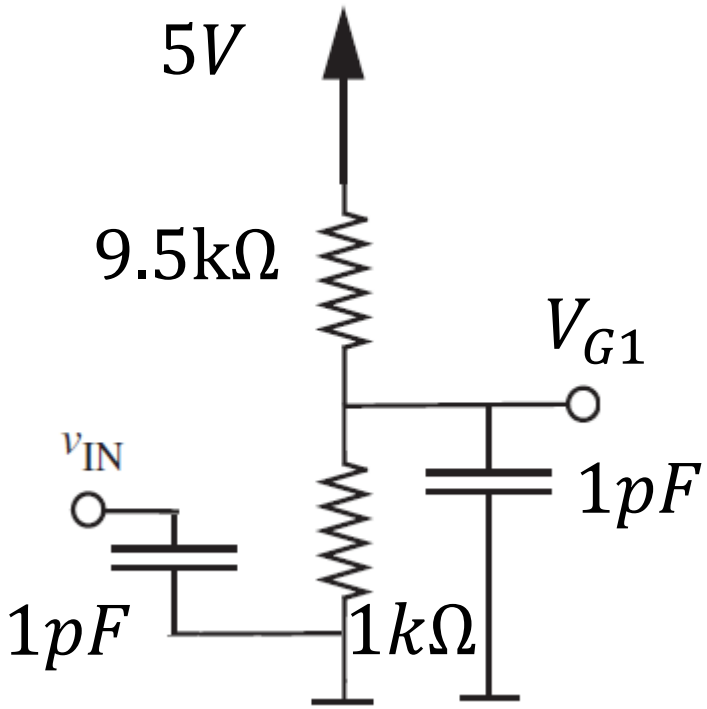

$R_{on} = 1k\Omega$

$V_T = 1V$

Q10

# Timing Analysis of the SRC model

- What is the time constant for the discharge of $V_{G1}$?
  - A. $10^{-12}$
  - B. $10^{-12} \times 1000$
  - C. $10^{-12} \times (9500 + 1200)$
  - D. $10^{-12} \times (9500 \parallel 1200)$
  - E. $2 \times 10^{-12} \times (9500 + 1200)$

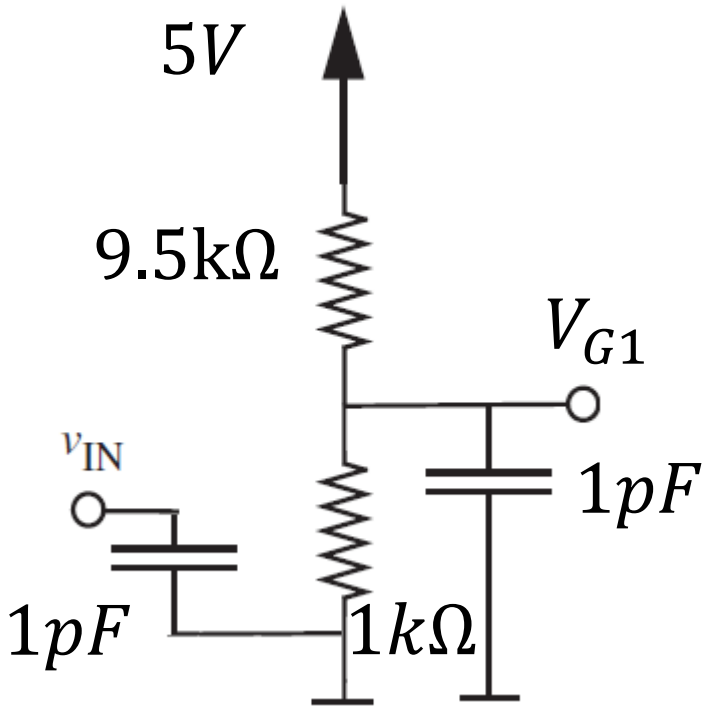



$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

Q11

# Timing Analysis of the SRC model

- Since $V_{G1}(0) = 5V$, $V_{G1}(\infty) = 0.476V$, and $\tau \approx 1ns$, then:
- $V_{G1}(t) = (5 - 0.476)e^{-t/\tau} + 0.476$
- How long will it take for the next inverter in the chain to turn on?

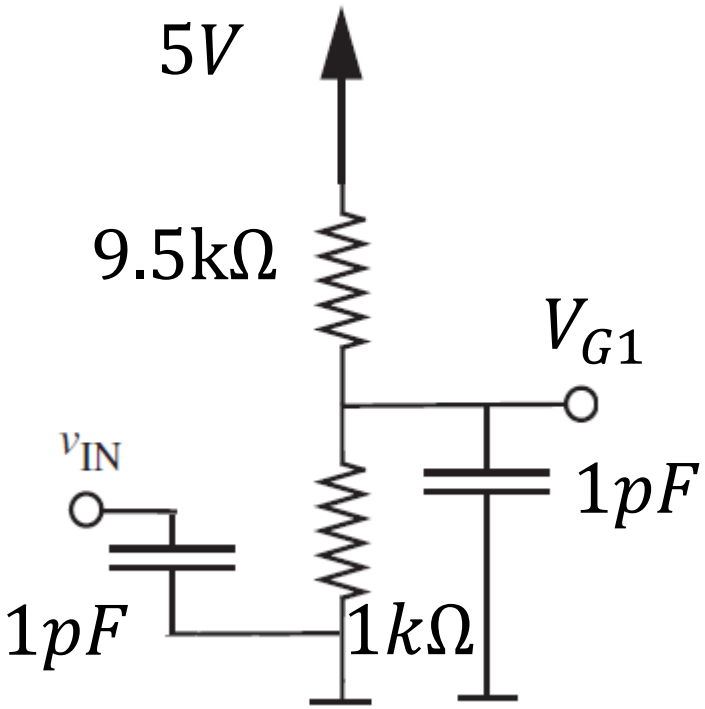



$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

$$\tau = 10^{-12} \times (9500 \parallel 1200) = 1.06 \times 10^{-9}$$

# Timing Analysis of the SRC model

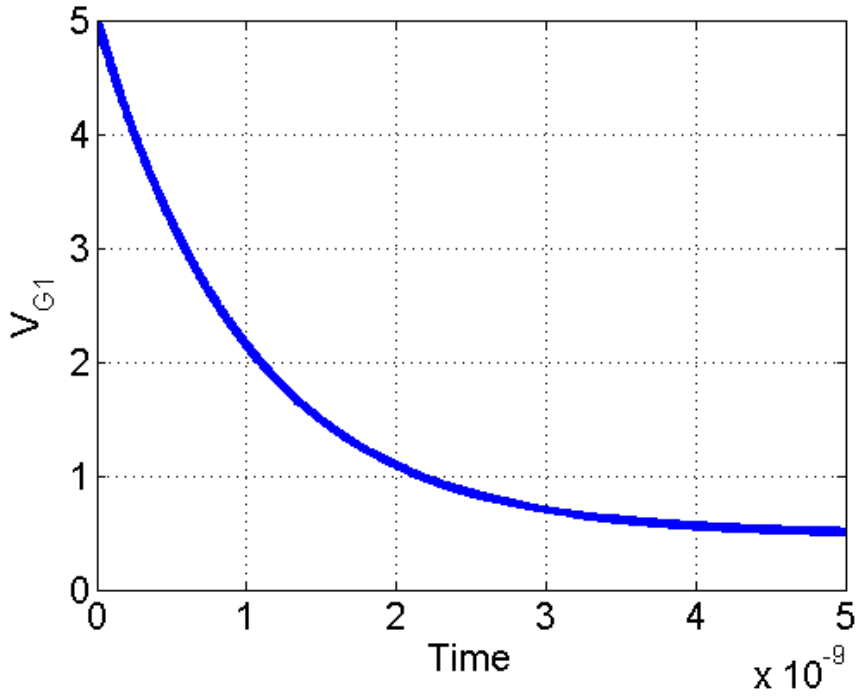
- $(5 - 0.476)e^{-t_{fall}/\tau} + 0.476 = 1$
- $-\tau \ln(0.1158) = t_{fall}$
- So $t_{fall} = 2.2ns$
- We call this the "**Fall Time**": gives time for $V_{G1}$ to fall from 5V to 1V

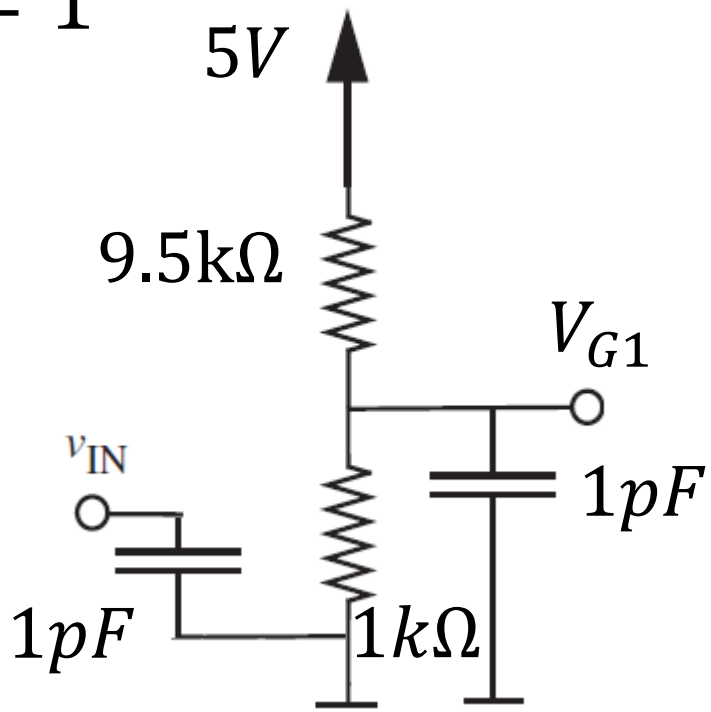



$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

# Fall Time

- $(5 - 0.476)e^{-t/\tau} + 0.476 = 1$
- $\tau \approx 10^{-9}$
- Gives: $t_{fall} = 2.2ns$



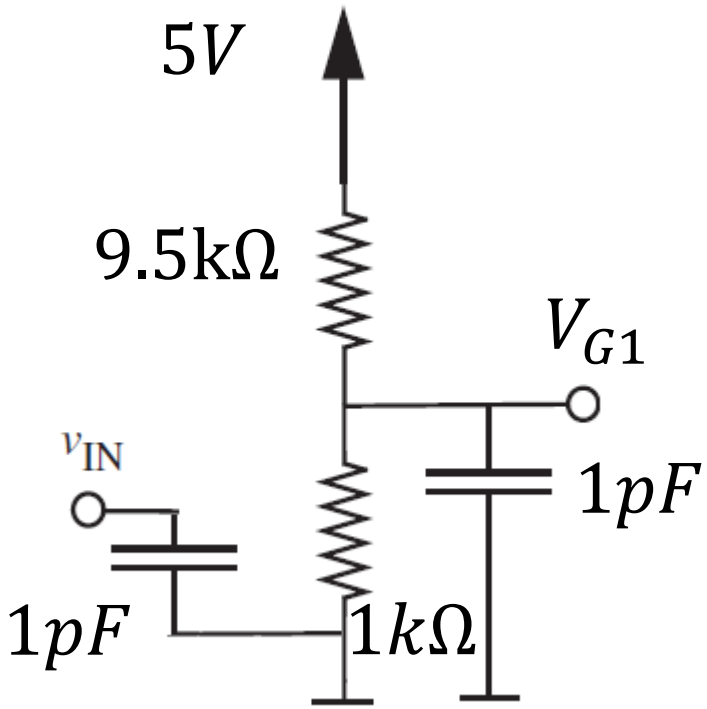




$R_{on} = 1k\Omega$

$V_T = 1V$

# Timing Analysis of the SRC model

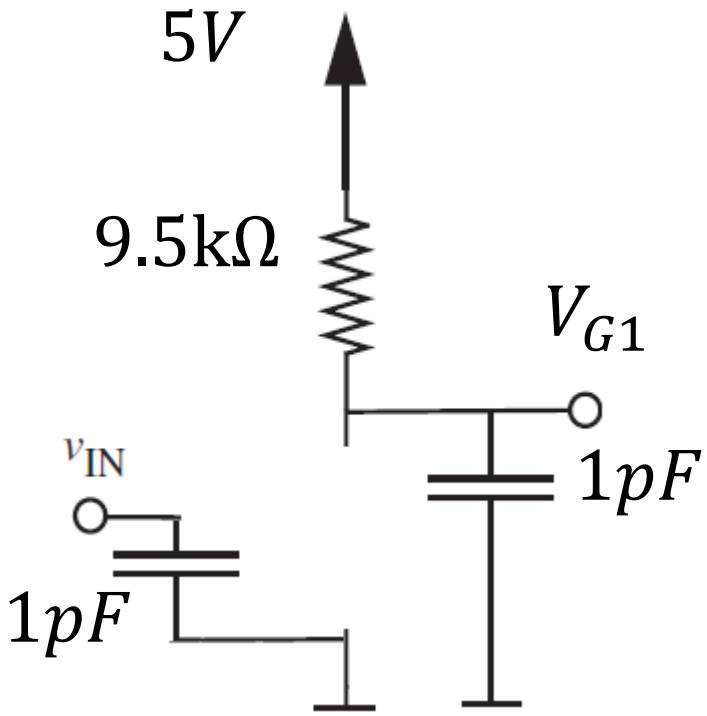
- How do we find the **Rise Time**?
- Have to replace by new equivalent circuit where:
  - Capacitor is initially discharged (0.476 V)
  - Switch is open




$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

# Timing Analysis of the SRC model

- How do we find the **Rise Time**?
- Have to replace by new equivalent circuit where:
  - Capacitor is initially discharged (0.476 V)
  - Switch is open
- $V_{G1} = (0.476 - 5)e^{-t/\tau} + 5$
- $\tau = 10^{-12} \times 9500 \approx 10ns$




$R_{on} = 1k\Omega$

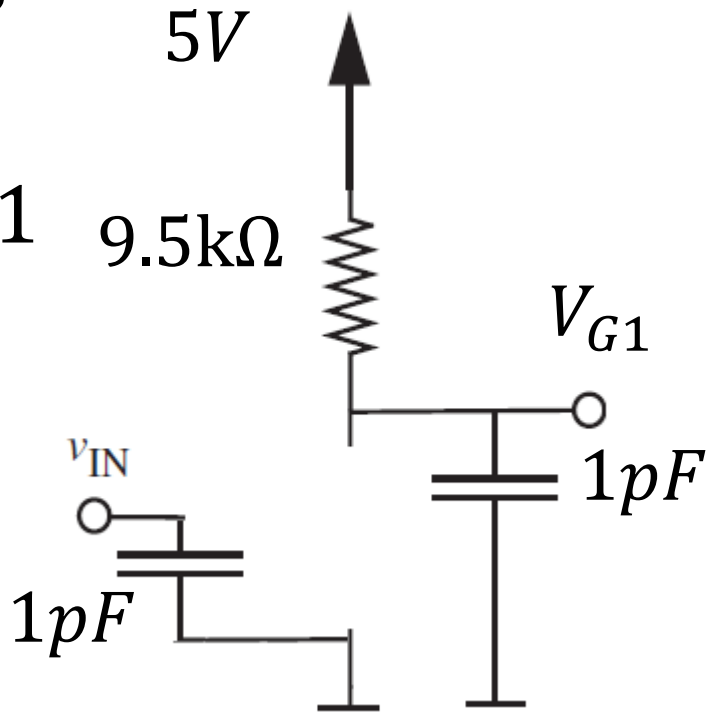
$V_T = 1V$

# Timing Analysis of the SRC model

- $V_{G1} = (0.476 - 5)e^{-t/\tau} + 5$
  $\tau = 10^{-12} \times 9500 \approx 10ns$
- $(0.476 - 5)e^{-t_{rise}/\tau} + 5 = 1$

$$-\tau \ln(0.884) = t_{rise}$$

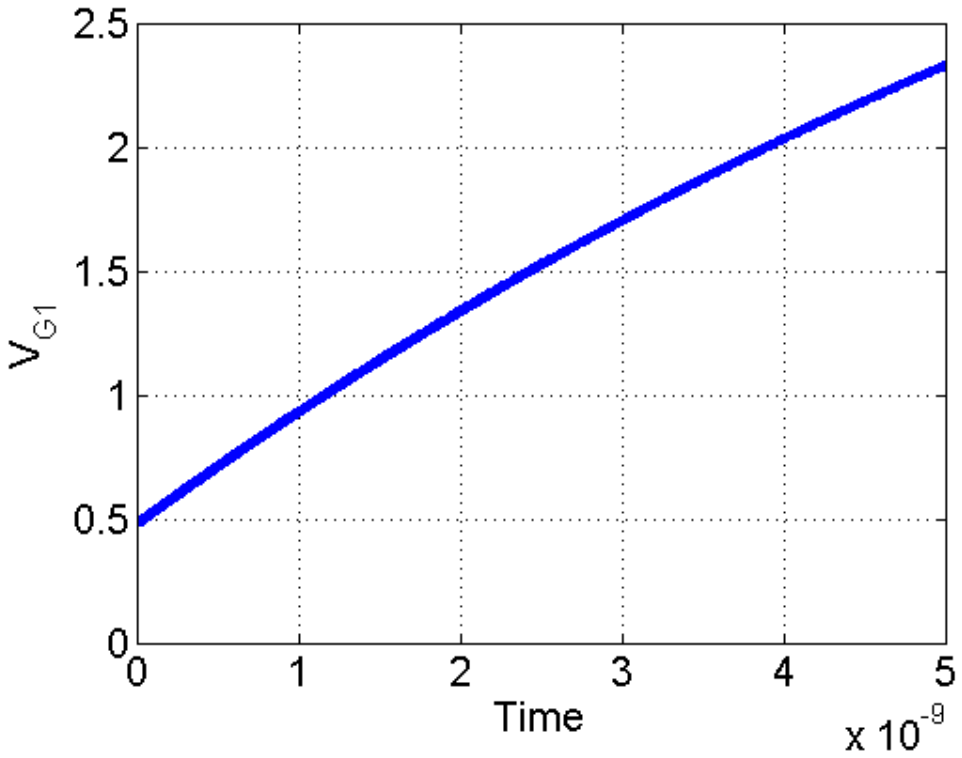
- $t_{rise} = 1.2ns$

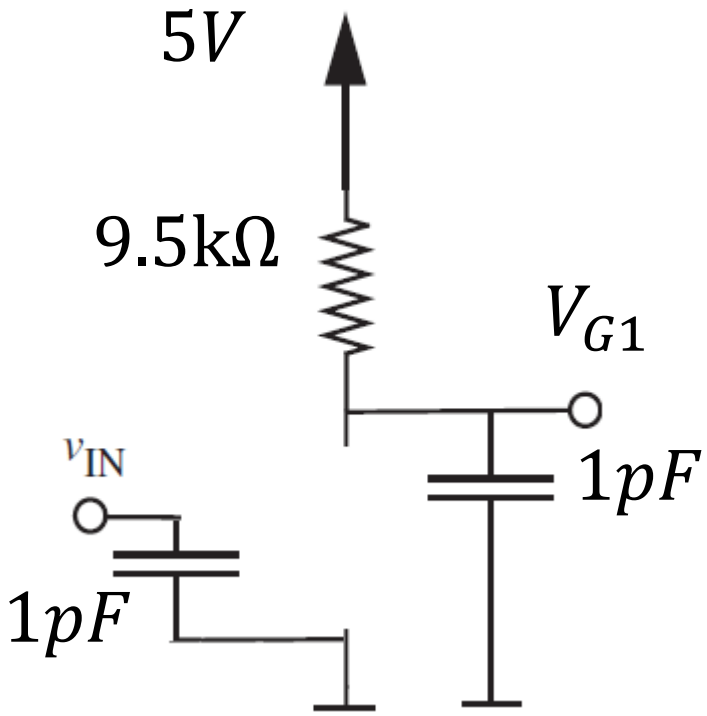



$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

# Timing Analysis of the SRC model

- $V_{G1} = (0.476 - 5)e^{-t/\tau} + 5$
- $\tau \approx 10^{-12}s$
- $t_{rise} = 1.2ns$



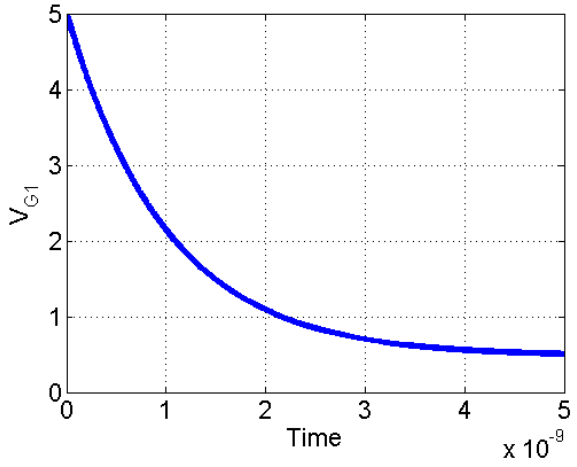



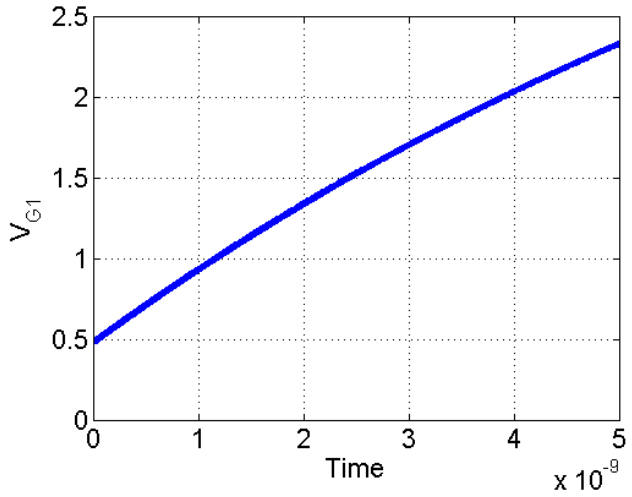

$R_{on} = 1k\Omega$

$V_T = 1V$

# Propagation Delay

- Rise and Fall Time are also called "Propagation Delays"

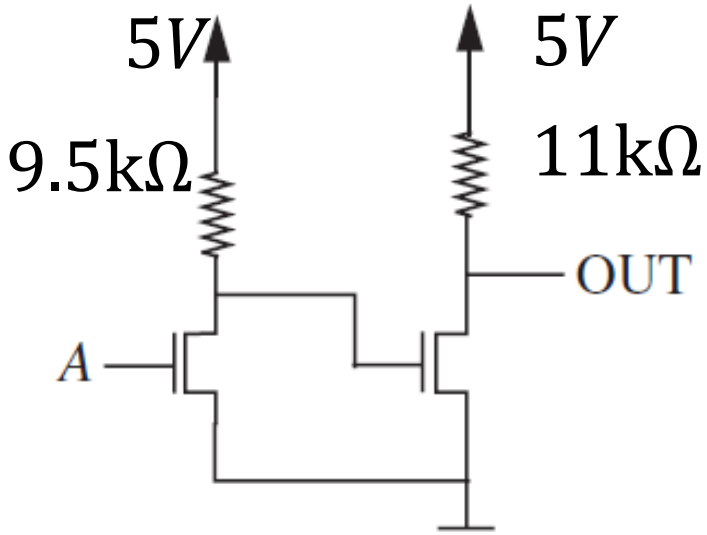


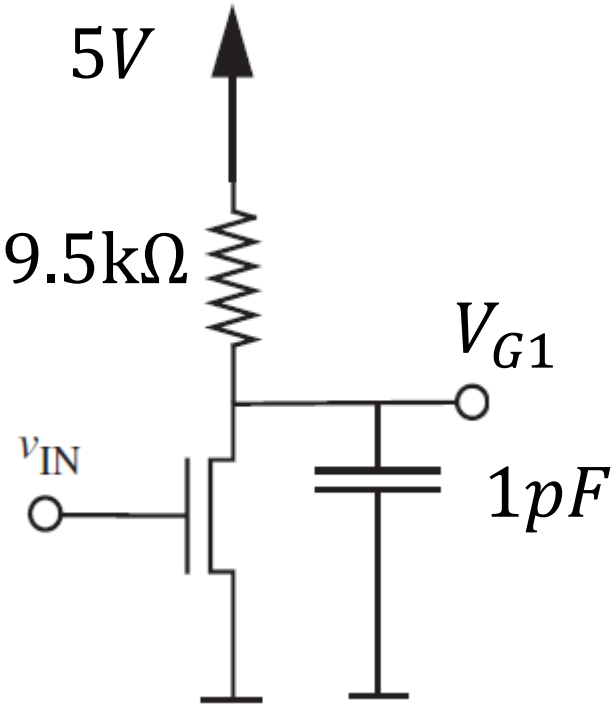

- Gives "delay time" between when the logical input changes and the logical output changes
- Book calls them $t_{pd,1\rightarrow0}$ and $t_{pd,0\rightarrow1}$

# Reminder of Where We Started

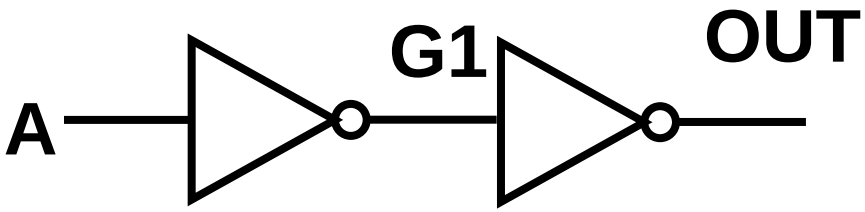
Wanted to study gate delay of:




So used SRC model:



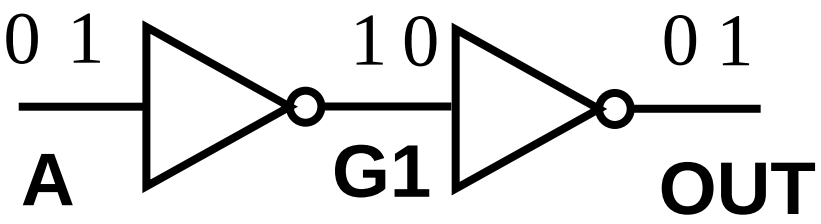

Which implements:




Giving delay of LEFT gate!

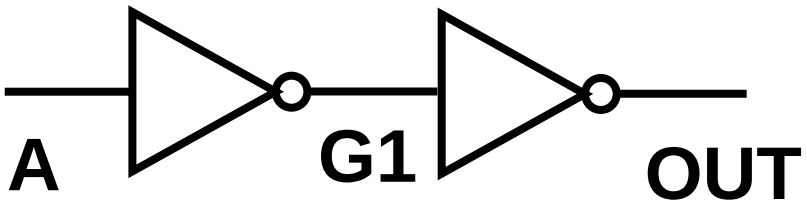
# Using Propagation Delays

- $t_{rise} = t_{pd,0\rightarrow1} = 1.2ns$
- $t_{fall} = t_{pd,1\rightarrow0} = 2.2ns$
- Suppose A has been zero a long time and switches to 1
  - How long does it take for $G_1$ to go to 0?
  - How long does it take for $OUT$ to go to 1?



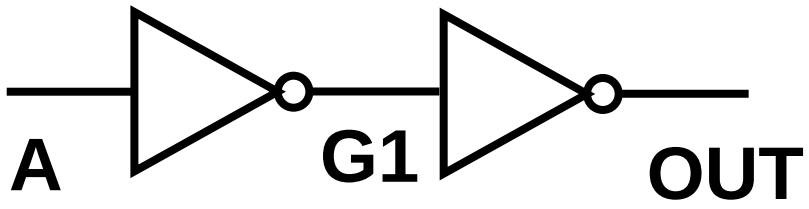
# Propagation Delays

- In general $t_{pd,0\rightarrow1}$ is not equal to $t_{pd,1\rightarrow0}$
- Thus, we usually just take the maximum and call that the propagation delay of the gate
- $t_{pd} = 2.2ns$
- Means that no matter what input you give the gate, output will be correct within $2.2ns$



# Bonus Question for CS61C Veterans

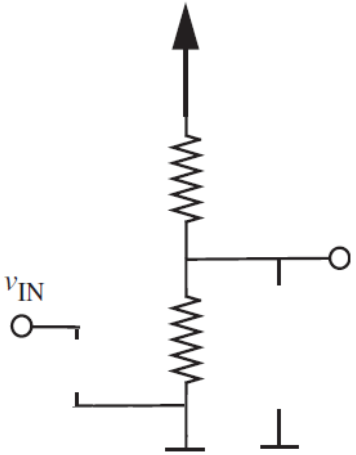
- Assume now that the rise and fall times of both gates are $2.2ns$
- Assume that we have a register driving “A” and a register receiving “OUT”
- Assume the registers operate instantaneously
- What is the minimum clock time if this very boring buffer is our longest pipeline stage?

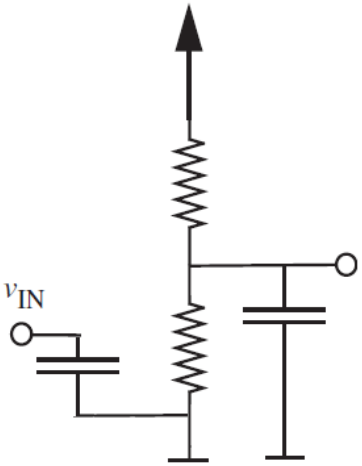


- This is where we stopped

# Power in the SRC Model

- **Static power** in the SRC Model is exactly as SR Model, compare:

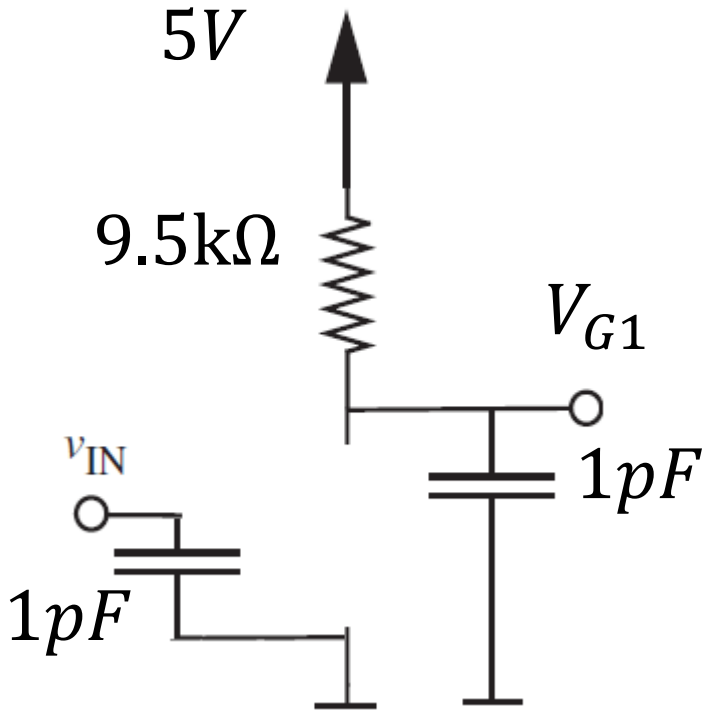


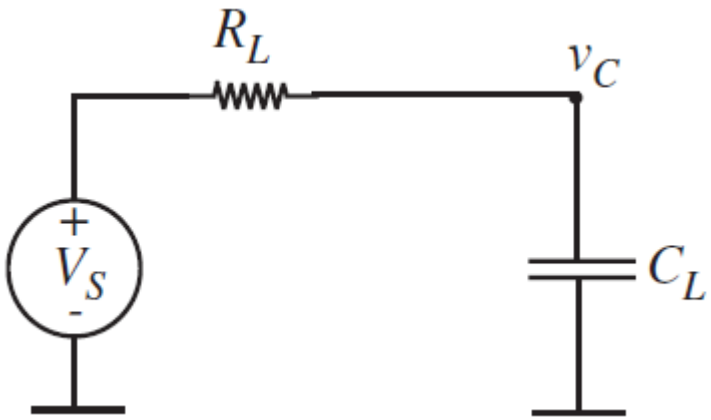




- We're also interested in the **dynamic power** while capacitance is charging
- Algebra is a bit involved. We'll outline the concept. Book has a very thorough treatment in sections 11.1 through 11.3

# Dynamic Power in NMOS Circuits

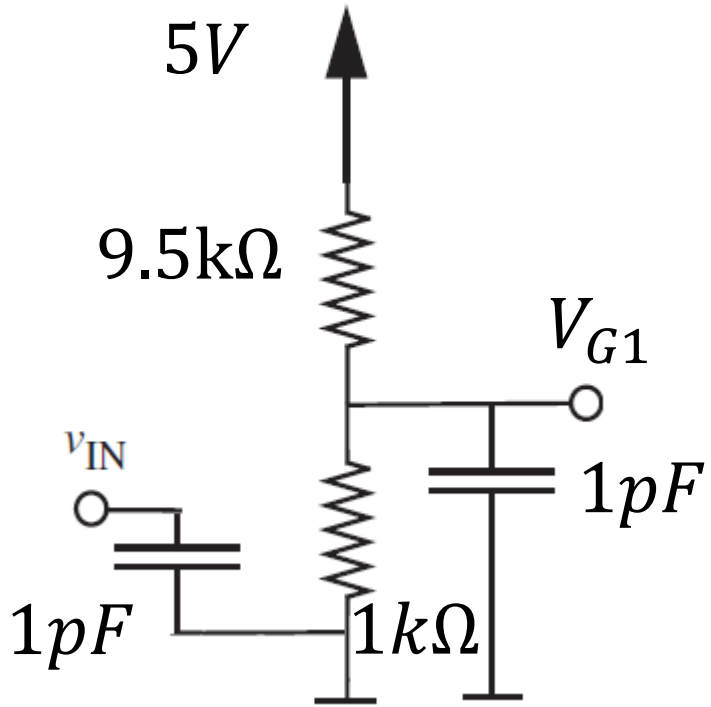
- When our inverter is going from **low to high**, we have the circuit on the left:
- In general, looks like circuit on the right:

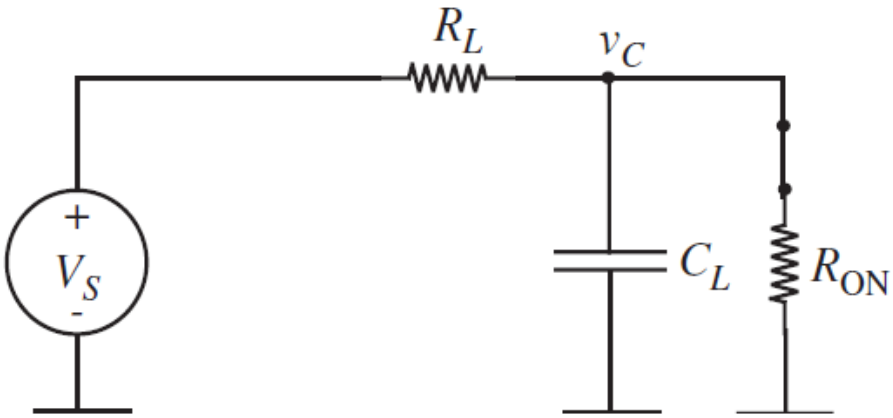


# Dynamic Power in NMOS Circuits

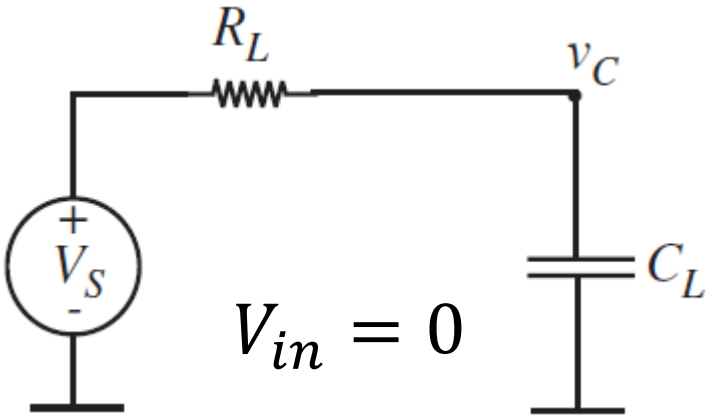
- When our inverter is going from **high to low**, we have the circuit on the left:
- In general, looks like circuit on the right:



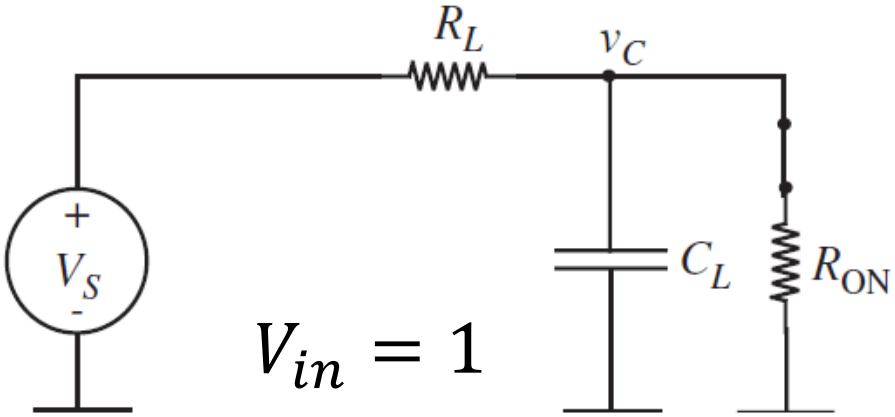



# Dynamic Power

- Worst case is that inverter is driven by a sequence of 1s and 0s
  - Circuit constantly switching behavior
  - Gate capacitor constantly charging and discharging



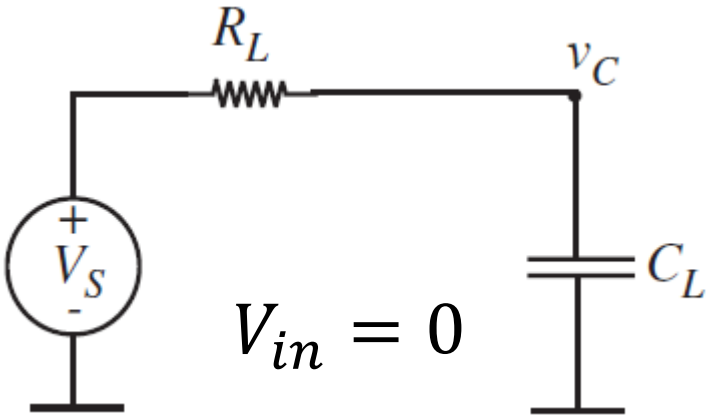

Charges up towards $V_S$



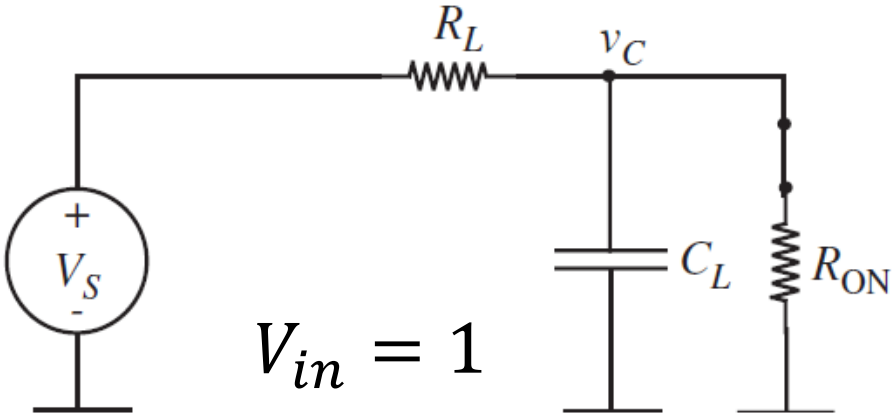

Discharges down towards $V_S \frac{R_{ON}}{R_{ON}+R_L}$

# Problem Setup

- $V_{in}$ is
  - 0 for some time $T_1$
    - Dissipates some energy $w_1$
  - 1 for some time $T_2$
    - Dissipates some energy $w_2$
- $P = \frac{w_1 + w_2}{T_1 + T_2}$
- See 11.1 through 11.3 for derivation




Charges up towards $V_S$



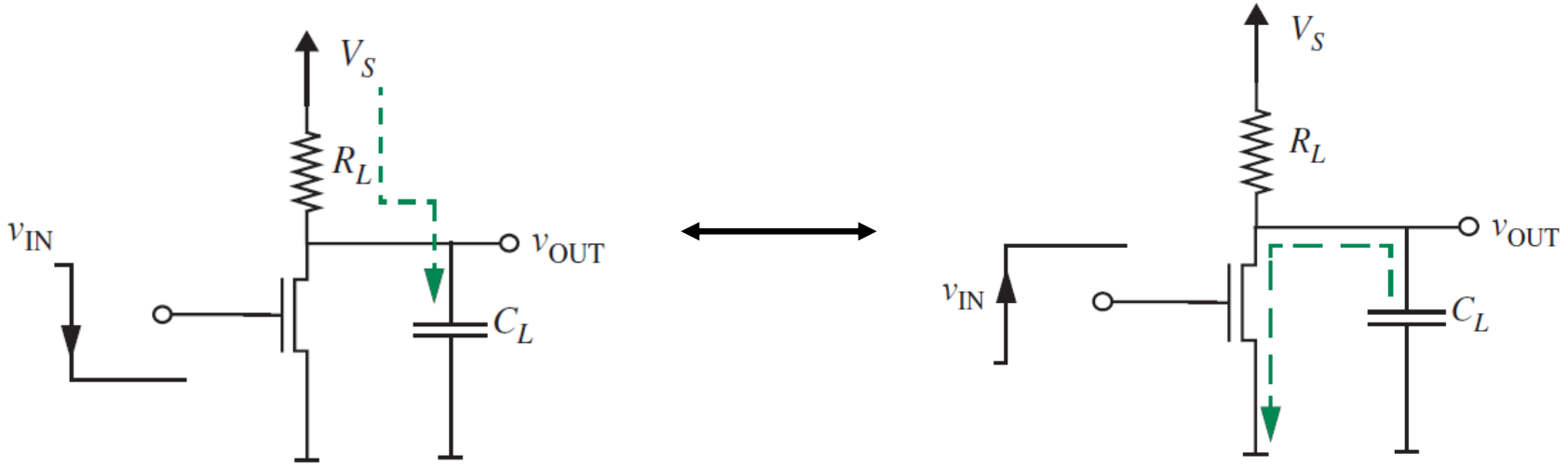

Discharges down towards $V_S \frac{R_{ON}}{R_{ON} + R_L}$

# Solution

$$\bar{p} = \frac{V_S^2}{2(R_L + R_{ON})} + \frac{V_S^2 R_L^2 C_L}{(R_L + R_{ON})^2 T}$$

$$p_{static} = \frac{V_S^2}{2(R_L + R_{ON})}$$

$$p_{dynamic} = \frac{V_S^2 R_L^2 C_L}{(R_L + R_{ON})^2 T}$$

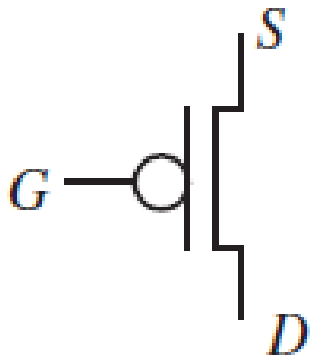


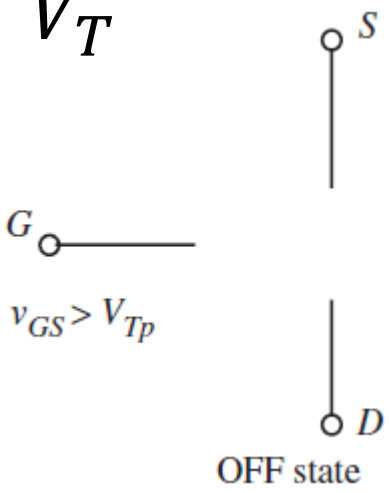
# Avoiding Static Power Loss

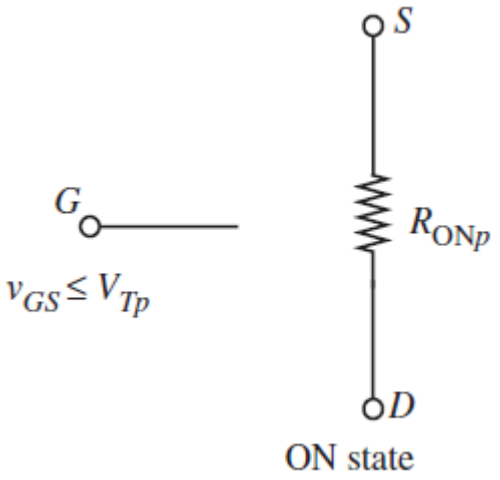
- Next we will talk about CMOS, which stands for Complementary MOS
- So far, all of our transistors have been NMOS transistors, where they are on if $V_{GS} \geq V_T$
- Next, we will discuss a new type of FET transistor called a PMOS
- Only difference is that they will be on when $V_{GS} \leq V_T$

# PMOS Transistor

- Drawn with a bubble at the input:
- Usually drawn with source on top and drain on bottom (for reasons that will become clear)
- Just as before, have ON and OFF states, now on when $V_{GS} \leq V_T$

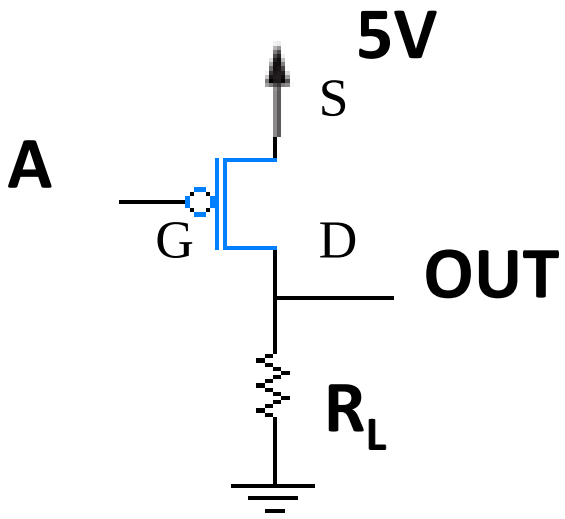


# Anything logical we can do with NMOS…

- …we can do with PMOS
- Example, we can build an inverter, try it for 60 seconds or so on the worksheet using a PMOS, 5V source, ground, and resistor
- Assume input signal is 0V or 5V and $V_T = -1V$




Here: $R_L$ acts as a pulldown resistor

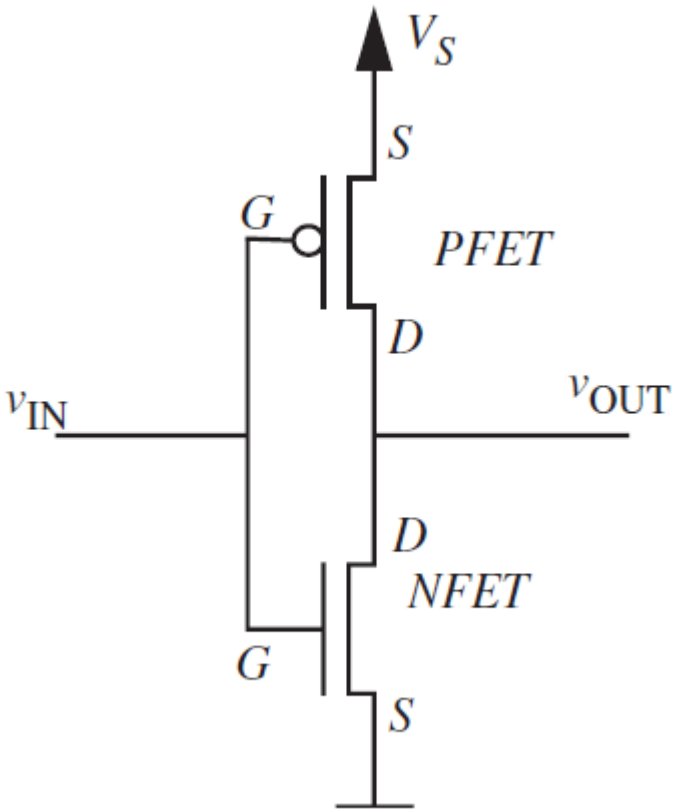
Q13

# Analysis of PMOS Logic

- We could go through and repeat everything we did for NMOS, but it would be almost exactly the same thing
- Instead, we're now going to use NMOS and PMOS in a clever way

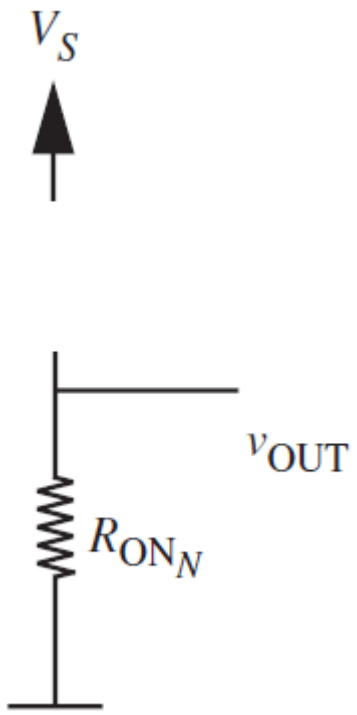
# CMOS Inverter

- Two complementary implementations of the same logic function
- When $V_{IN}$ is high:
  - Path to ground is closed
  - Path to $V_S$ is open



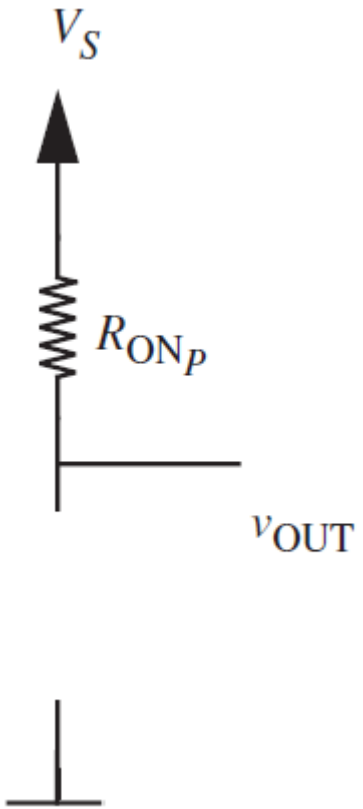
# CMOS Inverter

- When $V_{IN}$ is high:
  - Path to ground is closed
  - Path to $V_S$ is open
- Huge resistance on open PMOS acts as a pull-up resistor



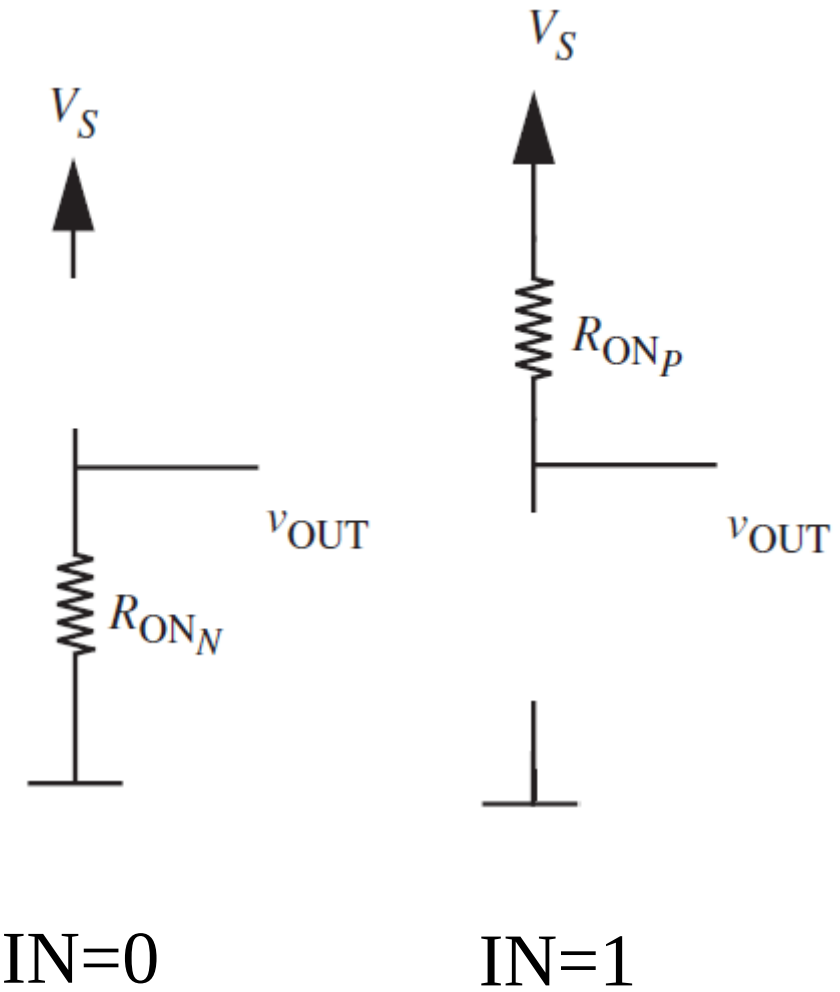
# CMOS Inverter

- When $V_{IN}$ is low:
  - Path to ground is open
  - Path to $V_S$ is closed
- Huge resistance on open NMOS acts as a pull-down resistor



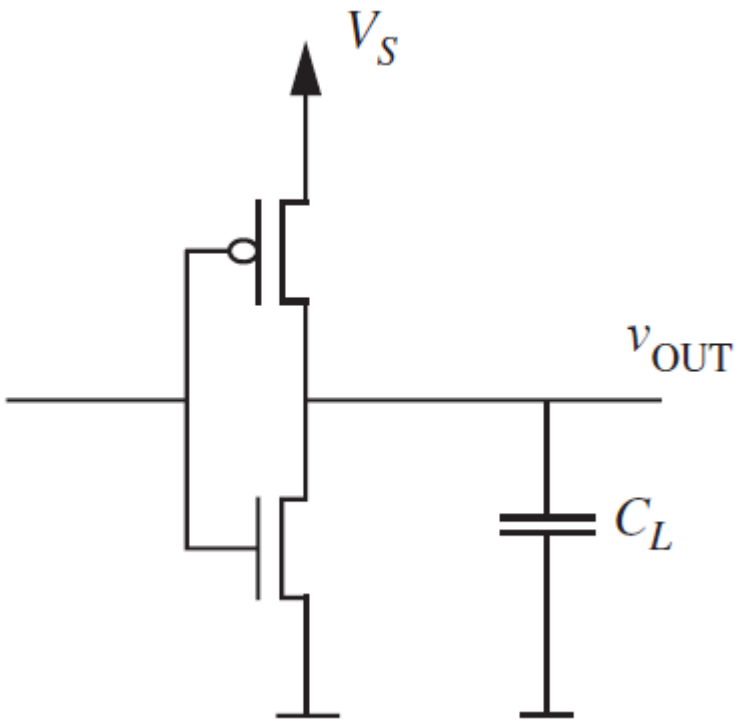
# Static Power in CMOS

- What is the static power consumed by this CMOS inverter when IN=0?
- When IN=1?
- In reality, as gate insulator gets thinner, there is a significant leakage component



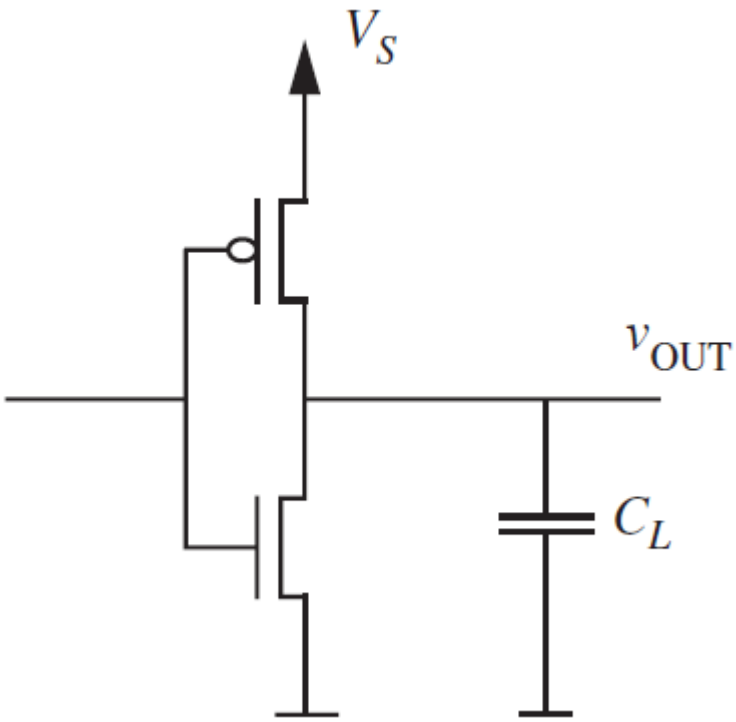
# Dynamic Power in CMOS

- **Load power:** Since our CMOS gates will be driving capacitive loads, they will still draw power when switching (since power is provided to the load)



# Dynamic Power in CMOS

- **Leakage Power:** Unless you're careful about timing, both MOSFETs could be closed at the same time
  - Power flows directly from $V_S$ to ground




- Even if timing is perfect, both transistors will at some point be "weakly on" – **subthreshold leakage**

# Dynamic Power

- These days, subthreshold leakage is a big issue
  - Thresholds have been reduced to decrease switching times
  - Reduced thresholds mean leakier MOSFETs
- In this class, we won't analyze this case, but be aware that in the world of digital integrated circuits, it plays a big role

# CMOS

- CMOS Summary:
  - No need for a pull-up or pull-down resistor
    - Though you can avoid this even with purely NMOS logic (see HW7)
  - Greatly reduced static power dissipation vs. our simple NMOS only logic
    - In reality, thin gate oxides lead to some static non-zero $i_G$, so static power is not zero
  - Dynamic power is still hugely significant
  - Uses twice the number of transistors as our simple purely NMOS logic

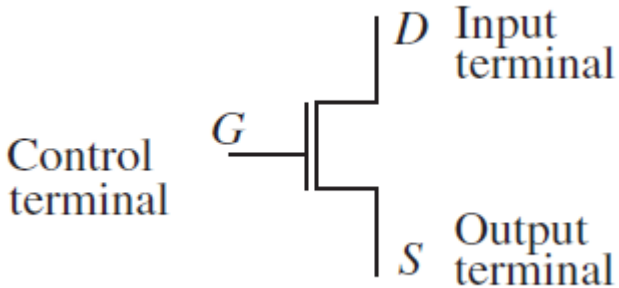
## Implementation of Complex Gates Using NMOS and CMOS

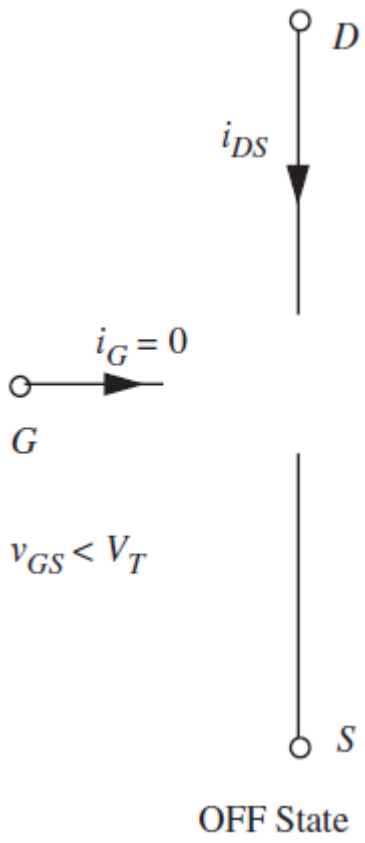
- In class today, we've discussed analysis of NMOS and CMOS circuits
- Haven't discussed how to design them
- Luckily, it is easy

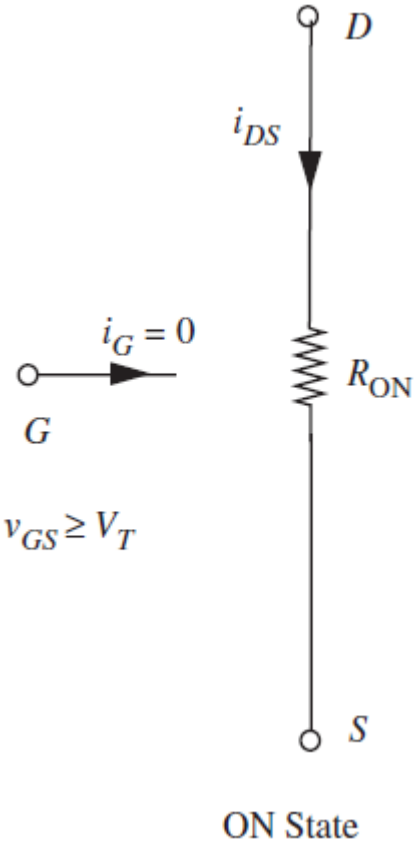
# That's it for today

# Extra Slides

# SR Model of the PMOS MOSFET




$$i_{DS} = \frac{V_{DS}}{R_{ONp}}, V_{GS} \leq V_T$$
$$= 0, \quad V_{GS} > V_T$$

No, has nothing to do with SR flip-flop