EE40
Lecture 16
Josh Hug

8/02\/2010

Logistics

- HW7 due tomorrow
- HW8 will be due Friday
- Mini-midterm 3 next Wednesday
  - 80/160 points will be a take-home set of design problems which will utilize techniques we've covered in class
    - Handed out Friday
    - Due next Wednesday
  - Other 80/160 will be an in class midterm covering HW7 and HW8
- Final will include Friday and Monday lecture
  - Design problems will provide practice

Project 2

- Active filter lab and Booster lab due this week
  - For Booster lab, ignore circuit simulation, though it may be instructive to try the Falstad simulator
- Project 2 due next Wednesday

Design Problems

- **ALL WORK MUST BE DONE COMPLETELY SOLO!**
- Maximum allowed time will be **5 hours**
  - Will be written so that it can be completed in approximately 2 hours
- Allowed resources:
  - May use any textbook (incl. Google Books)
  - Anything posted on the EE40 website
  - Only allowed websites are Google Books, wikipedia, and EE40 websites
  - Not allowed to use other websites like facebook answers, yahoo answers, etc. even if you are reading other people's responses
  - When in doubt, email me or text me
  - We will be very serious about cheating on this!

Example Design Problem

- Design a circuit which will sum three sinusoidal input voltages and attenuate any frequencies above 10,000 Hz by at least 20 dB

Project 2

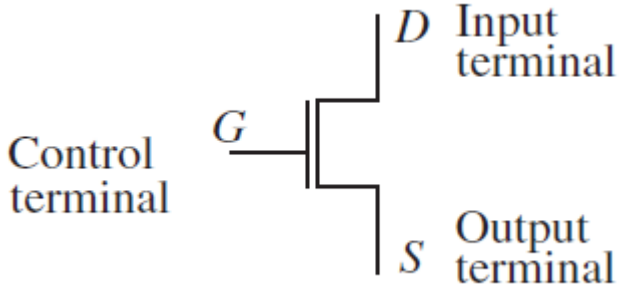
- For those of you who want to demo Project 2, we'll be doing demos in lab on Wednesday
  - Either at 1 PM after mini-midterm
  - Or at 2 PM during usual lab period
  - Opinions?

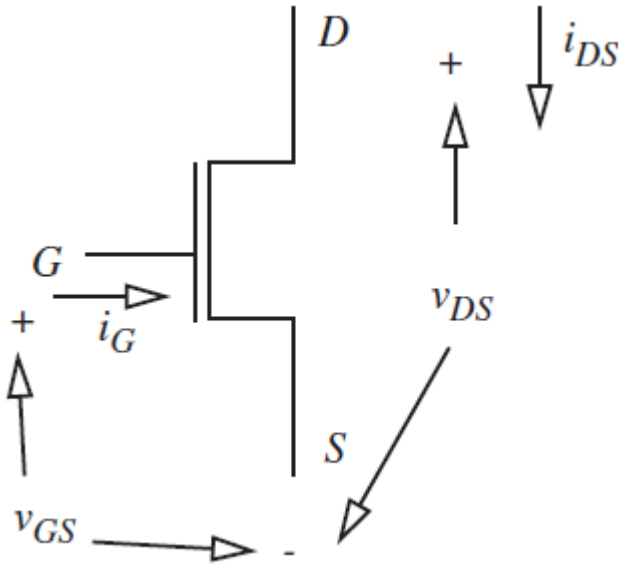
Interactive Lecture Question

- Did you like the interactive worksheet intensive MOSFET lecture?
  A. Yes, it was extremely useful and I highly prefer this type of lecture
  B. Yes, it was useful, but the usual 1-way lecture is fine
  C. No real opinion
  D. Didn't like it
  E. Hated it

MOSFET Model

- Schematically, we represent the MOSFET as a three terminal device
- Can represent all the voltages and currents between terminals as shown to the right



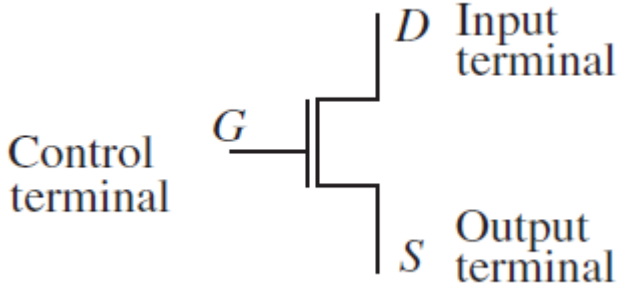


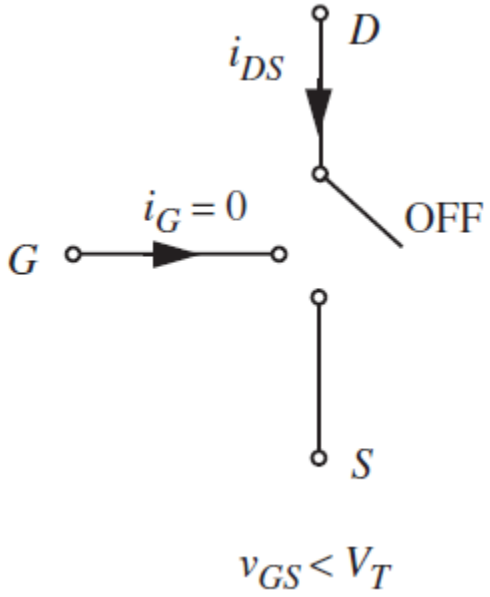
MOSFET modeling

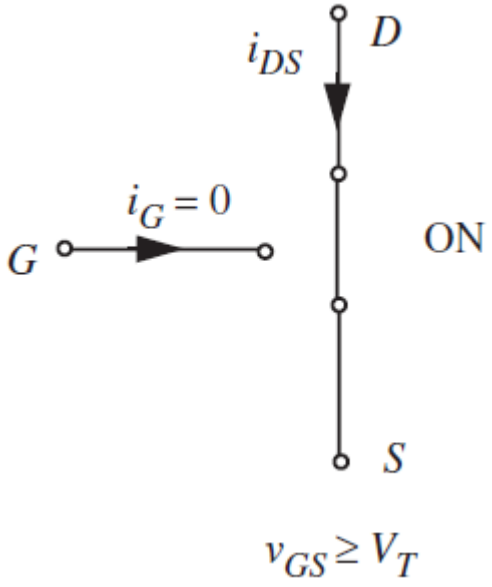
- MOSFET models vary greatly in complexity
- **S Model:** Good for explaining MOSFETs to someone with no EE knowledge
- **SR Model:** Includes effective resistance of a MOSFET. Good for understanding how to choose pull-up resistance
- **SR Model:** Include gate capacitance. Good for understanding dynamic power and gate delay

S Model of the MOSFET

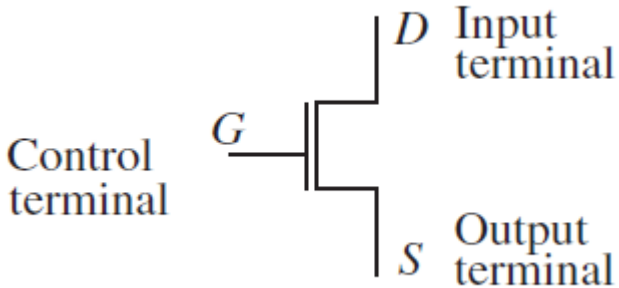
- The simplest model basically says that the MOSFET is:
  - Open for $V_{GS} < V_T$
  - Closed for $V_{GS} > V_T$

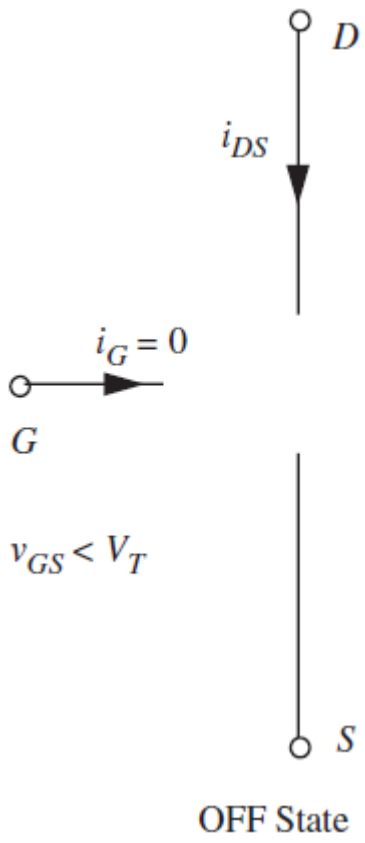


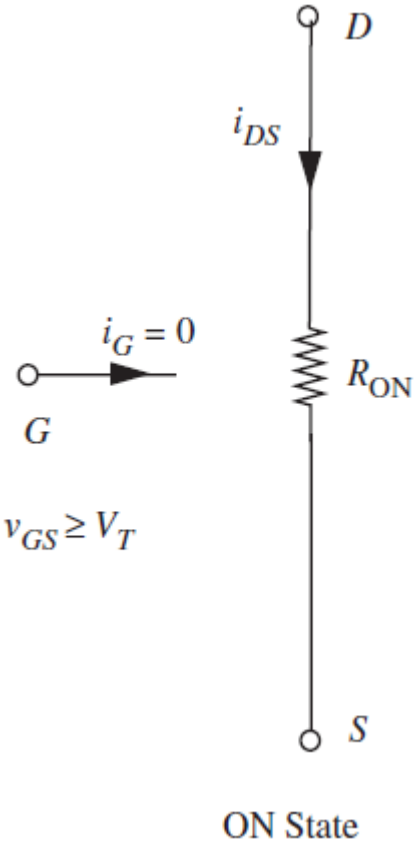




SR Model of the MOSFET





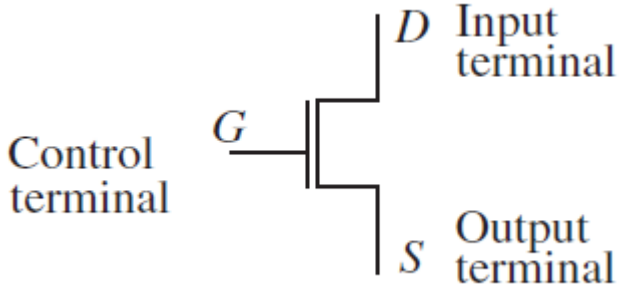


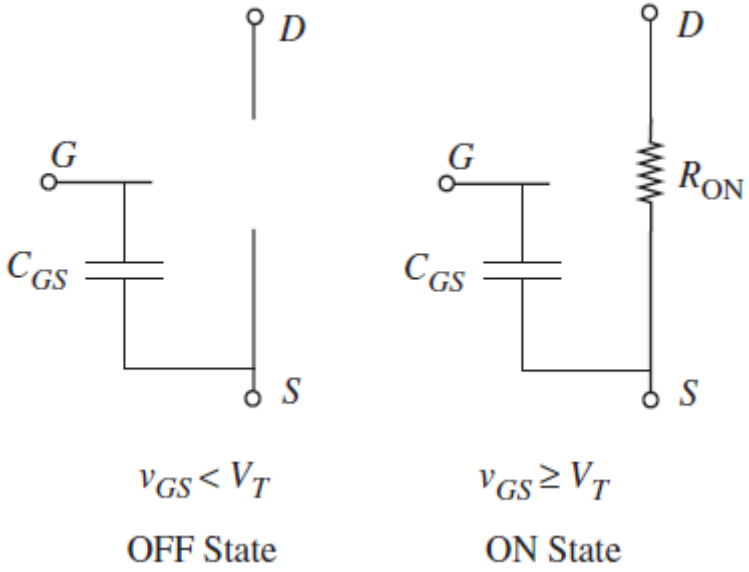
$$i_{DS} = \frac{V_{DS}}{R_{ON}}, V_{GS} \geq V_T$$
$$= 0, \quad V_{GS} < V_T$$

[Has nothing to do with SR flip-flop]

The SRC Model

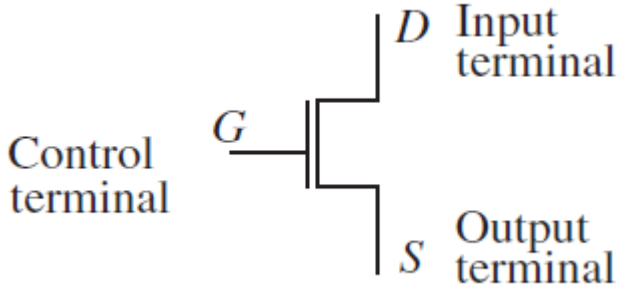
- The SRC Model is almost identical to the SR model, except that each gate node has a capacitance
- Like SR model: open when OFF and resistive when ON
- Note that now i_G is non-zero!

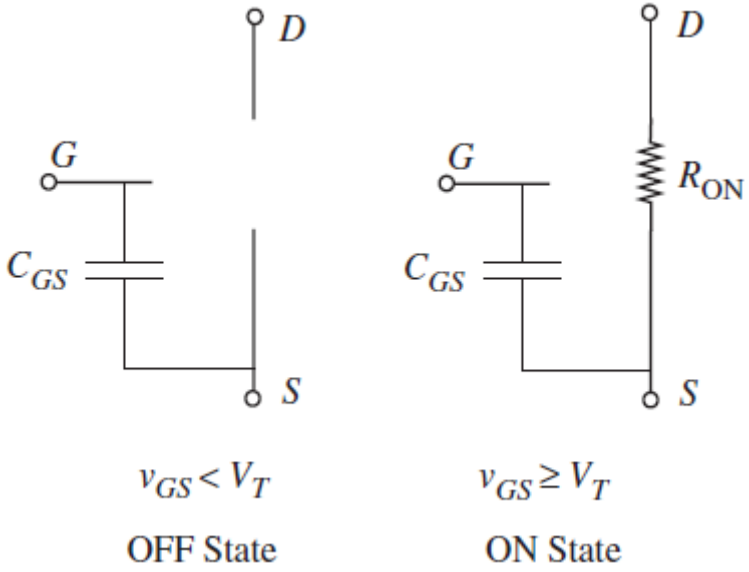




The SRC Model

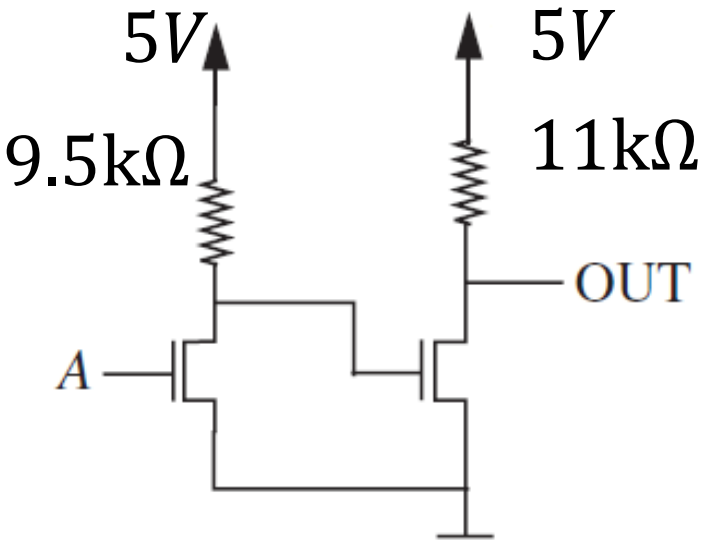
- Useful for modeling:
  - Gate delay: Takes time to charge up
  - Dynamic power: $i_G \neq 0$



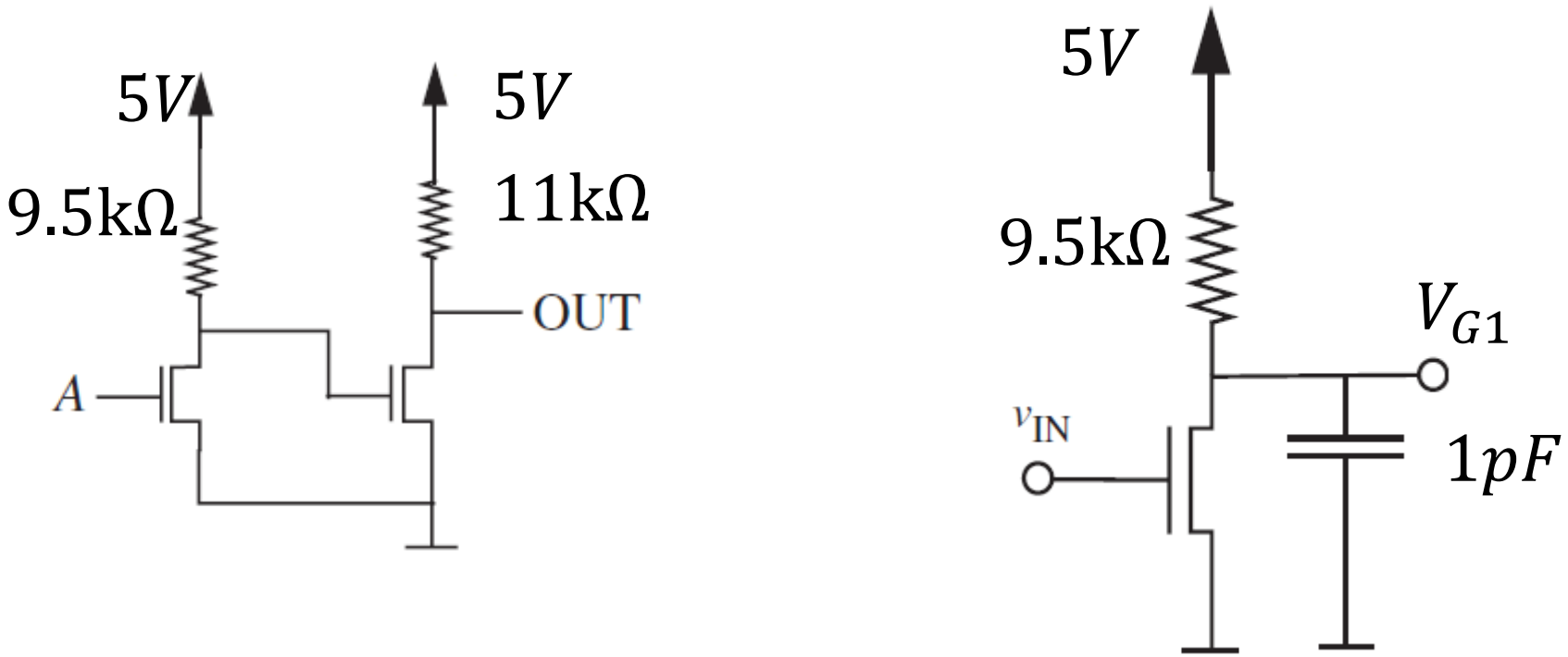


SRC Model

- Consider our familiar pair of inverters
- We're going to focus on the behavior of our left inverter
- Let's assume that both MOSFETs have a gate capacitance of $1pF$ or $10^{-12}F$



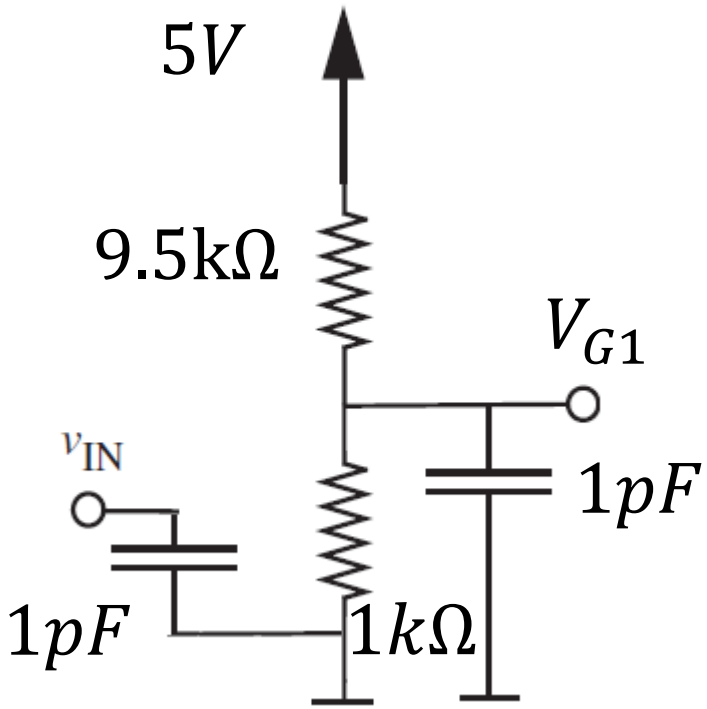
SRC Model of our 2 Inverters



- We decide to ignore the function of the gate on the right, keeping it in mind only because we know we'll have to charge it

Timing Analysis of the SRC model

- Since $V_{G1}(0) = 5V$, $V_{G1}(\infty) = 0.476V$, and $\tau \approx 1ns$, then:
- $V_{G1}(t) = (5 - 0.476)e^{-t/\tau} + 0.476$
- How long will it take for the next inverter in the chain to turn on?

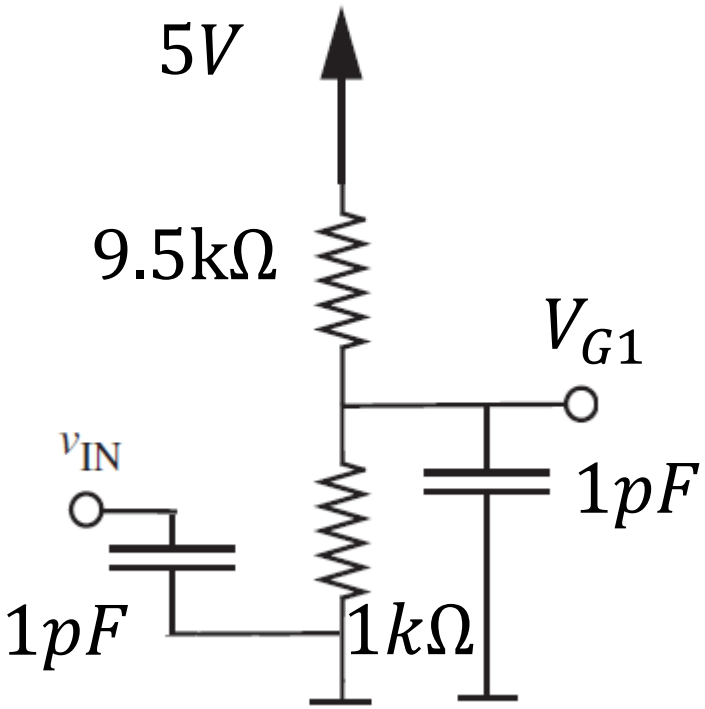


$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

$$\tau = 10^{-12} \times (9500 \parallel 1000) = 1.06 \times 10^{-9}$$

Timing Analysis of the SRC model

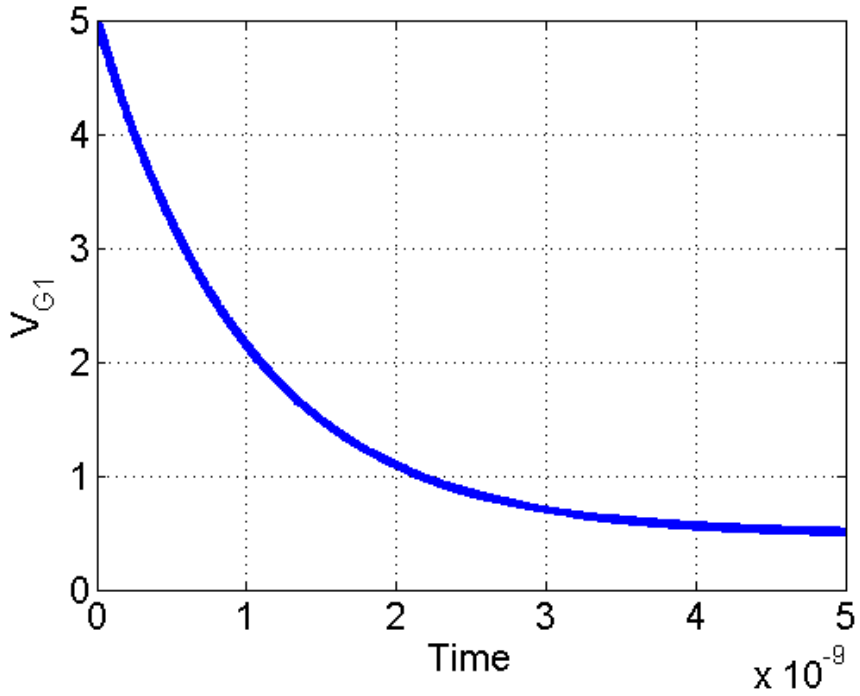
- $(5 - 0.476)e^{-t_{fall}/\tau} + 0.476 = 1$
- $-\tau \ln(0.1158) = t_{fall}$
- So $t_{fall} = 2.2ns$
- We call this the "**Fall Time**": gives time for V_{G1} to fall from 5V to 1V

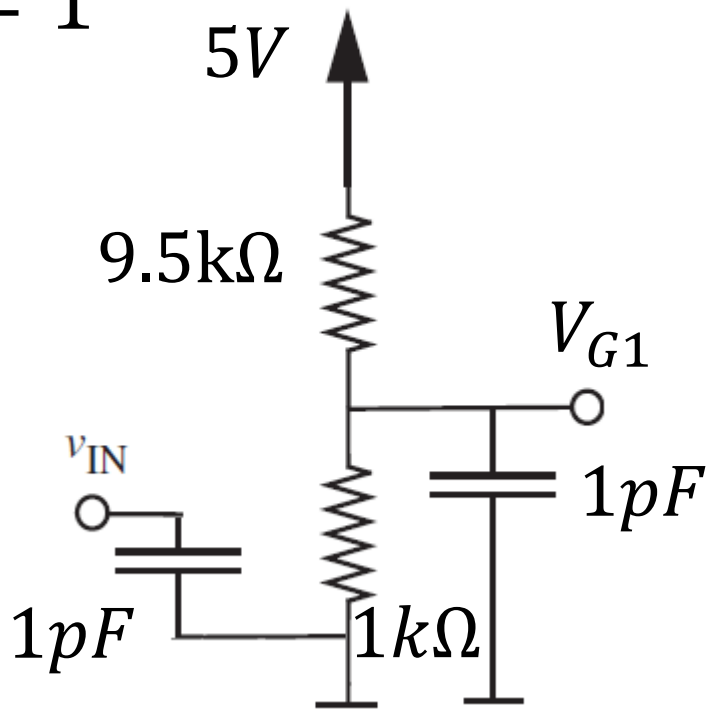


$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

Fall Time

- $(5 - 0.476)e^{-t/\tau} + 0.476 = 1$
- $\tau \approx 10^{-9}$
- Gives: $t_{fall} = 2.2ns$



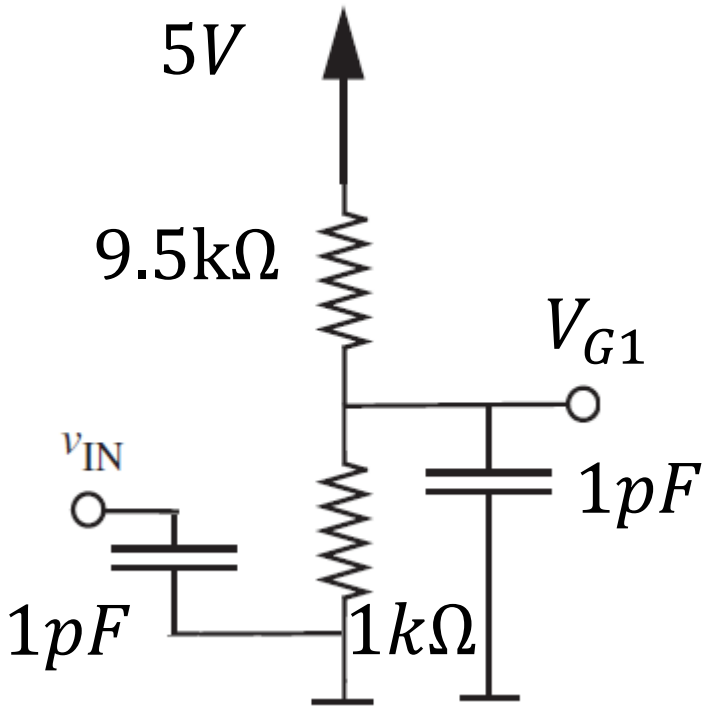


$R_{on} = 1k\Omega$

$V_T = 1V$

Timing Analysis of the SRC model

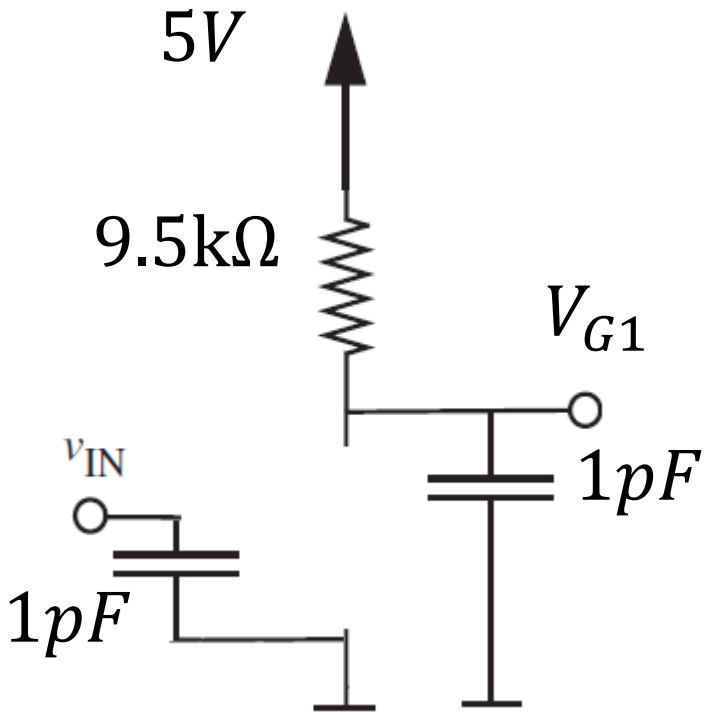
- How do we find the **Rise Time**?
- Have to replace by new equivalent circuit where:
  - Capacitor is initially discharged (0.476 V)
  - Switch is open



$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

Timing Analysis of the SRC model

- How do we find the **Rise Time**?
- Have to replace by new equivalent circuit where:
  - Capacitor is initially discharged (0.476 V)
  - Switch is open
- $V_{G1} = (0.476 - 5)e^{-t/\tau} + 5$
- $\tau = 10^{-12} \times 9500 \approx 10ns$



$R_{on} = 1k\Omega$

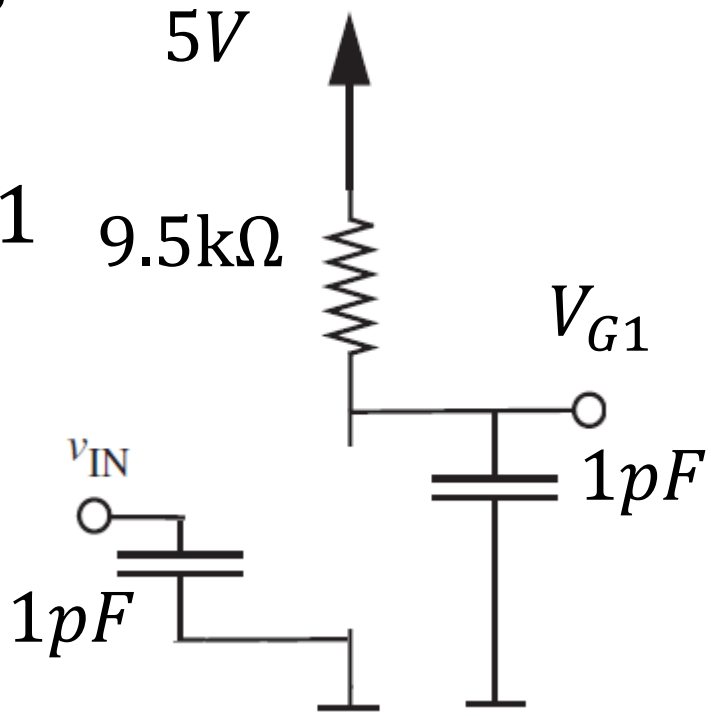
$V_T = 1V$

Timing Analysis of the SRC model

- $V_{G1} = (0.476 - 5)e^{-t/\tau} + 5$
  $\tau = 10^{-12} \times 9500 \approx 10ns$
- $(0.476 - 5)e^{-t_{rise}/\tau} + 5 = 1$

$$-\tau \ln(0.884) = t_{rise}$$

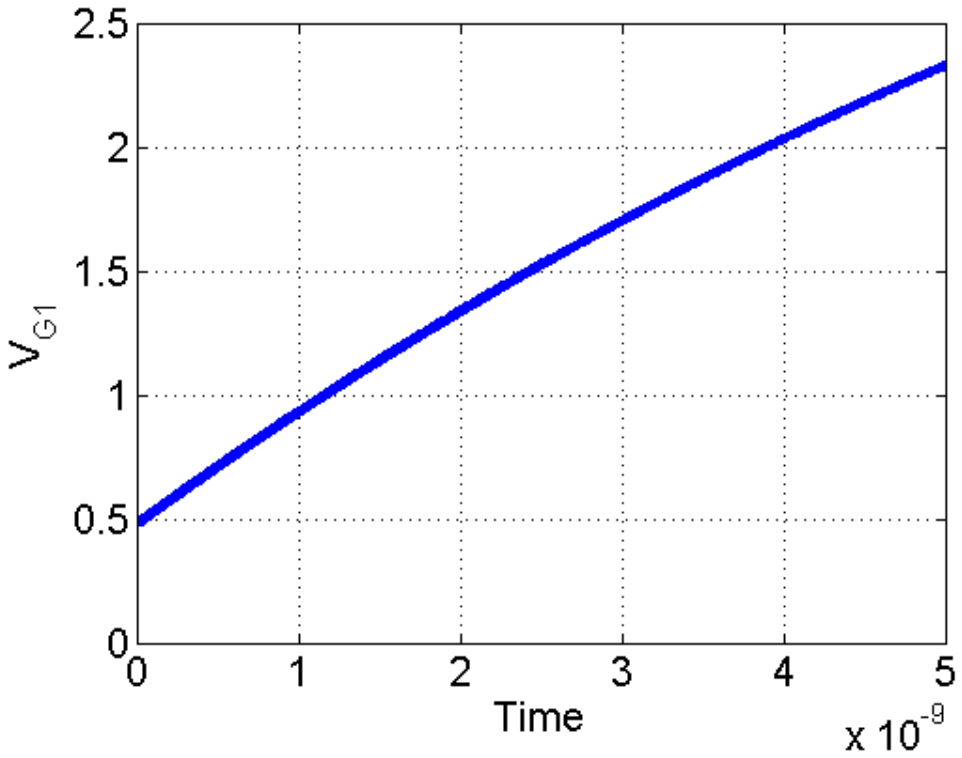
- $t_{rise} = 1.2ns$

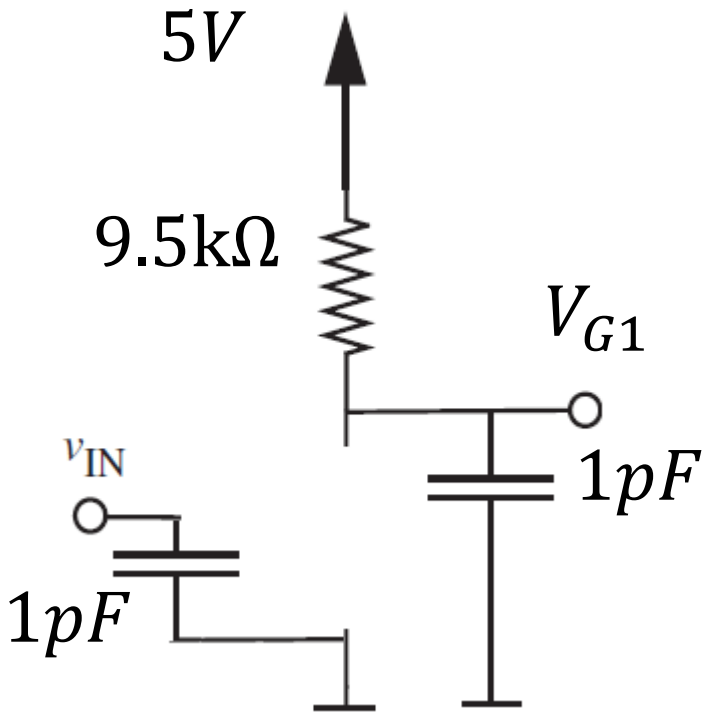


$$R_{on} = 1k\Omega$$
$$V_T = 1V$$

Timing Analysis of the SRC model

- $V_{G1} = (0.476 - 5)e^{-t/\tau} + 5$
- $\tau \approx 10^{-12}s$
- $t_{rise} = 1.2ns$



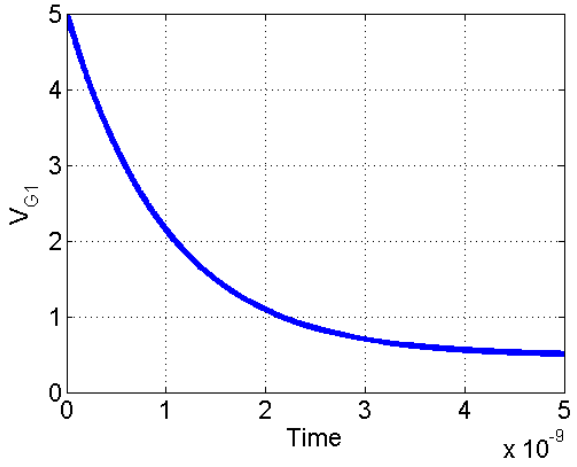


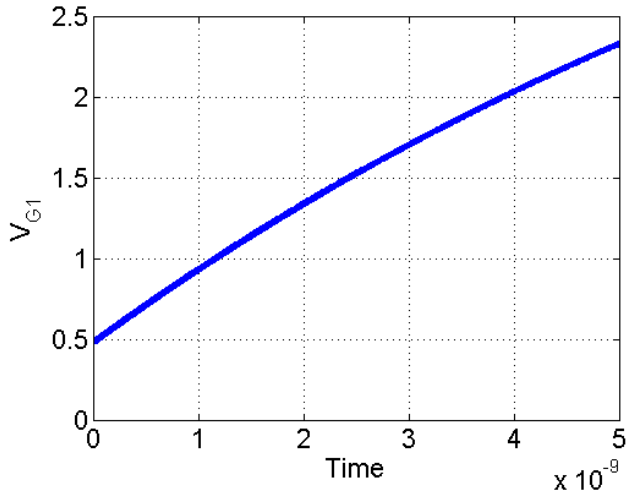
$R_{on} = 1k\Omega$

$V_T = 1V$

Propagation Delay

- Rise and Fall Time are also called "Propagation Delays"

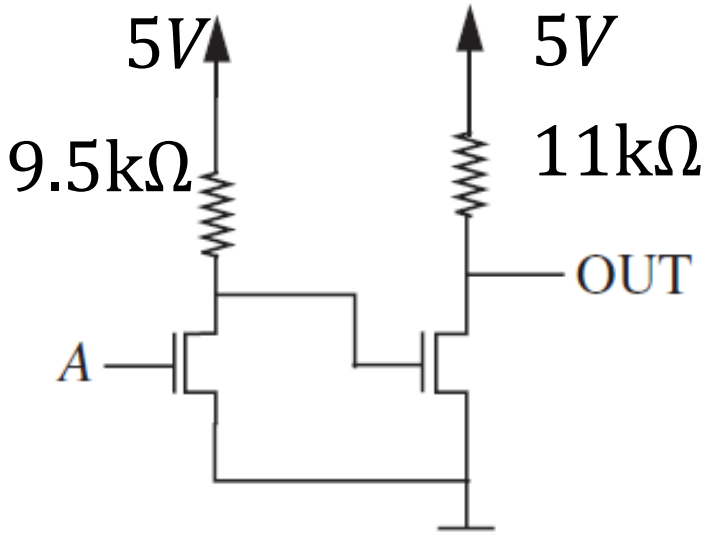




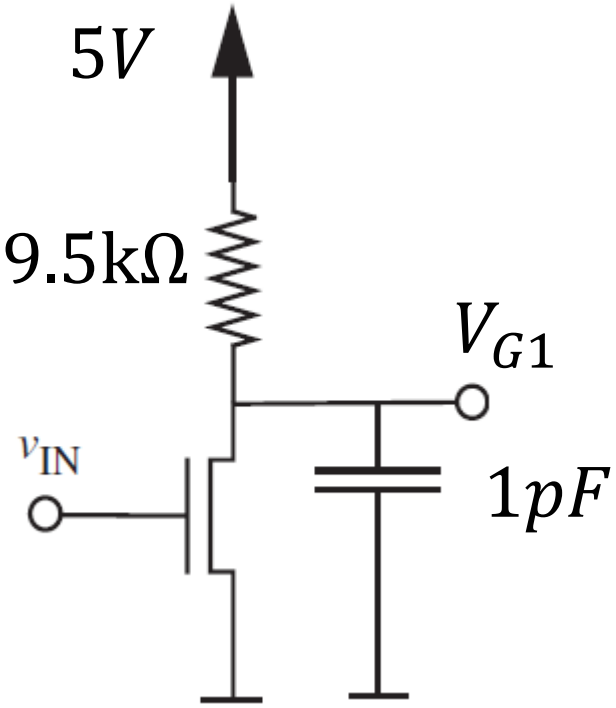
- Gives "delay time" between when the logical input changes and the logical output changes
- Book calls them $t_{pd,1\rightarrow0}$ and $t_{pd,0\rightarrow1}$

Reminder of Where We Started

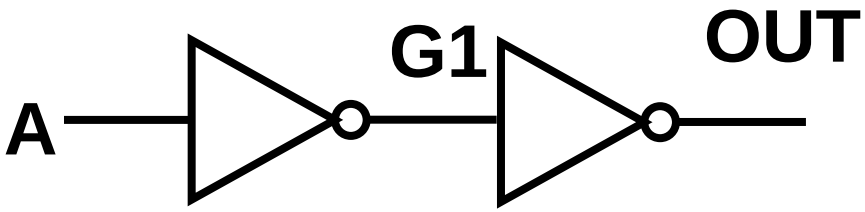
Wanted to study gate delay of:



So used SRC model:



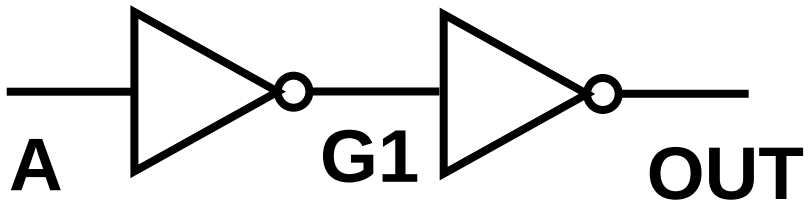
Which implements:



Giving delay of LEFT gate!

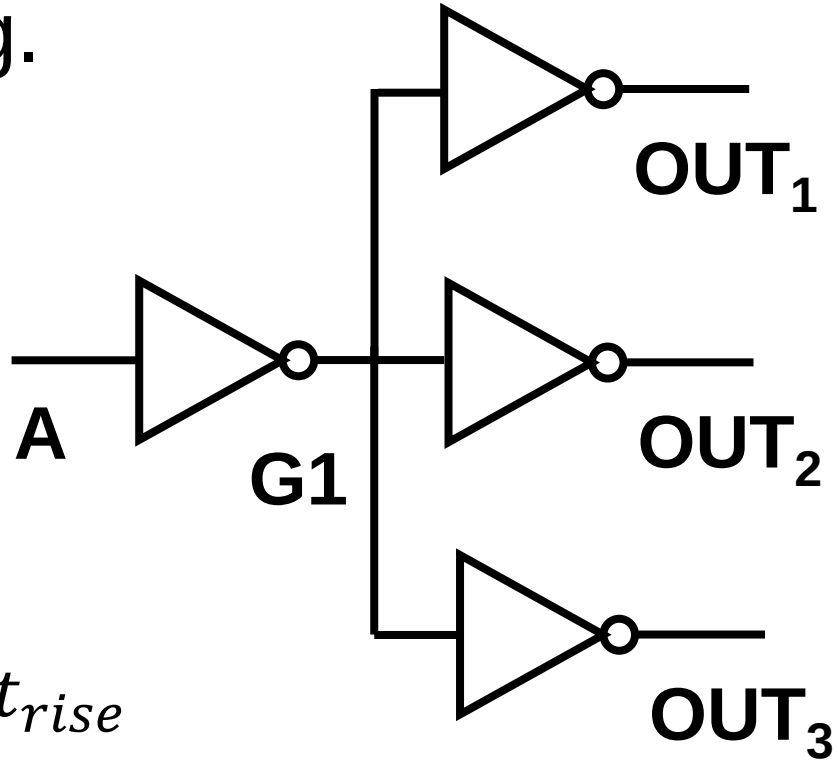
Propagation Delays

- In general $t_{pd,0\rightarrow1}$ is not equal to $t_{pd,1\rightarrow0}$
- Thus, we usually just take the **maximum** and call that the **propagation delay of the gate**
- $t_{pd} = 2.2ns$
- Means that no matter what input you give the gate, output will be correct within $2.2ns$



Propagation Delay

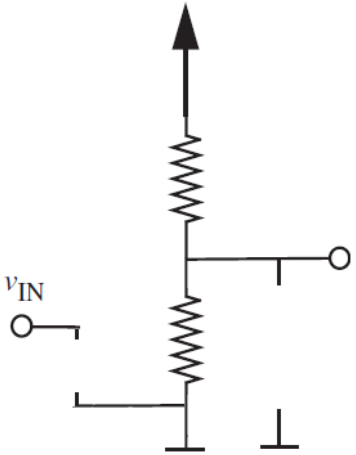
- Is our analysis still correct if we add more output gates?
- No, gate capacitance increases! Takes 3 times as long.

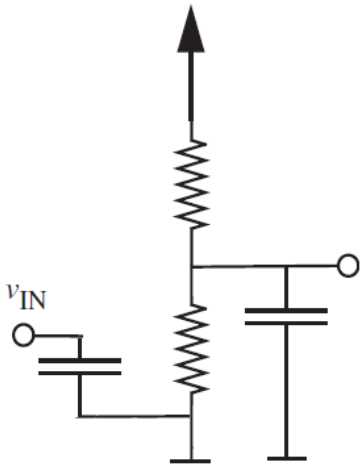


$$-\tau \ln(0.884) = t_{rise}$$

Power in the SRC Model

- **Static power** in the SRC Model is exactly as SR Model, compare:

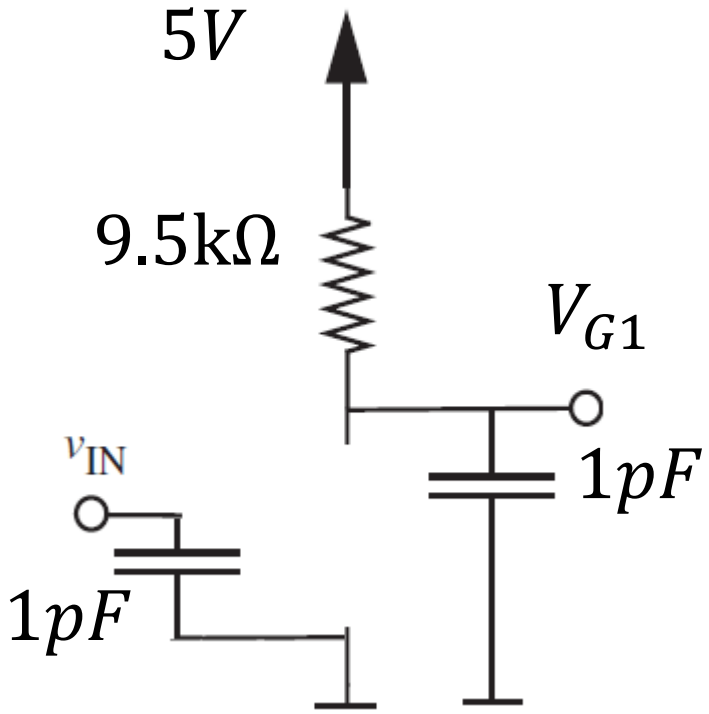


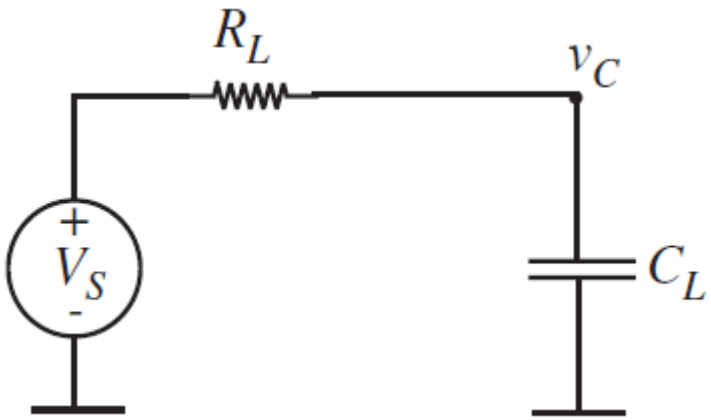


- We're also interested in the **dynamic power** while capacitance is charging
- Algebra is a bit involved. We'll outline the concept. Book has a very thorough treatment in sections 11.1 through 11.3

Dynamic Power in NMOS Circuits

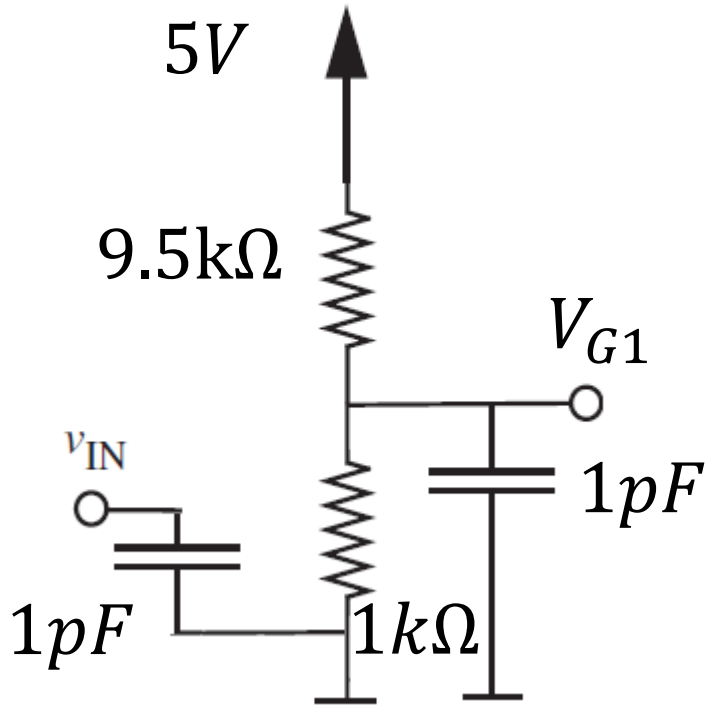
- When our inverter is going from **low to high**, we have the circuit on the left:
- In general, looks like circuit on the right:

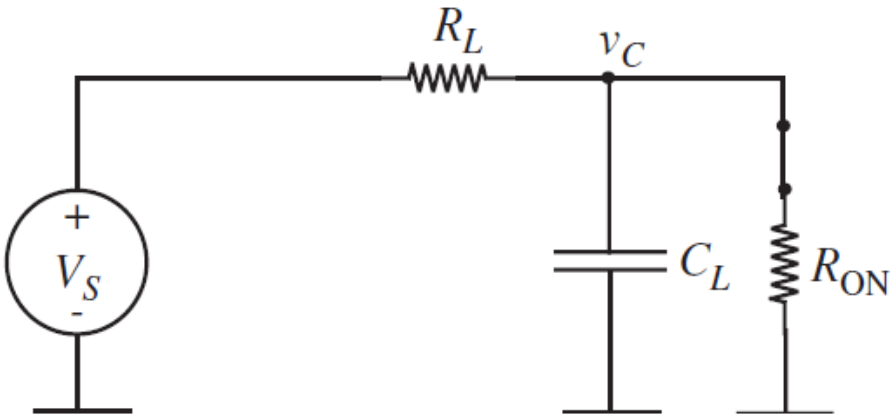




Dynamic Power in NMOS Circuits

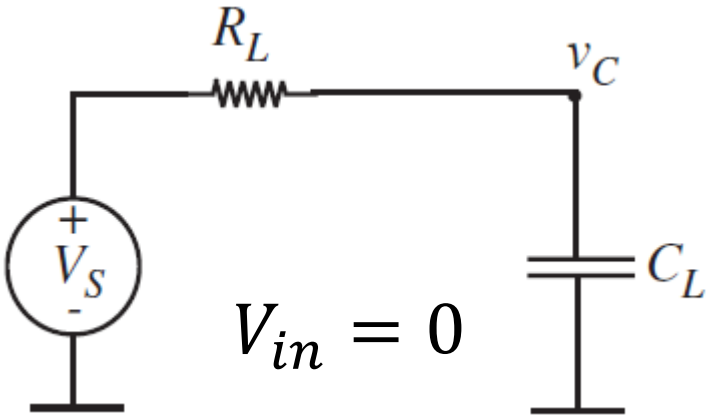
- When our inverter is going from **high to low**, we have the circuit on the left:
- In general, looks like circuit on the right:



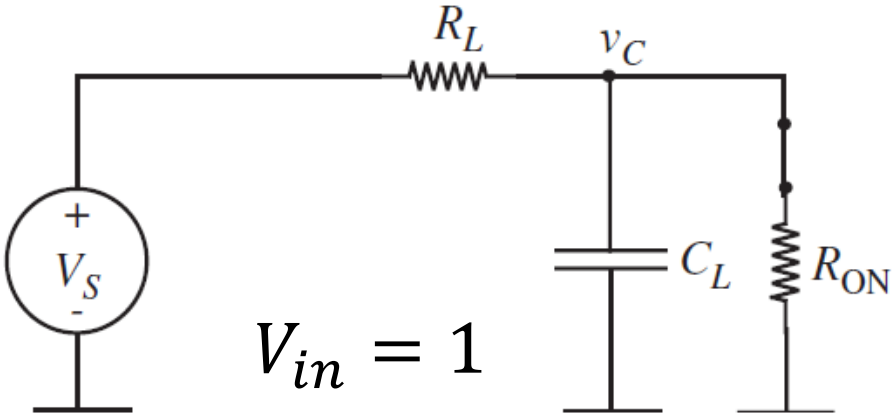


Dynamic Power

- Worst case is that inverter is driven by a sequence of 1s and 0s
  - Circuit constantly switching behavior
  - Gate capacitor constantly charging and discharging



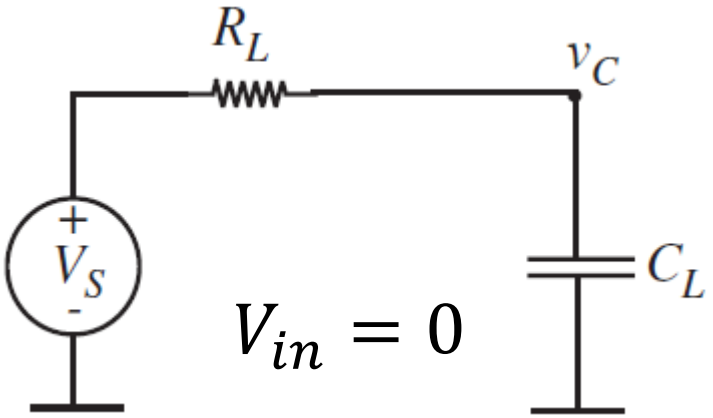
Charges up towards V_S



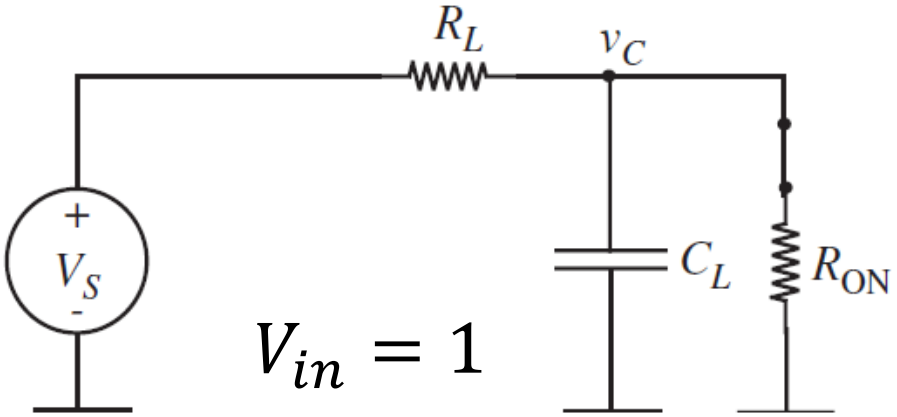
Discharges down towards $V_S \frac{R_{ON}}{R_{ON}+R_L}$

Problem Setup

- V_{in} is
  - 0 for some time T_1
    - Dissipates some energy w_1
  - 1 for some time T_2
    - Dissipates some energy w_2
- $P = \frac{w_1 + w_2}{T_1 + T_2}$
- See 11.1 through 11.3 for derivation



Charges up towards V_S



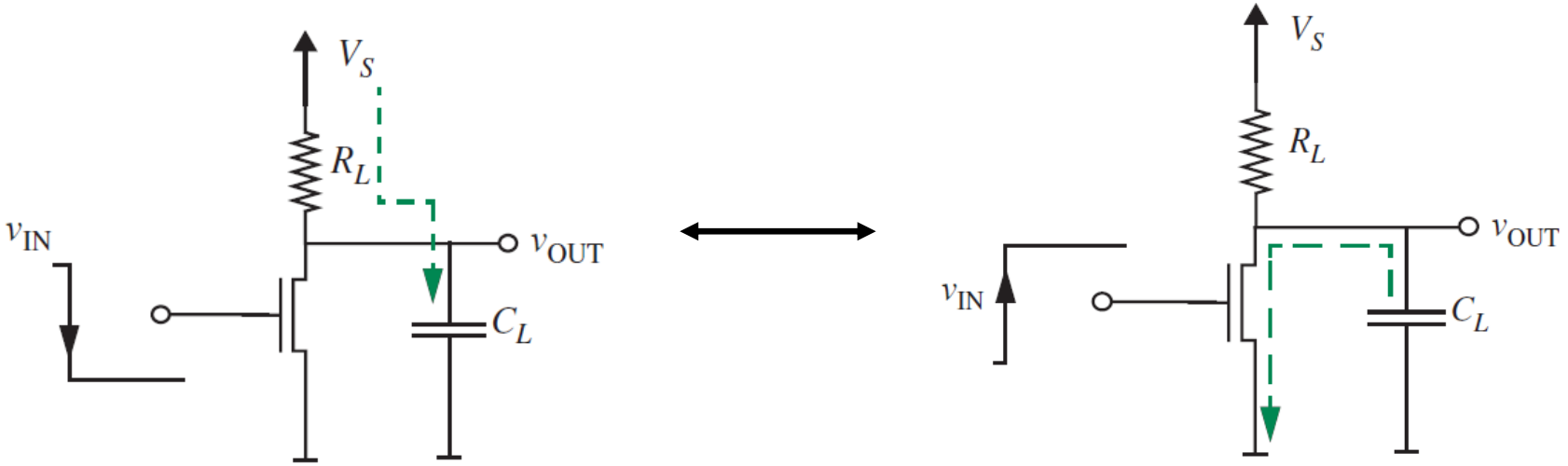
Discharges down towards $V_S \frac{R_{ON}}{R_{ON} + R_L}$

Solution

$$\bar{p} = \frac{V_S^2}{2(R_L + R_{ON})} + \frac{V_S^2 R_L^2 C_L}{(R_L + R_{ON})^2 T}$$

$$p_{static} = \frac{V_S^2}{2(R_L + R_{ON})}$$

$$p_{dynamic} = \frac{V_S^2 R_L^2 C_L}{(R_L + R_{ON})^2 T}$$

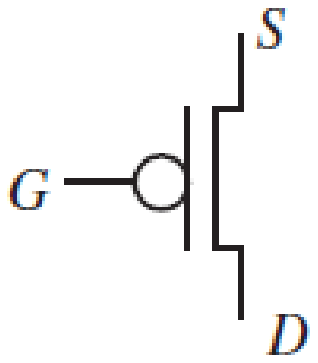


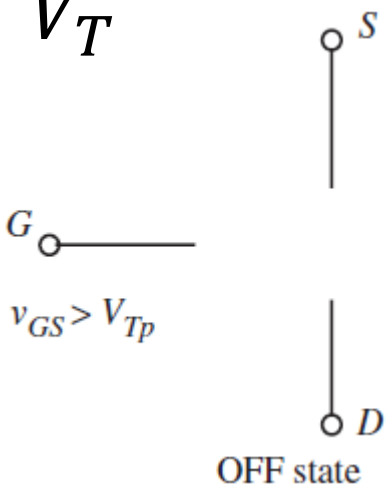
Avoiding Static Power Loss

- Next we will talk about CMOS, which stands for Complementary MOS
- So far, all of our transistors have been NMOS transistors, where they are on if $V_{GS} \geq V_T$
- Next, we will discuss a new type of FET transistor called a PMOS
- Only difference is that they will be on when $V_{GS} \leq V_T$

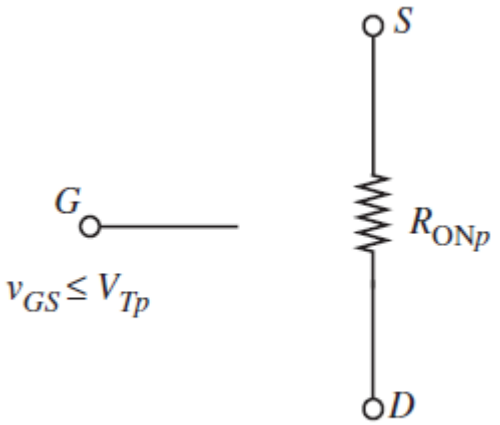
PMOS Transistor

- Drawn with a bubble at the input:
- Usually drawn with source on top and drain on bottom (for reasons that will become clear)
- Just as before, have ON and OFF states, now on when $V_{GS} \leq V_T$





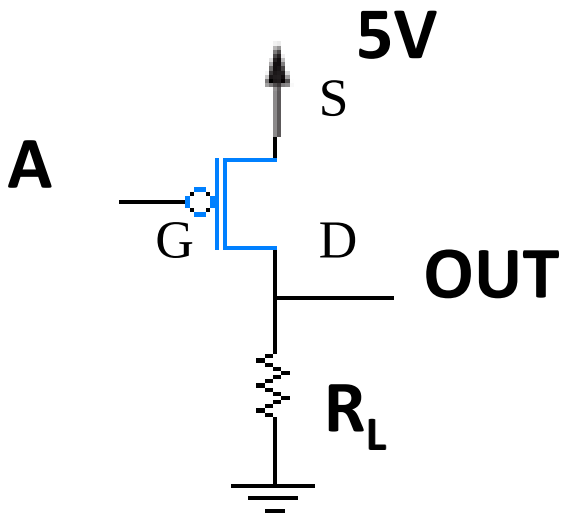
OFF state



ON state

Anything logical we can do with NMOS…

- …we can do with PMOS
- Example, we can build an inverter, try it for a minute or so on the worksheet using a PMOS, 5V source, ground, and resistor
- Assume input signal is 0V or 5V and $V_T = -1V$



Here: R_L acts as a pulldown resistor

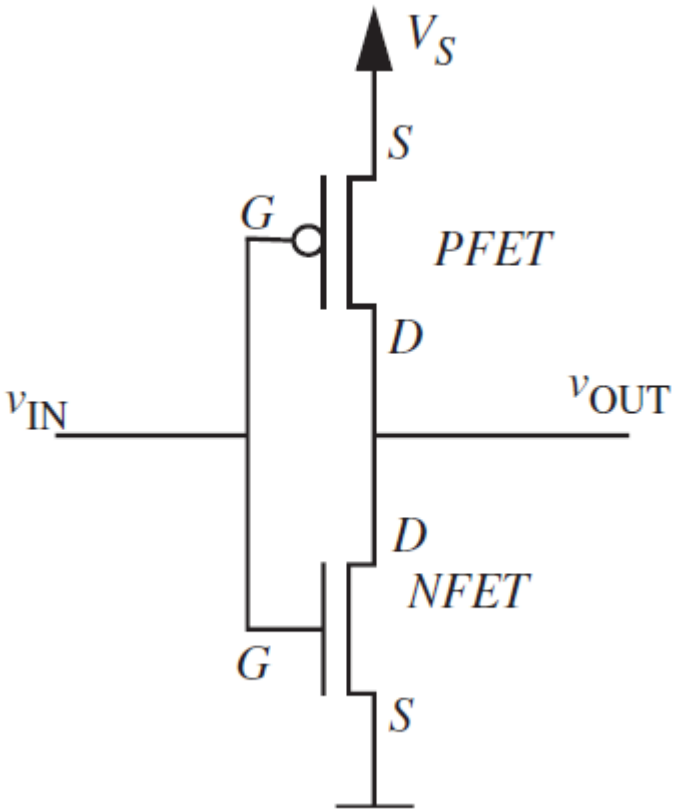
Q13

Analysis of PMOS Logic

- We could go through and repeat everything we did for NMOS, but it would be almost exactly the same thing
- Instead, we're now going to use NMOS and PMOS together in a new clever way

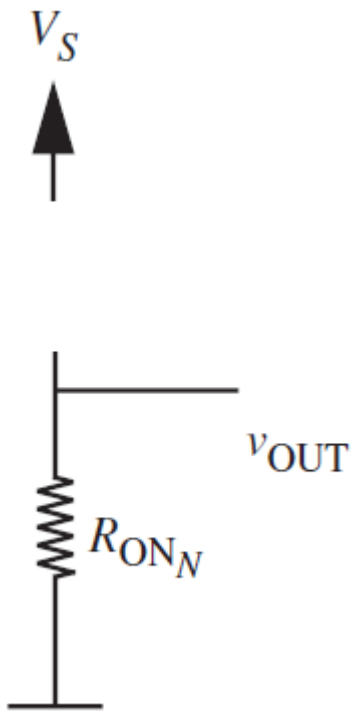
CMOS Inverter

- Two complementary implementations of the same logic function
- When V_{IN} is high:
  - Path to ground is closed
  - Path to V_S is open



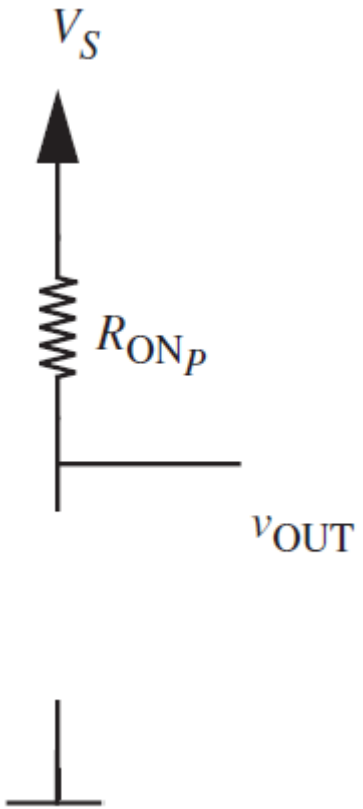
CMOS Inverter

- When V_{IN} is high:
  - Path to ground is closed
  - Path to V_S is open
- Huge resistance on open PMOS acts as a pull-up resistor



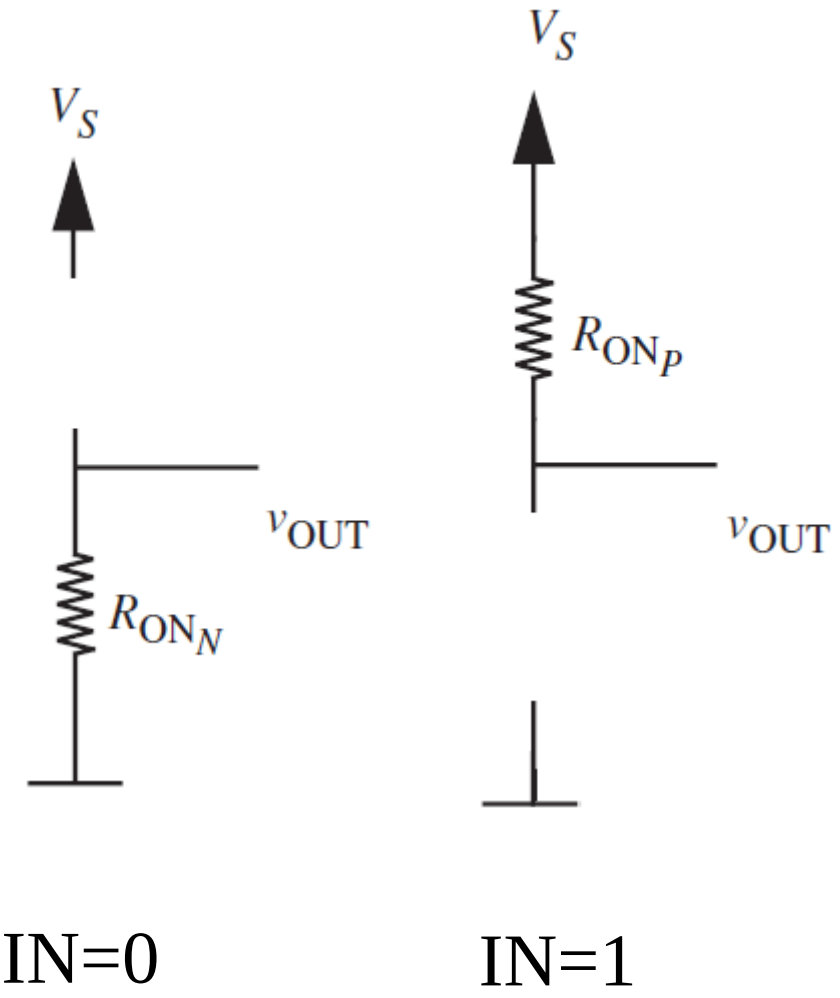
CMOS Inverter

- When V_{IN} is low:
  - Path to ground is open
  - Path to V_S is closed
- Huge resistance on open NMOS acts as a pull-down resistor



Static Power in CMOS

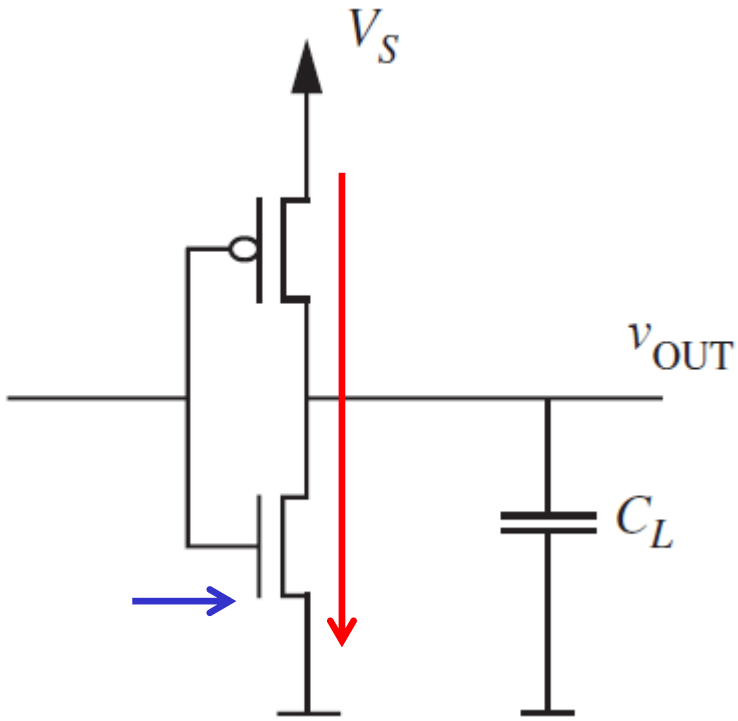
- What is the static power consumed by this CMOS inverter when IN=0?
- When IN=1?
- In reality, there is a substantial static power component



IN=0 IN=1

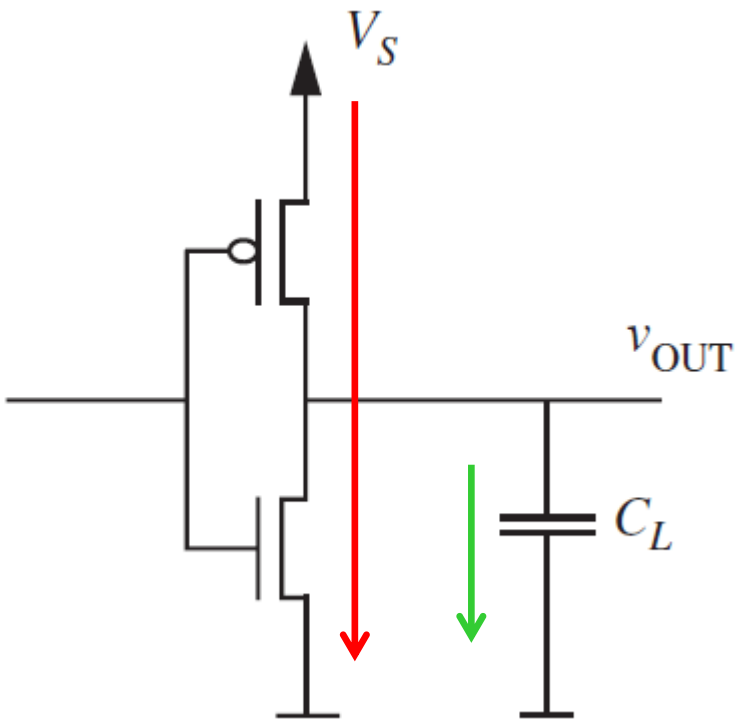
Static Power in CMOS

- **Gate Power**: As gate oxides get smaller, gate current grows
- **Subthreshold Leakage Power**: As thresholds are reduced (to increase speed), transistors are never fully OFF, so current always flows from V_s to V_{low}



Dynamic Power in CMOS

- **Load power**: Since our CMOS gates will be driving capacitive loads, they will still draw power when switching (since power is provided to the load)



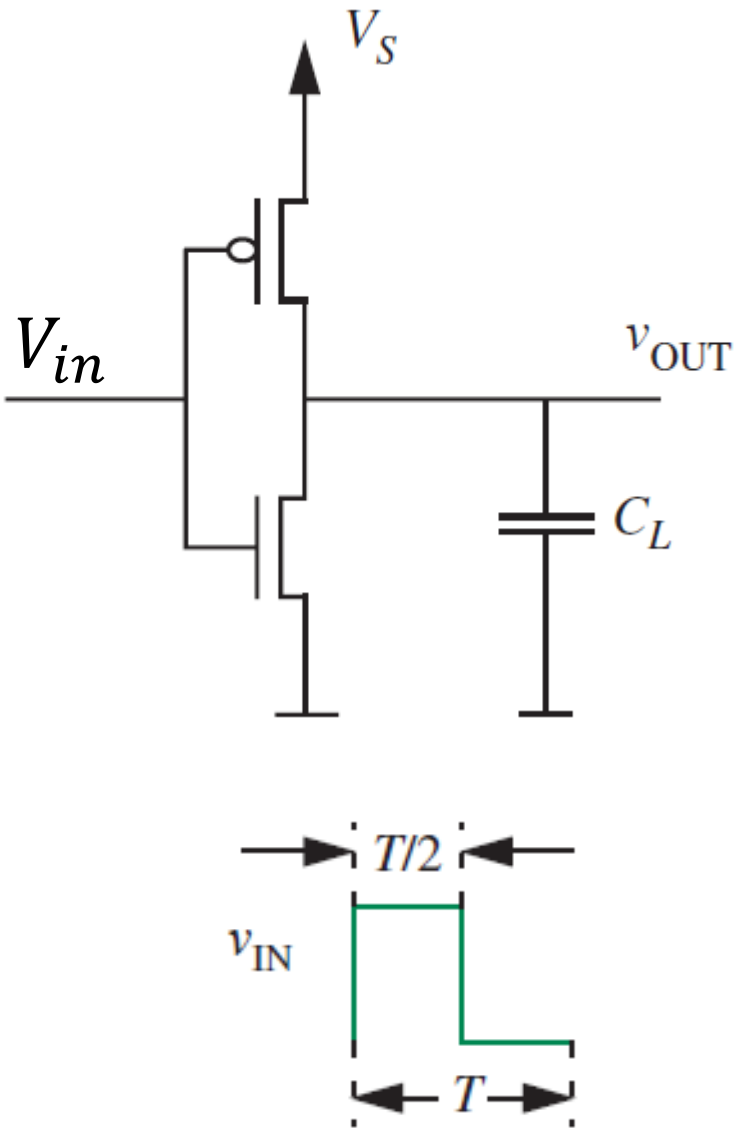
- **STL**: Both transistors are again weakly on at intermediate values

Power in CMOS

- Though **subthreshold leakage** is a significant component to MOSFET power (>50%), it involves a more complex MOSFET model we haven't studied
- We'll instead focus on **dynamic load power**
  - Still accounts for vast portion of chip power consumption

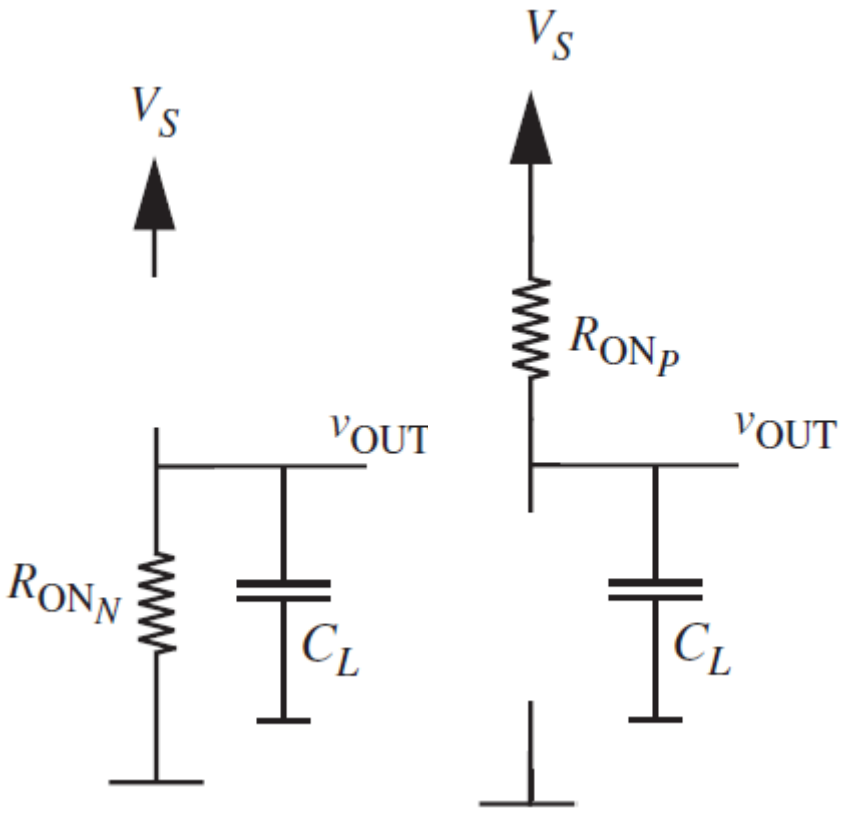
Load Power Analysis

- Assume our inverter is driven by a square wave
- Capacitor will be constantly charging and discharging



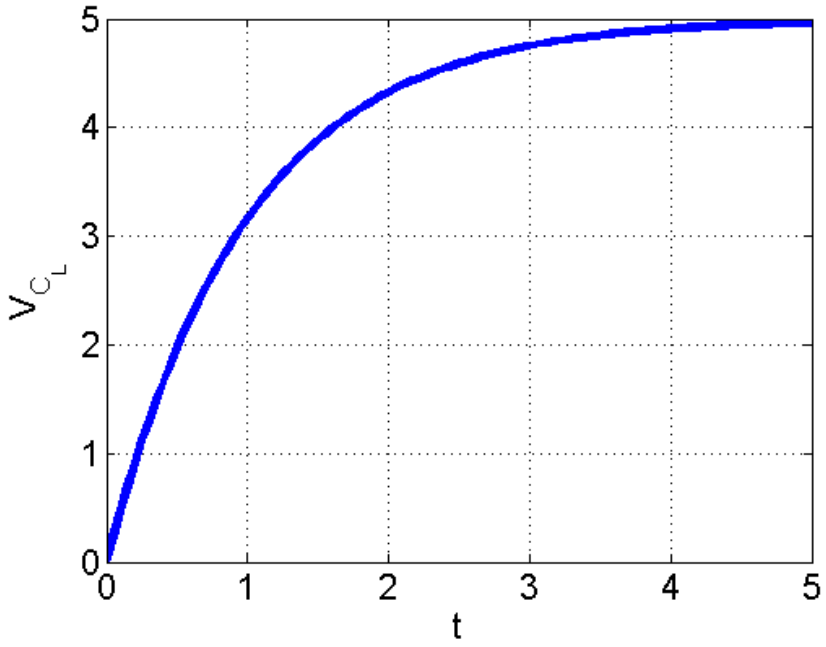
Load Power Analysis

- When input is low, capacitor charges to V_S, energy stored is
  - $\frac{1}{2} C_L V_S^2$
- When input is high, capacitor charges to 0, energy stored is
  - 0

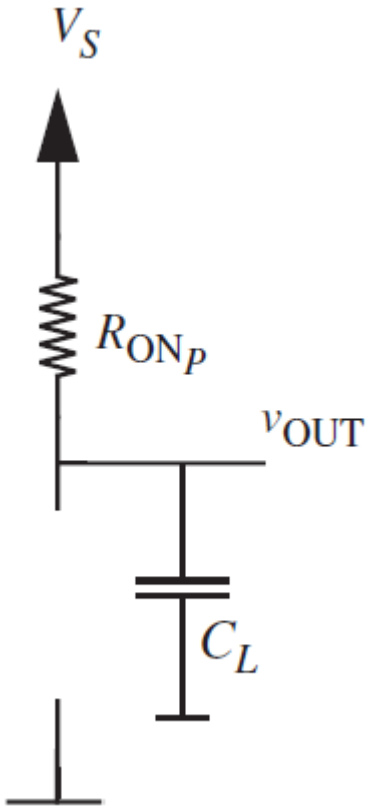


$V_{in} = V_s$ $V_{in} = 0$

Rising Case

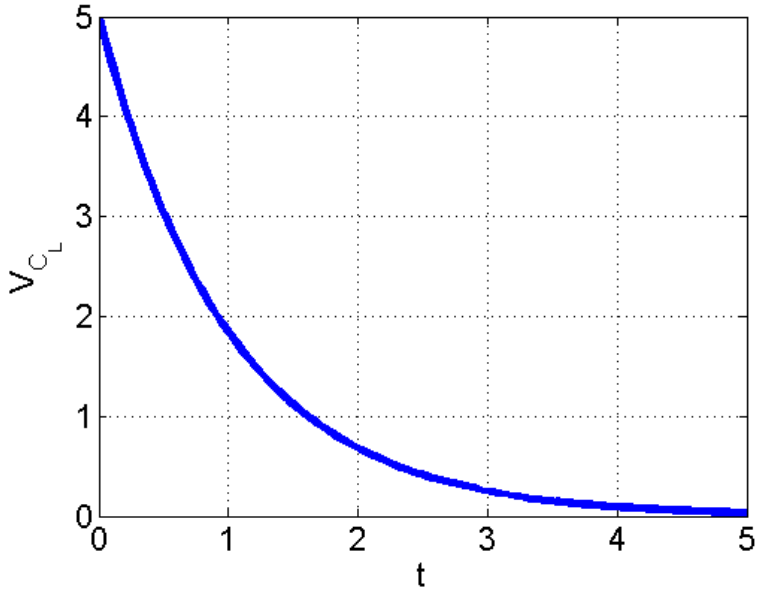


- From homework, how much energy is dissipated in the resistor as C_L charges to V_S?

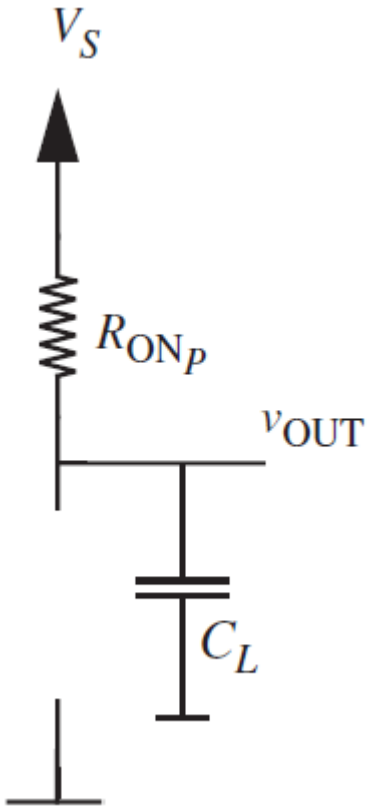


$V_{in} = 0$

Falling Case



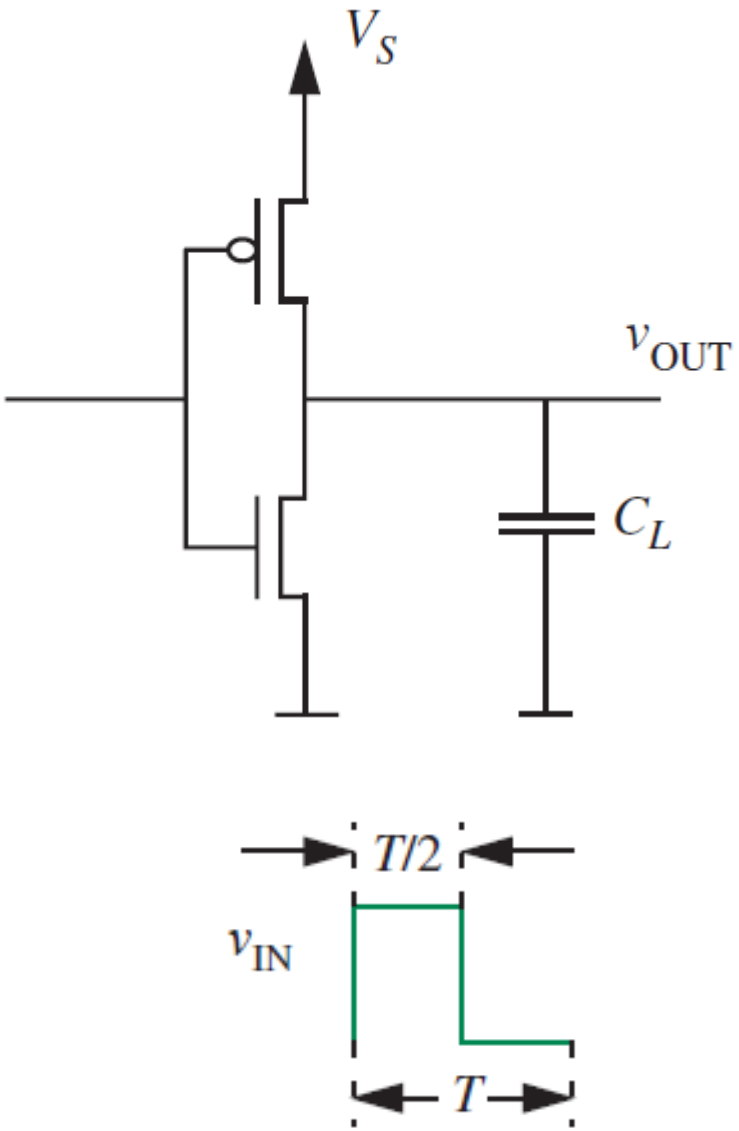
- If capacitor starts with $\frac{1}{2}C_L V_S^2$ Joules of energy, and it all gets dissipated through resistor, then energy dissipated is $\frac{1}{2}C_L V_S^2$



$V_{in} = 0$

Dynamic Load Power

- Thus, if clock cycle is long enough, each switching event consumes $\frac{1}{2} C_L V_S^2$ joules of energy
- In T seconds, we consume $C_L V_S^2$
- Power is $\frac{C_L V_S^2}{T} = C_L V_S^2 f$



CMOS

- CMOS Summary:
  - No need for a pull-up or pull-down resistor
    - Though you can avoid this even with purely NMOS logic (see HW7)
  - Greatly reduced static power dissipation vs. our simple NMOS only logic
    - In reality, MOSFETs are never truly off, and static leakage power consumes >50% of chip power
  - Dynamic power is still hugely significant
  - Uses twice the number of transistors as our simple purely NMOS logic

Preview of Tradeoffs in Digital Circuits

- Processor can do more work per second if f is high
  - Increasing V_S and lowering V_T give faster rise and fall times, letting us increase f
  - Dynamic power (and heat) in CMOS scales as $C_L V_S^2 f$
  - Subthreshold leakage power (and heat) gets larger as V_T gets smaller and as heat increases
- Smarter hardware takes more transistors
  - More area means fewer chips per wafer
  - More transistors means more power consumption

Implementation of Complex Gates Using NMOS and CMOS

- In class, we've discussed analysis of NMOS and CMOS circuits
- Haven't discussed how to design them
- Luckily, it is isn't very hard

Design of NMOS Circuits

- Gates can be designed which use only NMOS transistors and a pull-up resistor
  - Easy to pick parameters to satisfy static discipline
- The basic idea is to **construct an NMOS network which**:
  - **Provides a path from V_{low} to V_{out} ONLY when logical function is false**
  - When path from V_{low} to V_{out} is not available, then $\mathrm{V_{out}} = V_{high}$ through pull-up resistor
- Examples on board

Example on Board

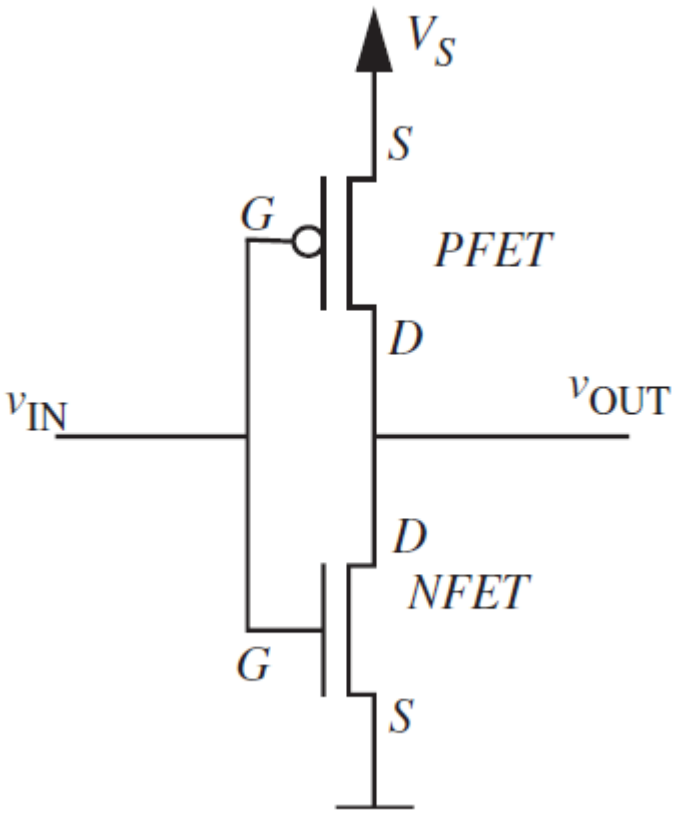
CMOS Design

- In the CMOS case, things are almost exactly the same
- NMOS network which connects V_{low} to V_{out} only when function is false
  - Same network as in NMOS only logic
- PMOS network which connects V_{high} to V_{out} only when function is true
- Examples on board

- This is where we stopped

Model Corner Cases

- What happens if:
  - $V_{in} = 0.99V$
  - $V_{in} = 1.01V$
  - $V_{in} = 1V$
- Real MOSFET model is more complicated
  - Switch can be semi-on
  - i_{DS} saturates for large V_{DS} [not really a resistor]



$V_{t,n} = 1V$

$V_{t,p} = -1V$

Real MOSFET Model

- If we have time this week, we'll discuss a more realistic model of the MOSFET

$$i_{DS} = \begin{cases} K\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right] & \text{for } v_{GS} \geq V_T \text{ and } v_{DS} < v_{GS} - V_T \\ \frac{K(v_{GS}-V_T)^2}{2} & \text{for } v_{GS} \geq V_T \text{ and } v_{DS} \geq v_{GS} - V_T \\ 0 & \text{for } v_{GS} < V_T. \end{cases}$$

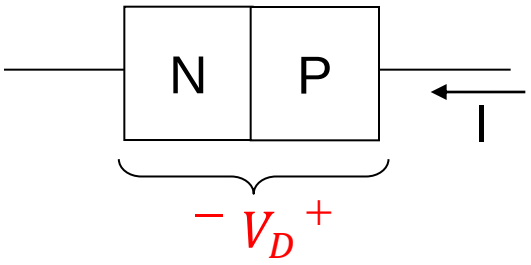
- Useful for understanding invalid input voltages in logic circuits
- More importantly, tells us how we can utilize MOSFETs in analog circuits
  - Op-amps are built from transistors

Nonlinear Elements

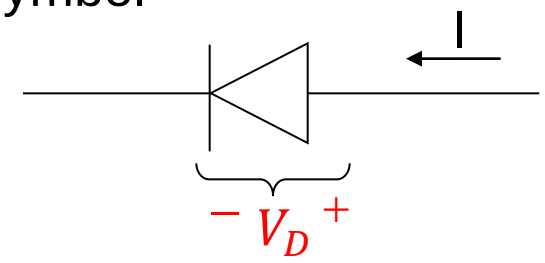
- This more realistic MOSFET model is nonlinear
- MOSFETs are three terminal devices, and it will be tough to begin our nonlinear adventure
  - Functionality is similar to what we've seen before (op-amps)
  - Analysis is tough
- We'll instead turn to diodes
  - Interesting new function
  - Analysis is easier
- If we have time, we will talk on Friday or Monday about analog MOSFET circuits

Diode Physical Behavior and Equation

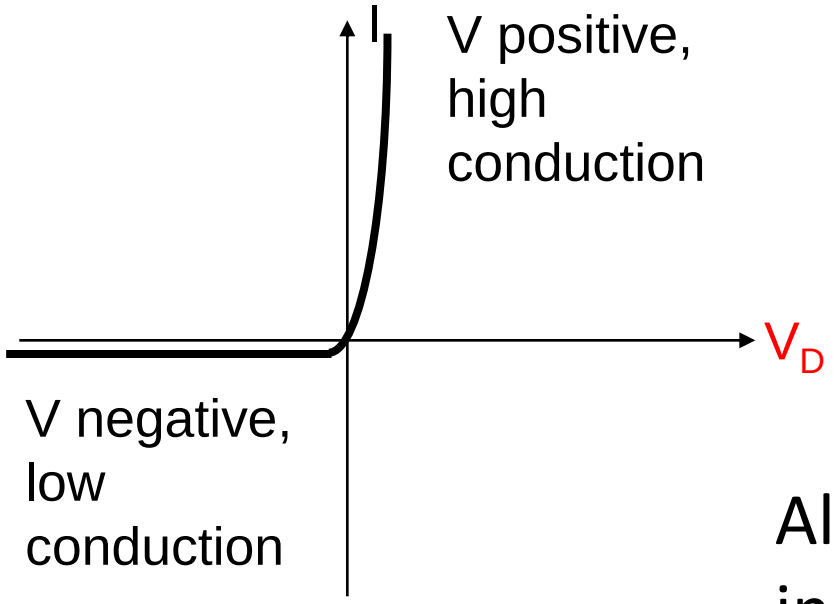
Schematic Device



Symbol



Qualitative I-V characteristics:



Quantitative I-V characteristics:

$$I = I_O(e^{V_D/nV_T} - 1)$$

$$V_T = \frac{kT}{q} = 0.026V$$

n: 1 to 2

I_O: $10^{-15}A$ to $10^{-12}A$

Allows significant current flow in only one direction

The pn Junction I vs. V Equation

I-V characteristic of PN junctions

In EECS 105, 130, and other courses you will learn why the I vs. V relationship for PN junctions is of the form

$$I = I_O(e^{V_D/nV_T} - 1) \qquad V_T = \frac{kT}{q} = 0.026V$$

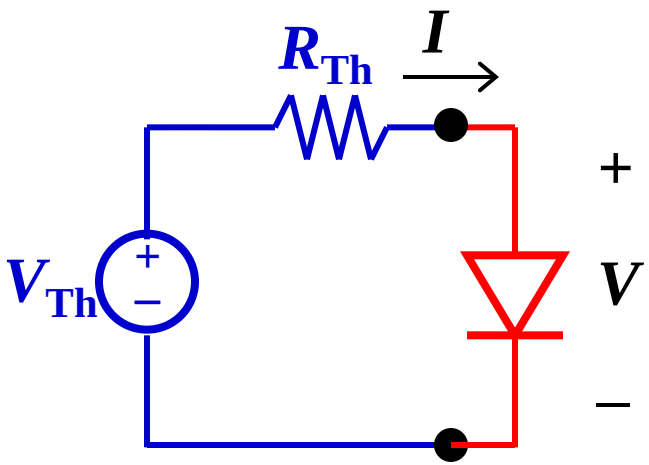
where I_0 is a constant related to device area and materials used to make the diode, $q = \text{electronic charge} = 1.6\times10^{-19}$,
k is Boltzman constant, and T is absolute temperature.
$KT/q = 0.026\text{V at} 300°\text{K}$, a typical value for I_0 is $10^{-12} - 10^{-15}$ A

We note that in forward bias, I increases **exponentially** and is in the μA-mA range for voltages typically in the range of 0.6-0.8V.
In reverse bias, the current is essentially zero.

Solving diode circuits

- How do we solve this circuit?
- KCL at the top right node:

$$\frac{V - V_{Th}}{R_{Th}} = I_O\left(e^{\frac{V}{0.026}} - 1\right)$$



Quantitative I-V characteristics:

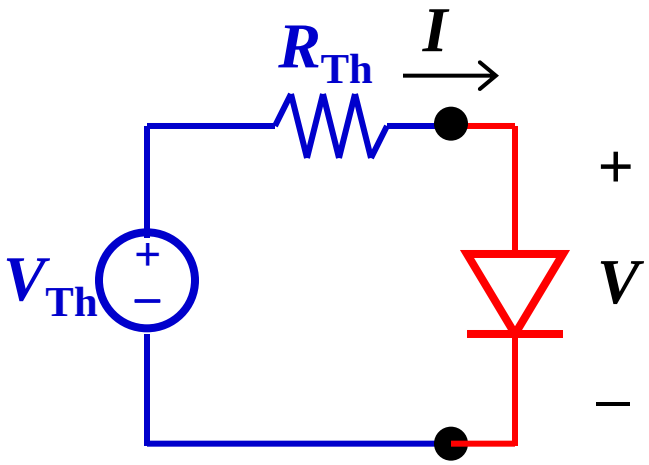
$$I = I_O(e^{V_D/V_T} - 1)$$

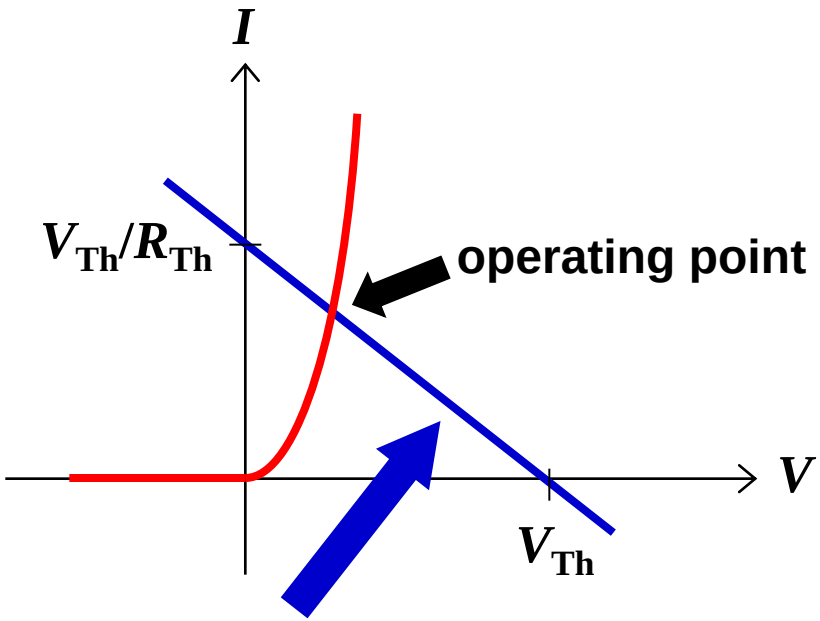
n=1

No algebraic solution!

Load Line Analysis Method

1. Graph the *I-V* relationships for the non-linear element and for the rest of the circuit
2. The operating point of the circuit is found from the intersection of these two curves.



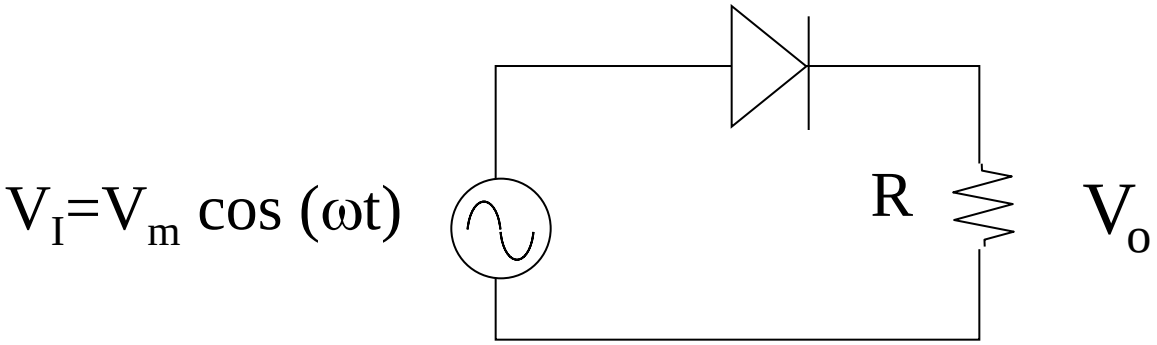


$$\frac{V - V_{Th}}{R_{Th}} = I_O\left(e^{\frac{V}{0.026}} - 1\right)$$

The *I-V* characteristic of all of the circuit except the non-linear element is called the *load line*

Load Line Example: Power Conversion Circuits

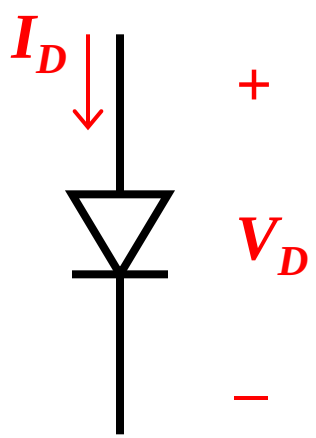
- Converting AC to DC
- Potential applications: Charging a battery



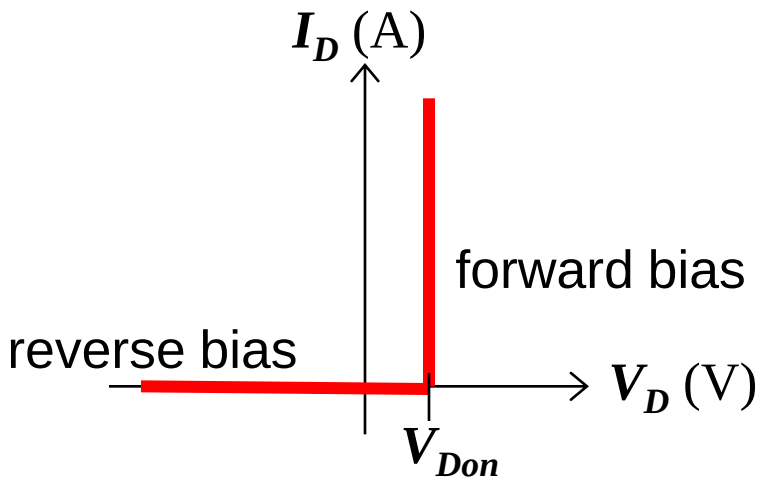
- Can we use phasors?
- Example on board

Piecewise Linear Model

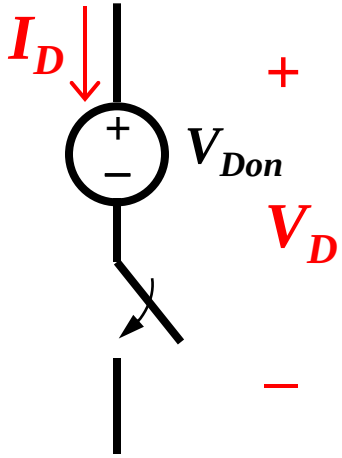
Circuit symbol



***I-V* characteristic**



Switch model



For a Si pn diode, $V_{Don} \cong 0.7$ V

RULE 1: When $I_D > 0$, $V_D = V_{Don}$

RULE 2: When $V_D < V_{Don}$, $I_D = 0$

Diode behaves like a voltage source in series with a switch:
- **closed in forward bias mode**
- **open in reverse bias mode**

How to Analyze Diode Circuits with Piecewise Linear Model

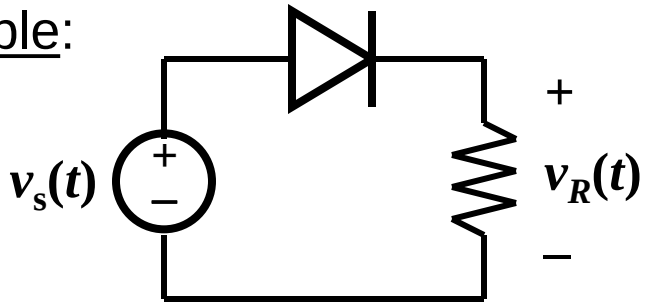
A diode has only two states:

- **forward biased:** $I_D > 0$, $V_D = 0.7$ V
- **reverse biased:** $I_D = 0$, $V_D < 0.7$ V

Procedure:

1. Guess the state(s) of the diode(s)
2. Check to see if KCL and KVL are obeyed.
3. If KCL and KVL are not obeyed, refine your guess
4. Repeat steps 1-3 until KCL and KVL are obeyed.

Example:



If $v_s(t) > 0.7$ V, diode is forward biased (else KVL is disobeyed – try it)

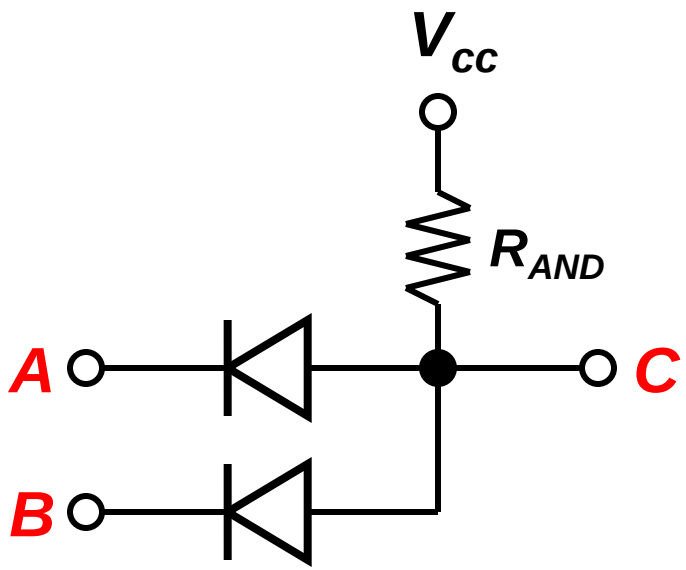
If $v_s(t) < 0.7$ V, diode is reverse biased (else KVL is disobeyed – try it)

Diode Logic: AND Gate

- Diodes can be used to perform logic functions:

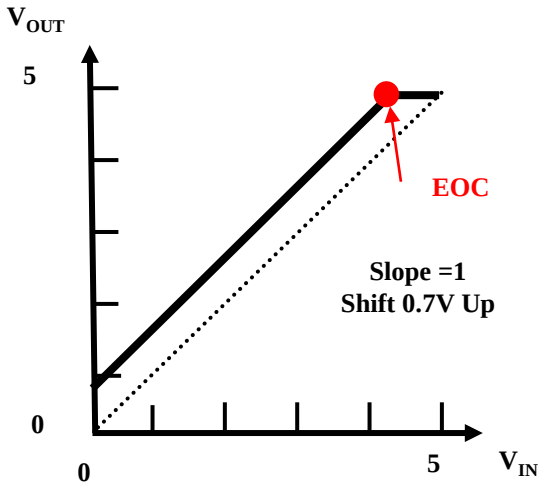
AND gate

output voltage is high only if both A and B are high



Inputs A and B vary between 0 Volts ("low") and V_{cc} ("high")

Between what voltage levels does C vary?



Diode Logic: OR Gate

- Diodes can be used to perform logic functions:

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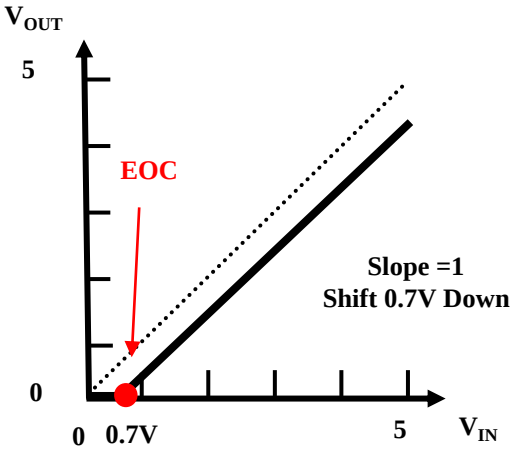
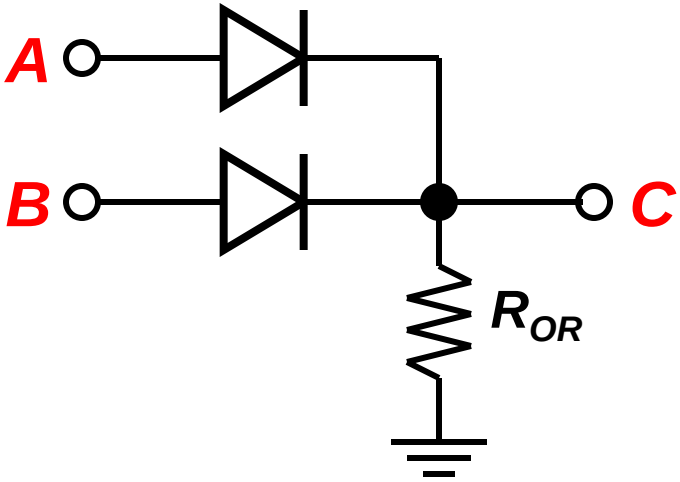


OR gate

output voltage is high if either (or both) A and B are high



Diode Logic: Incompatibility and Decay

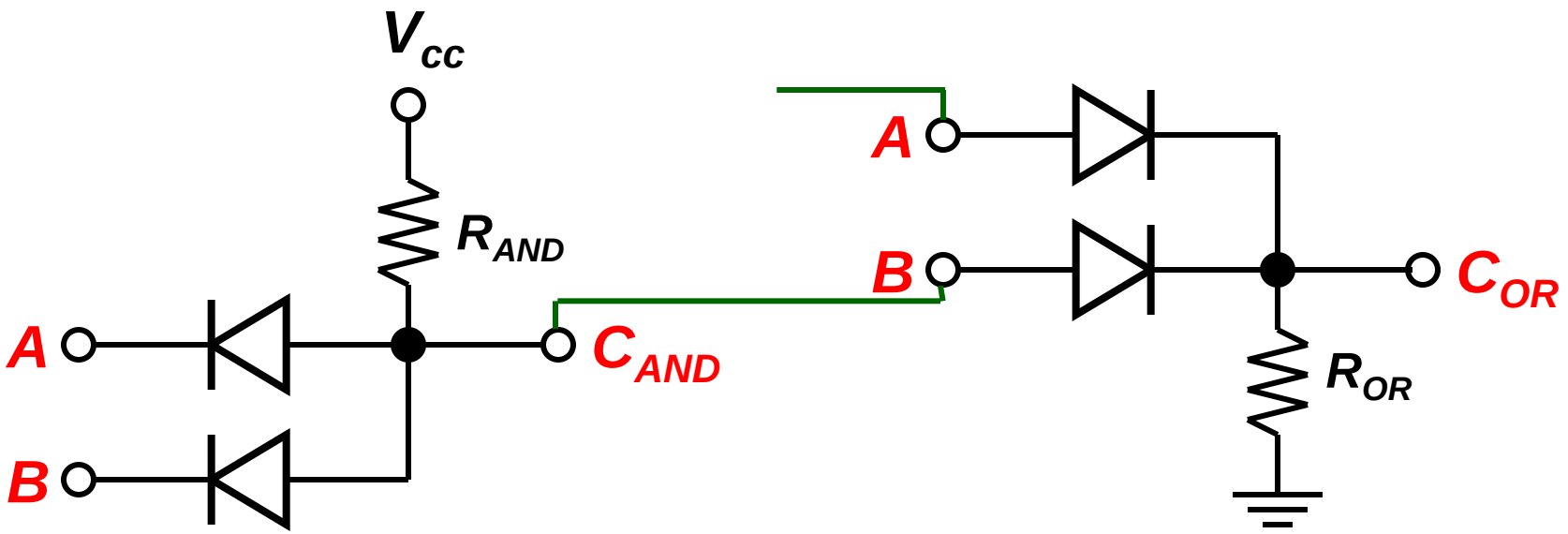
- Diode Only Gates are Basically Incompatible:

AND gate

output voltage is high only if both A and B are high

OR gate

output voltage is high if either (or both) A and B are high



Signal Decays with each stage (Not regenerative)

That's all for today

- Next time, more Diodes and a little more on the more realistic model of MOSFETs