EE40
Lecture 17
Josh Hug

8/04/2010

Logistics

- HW8 will be due Friday
- Mini-midterm 3 next Wednesday
  - 80/160 points will be a take-home set of design problems which will utilize techniques we've covered in class
    - Handed out Friday
    - Due next Wednesday
  - Other 80/160 will be an in class midterm covering HW7 and HW8
- Final will include Friday and Monday lecture, Midterm won't
  - Design problems will provide practice

Project 2

- Booster lab actually due next week
  - For Booster lab, ignore circuit simulation, though it may be instructive to try the Falstad simulator
- Project 2 due next Wednesday
  - Presentation details to come [won't be mandatory, but we will ask everyone about their circuits at some point]

Project 2

- For those of you who want to demo Project 2, we'll be doing demos in lab on Wednesday at some point
  - Will schedule via online survey

CMOS/NMOS Design Correction

- (Sent by email)
- My on-the-fly explanation was correct, but not the most efficient way
  - If your FET circuit is implementing a logic function with a bar over it, i.e.
    - $Z = \overline{A + BC + D + EF(G + H)}$
  - Then don't put an inverter at the output, it just makes things harder and less efficient
- Sorry, on-the-fly-explanations can be dicey

CMOS

- CMOS Summary:
  - No need for a pull-up or pull-down resistor
    - Though you can avoid this even with purely NMOS logic (see HW7)
  - Greatly reduced static power dissipation vs. our simple NMOS only logic
    - In reality, MOSFETs are never truly off, and static leakage power consumes >50% of chip power
  - Dynamic power is still hugely significant
  - Uses twice the number of transistors as our simple purely NMOS logic

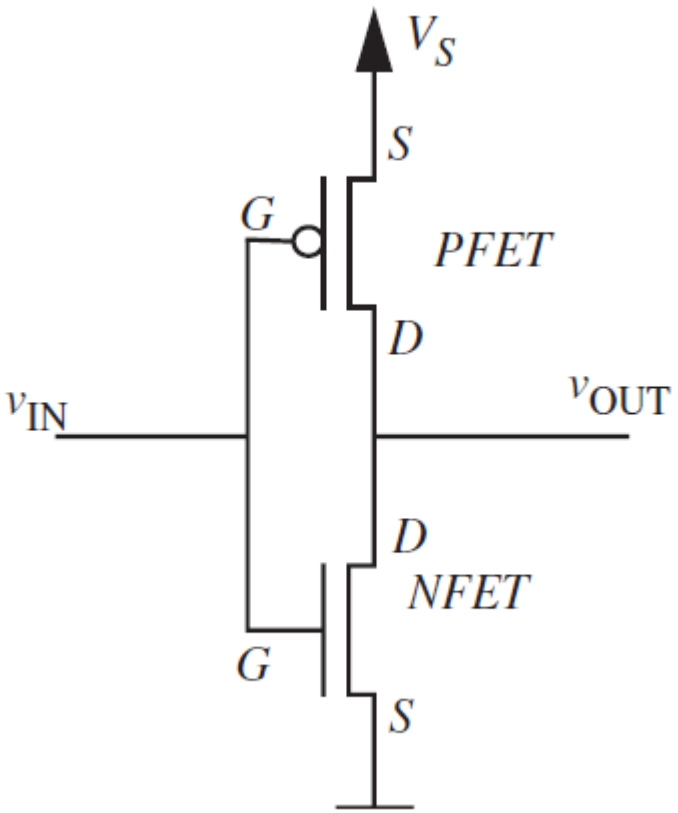
Tradeoffs in Digital Circuits

- Processor can do more work per second if f is high
  - Increasing V_S and lowering V_T give faster rise and fall times, letting us increase f
  - Dynamic power (and heat) in CMOS scales as $C_L V_S^2 f$
  - Subthreshold leakage power (and heat) gets larger as V_T gets smaller and as heat increases
- Smarter hardware takes more transistors
  - More area means fewer chips per wafer
  - More transistors means more power consumption

Model Corner Cases

- What happens if:
  - $V_{in} = 0.99V$
  - $V_{in} = 1.01V$
  - $V_{in} = 1V$

- Real MOSFET model is more complicated
  - Switch can be semi-on
  - i_{DS} saturates for large V_{DS} [not really a resistor]



$$V_{t,n} = 1V$$
$$V_{t,p} = -4V$$

Real MOSFET Model

- If we have time this week, we'll discuss a more realistic model of the MOSFET

$$i_{DS} = \begin{cases} K\left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}\right] & \text{for } v_{GS} \geq V_T \text{ and } v_{DS} < v_{GS} - V_T \\ \frac{K(v_{GS}-V_T)^2}{2} & \text{for } v_{GS} \geq V_T \text{ and } v_{DS} \geq v_{GS} - V_T \\ 0 & \text{for } v_{GS} < V_T. \end{cases}$$

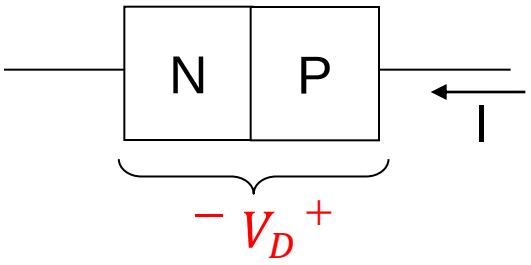
- Useful for understanding invalid input voltages in logic circuits
- More importantly, tells us how we can utilize MOSFETs in analog circuits
  - Op-amps are built from transistors

Nonlinear Elements

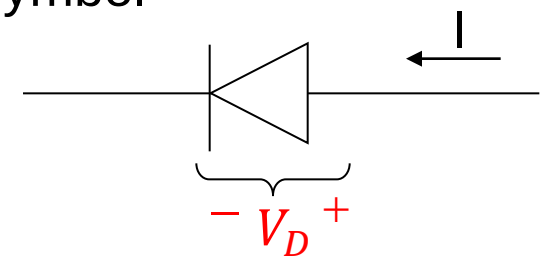
- This more realistic MOSFET model is nonlinear
- MOSFETs are three terminal nonlinear devices. We will get back to these briefly on Friday
  - Functionality is similar to what we've seen before (op-amps)
  - Analysis isn't too bad, but will take too long to go through. If you're curious see chapters 7 and 8.
- We'll instead turn to diodes
  - Interesting new function
  - Analysis is easier

Diode Physical Behavior and Shockley Equation

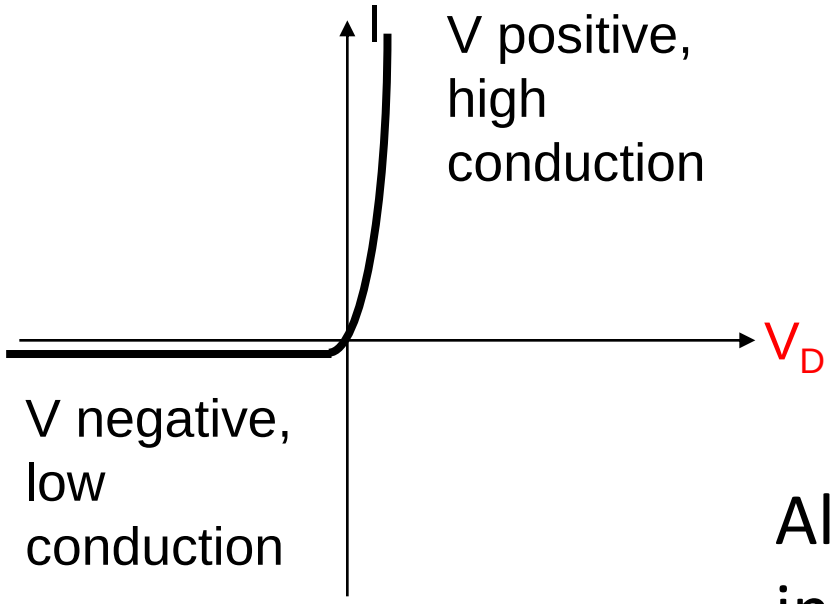
Physical Device



Symbol



Qualitative I-V characteristics:



Quantitative I-V characteristics:

$$I = I_O(e^{V_D/nV_T} - 1)$$

$$V_T = \frac{kT}{q} = 0.026V$$

n: 1 to 2

I_O: $10^{-15}A$ to $10^{-12}A$

Allows significant current flow in only one direction

The pn Junction I vs. V Equation

I-V characteristic of PN junctions

In EECS 105, 130, and other courses you will learn why the I vs. V relationship for PN junctions is of the form

$$I = I_O(e^{V_D/nV_T} - 1) \qquad V_T = \frac{kT}{q} = 0.026V$$

where I_0 is a constant related to device area and materials used to make the diode, $q = \text{electronic charge} = 1.6\times10^{-19}$,
k is Boltzman constant, and T is absolute temperature.

a typical value for I_0 is $10^{-12} - 10^{-15}$ A

We note that in forward bias, I increases **exponentially** and is in the μA-mA range for voltages typically in the range of 0.6-0.8V.
In reverse bias, the current is essentially zero.

Shockley Equation for the Diode

$$I = I_O(e^{V_D/nV_T} - 1)$$

$$V_T = \frac{kT}{q} = 0.026V$$

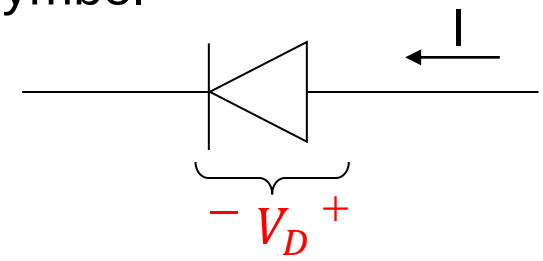
For typical values:

$$T = 300K$$

$$I_O = 10^{-12}A$$

Real Diodes will eventually become linear for large V_D, and for really large V_D they'll die

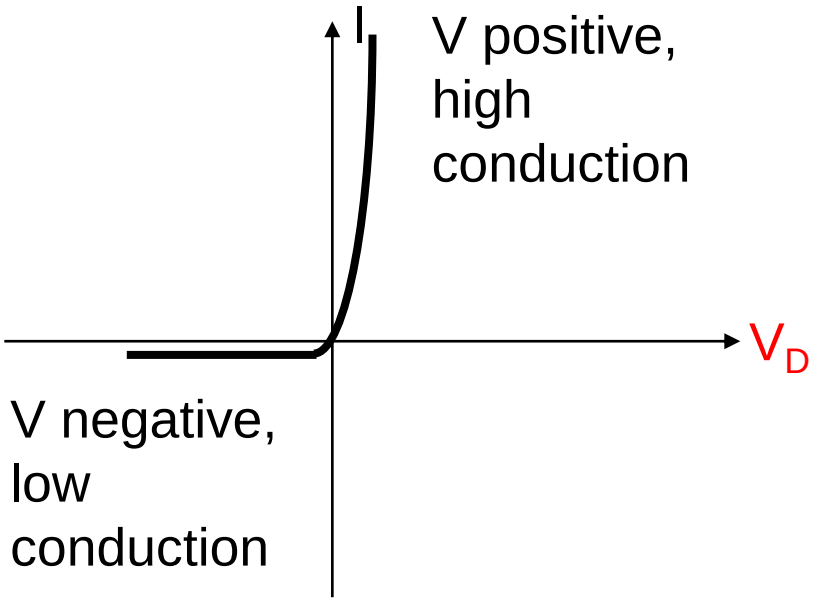
Symbol



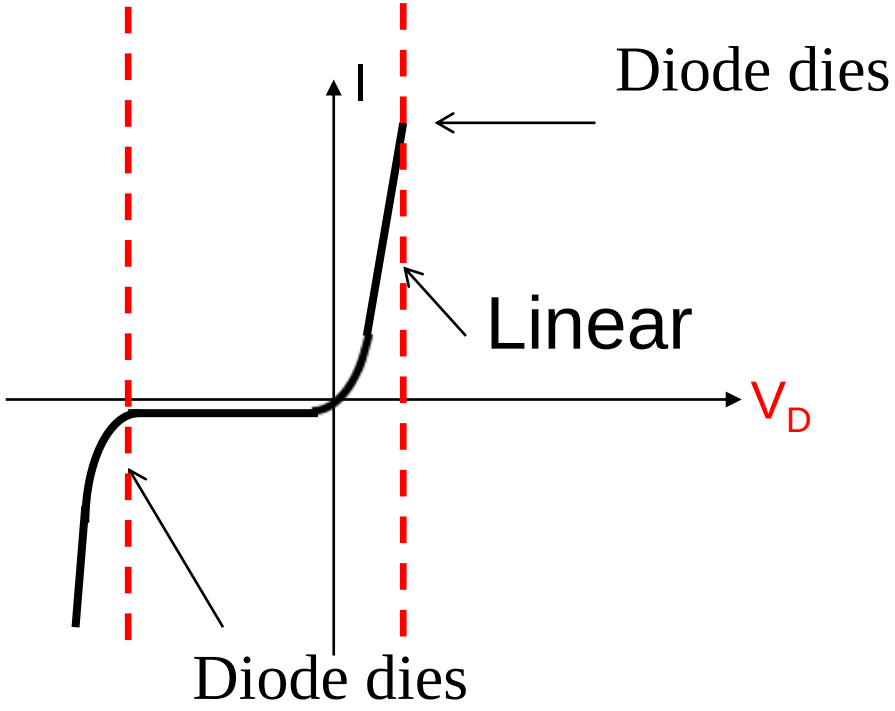
V_D (volts)	I (amps)
-1	−0.000000000001
-0.1	−0.0000000000098
0	0
0.1	0.000000000045
0.3	0.000000102
0.6	0.01
0.7	0.49
0.8	23
0.9	1080

Large Voltage Limits of the Diode

Qualitative I-V characteristics: (small V)



Qualitative I-V characteristics: (large V)



Green LEDs in lab:

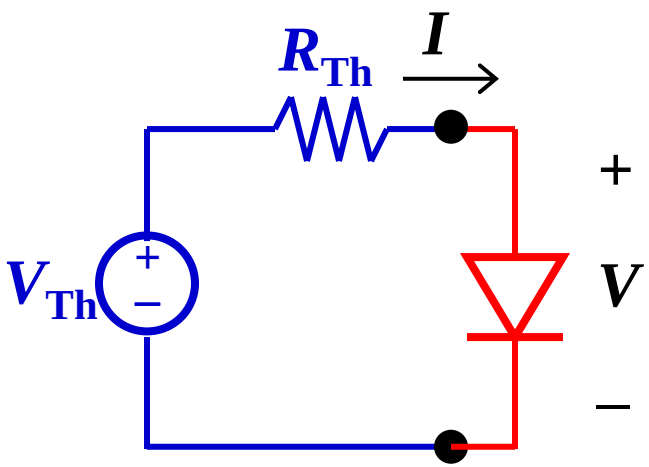
Linear for $\geq$ 2.3V

Die at $\approx$ 6V

Solving diode circuits

- How do we solve this circuit assuming zoomed-in region?
- KCL at the top right node:

$$\frac{V_{Th} - V}{R_{Th}} = I_O\left(e^{\frac{V}{0.026}} - 1\right)$$



Quantitative I-V characteristics:

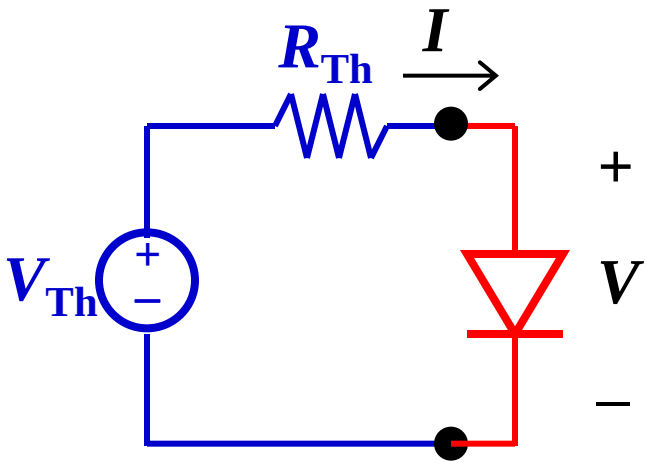
$$I = I_O(e^{V_D/V_T} - 1)$$

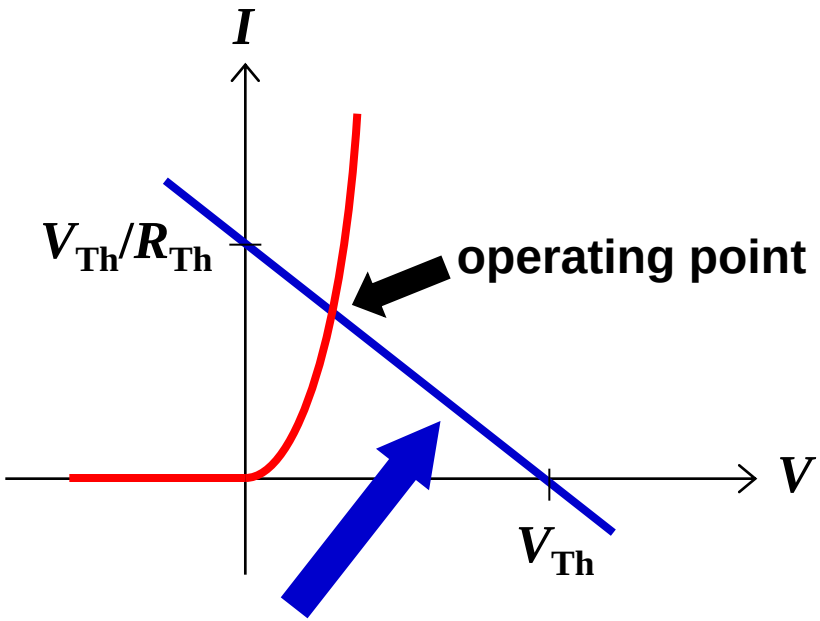
n=1

No algebraic solution!

Load Line Analysis Method

1. Graph the *I-V* relationships for the non-linear element and for the rest of the circuit
2. The operating point of the circuit is found from the intersection of these two curves.



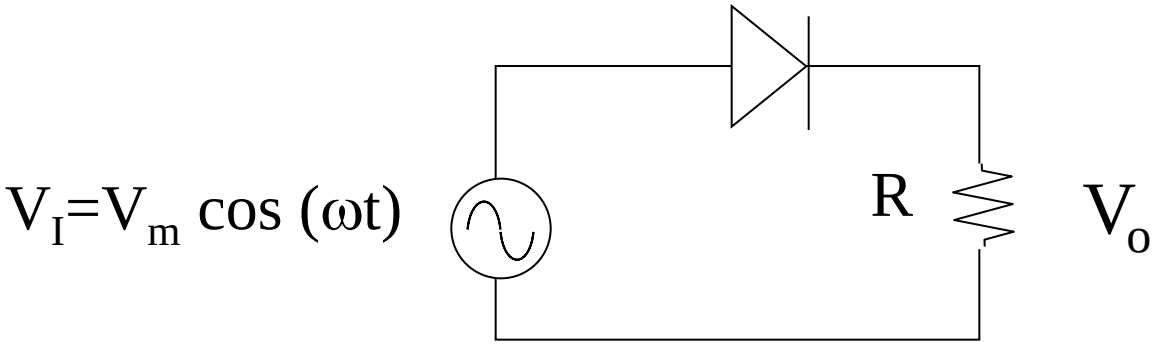


$$\frac{V_{Th} - V}{R_{Th}} = I_O\left(e^{\frac{V}{0.026}} - 1\right)$$

The *I-V* characteristic of all of the circuit except the non-linear element is called the *load line*

Load Line Example: Power Conversion Circuits

- Converting AC to DC
- Potential applications: Charging a battery

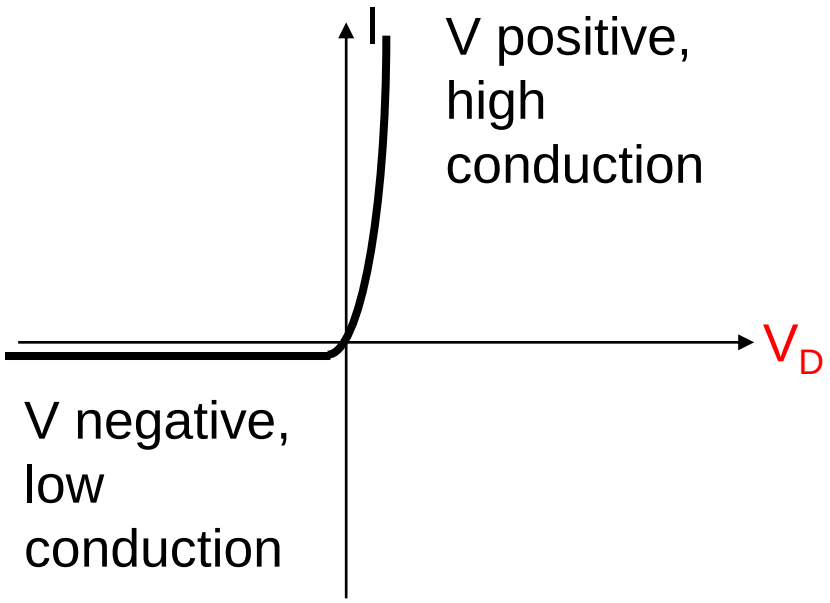


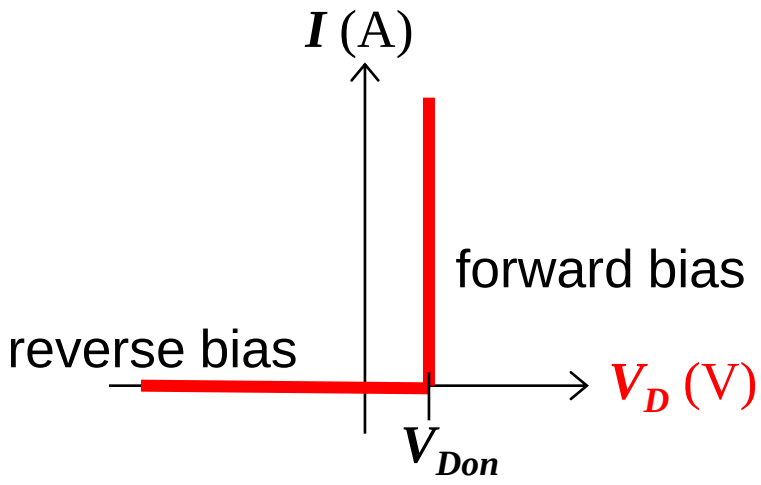
- Can we use phasors?
- Example on board

Simple Model of a Diode

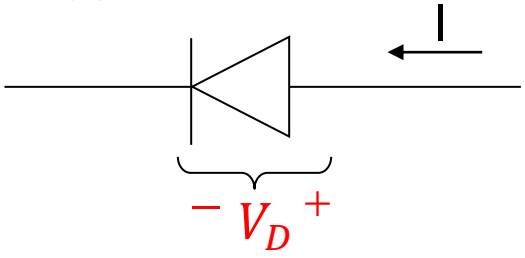
- Just as we did with MOSFETs, we will utilize a simpler model
  - Goal: Accurate enough that we can design circuits
- For Diodes, we started with the “real” model and are now simplifying
- For MOSFETs, we started with the simplest model, and added complexity
  - Omitted real model for MOSFETs because it’s not very intuitive [unlike real diodes]

Simpler Diode Model





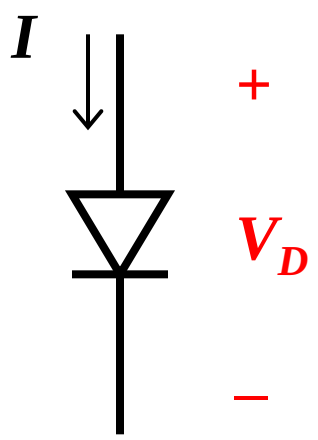
Symbol



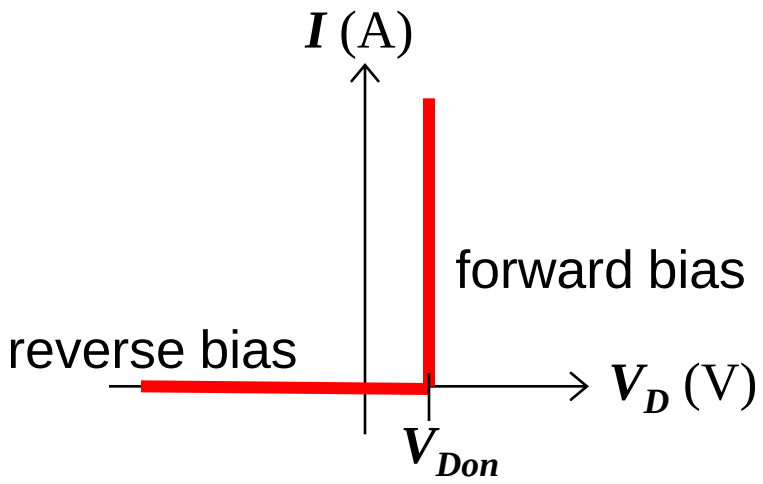
Goal: To give us approximately the right answer for most inputs

Voltage Source Model

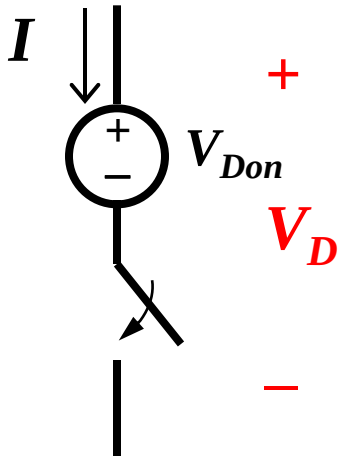
Circuit symbol



***I-V* characteristic**



VS model



For a Si pn diode, $V_{Don} \cong 0.7$ V

ON: When $I_D > 0$, $V_D = V_{Don}$

OFF: When $V_D < V_{Don}$, $I_D = 0$

Diode behaves like a voltage source in series with a switch:
- **closed in forward bias mode**
- **open in reverse bias mode**

How to Analyze Diode Circuits with Method of Assumed States

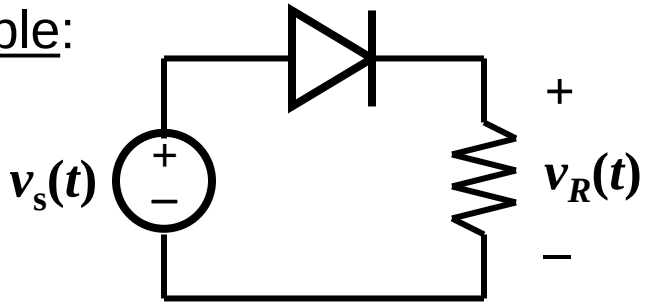
A diode has only two states:

- **forward biased:** $I_D > 0$, $V_D = 0.7$ V (or some other V_K)
- **reverse biased:** $I_D = 0$, $V_D < 0.7$ V

Procedure:

1. Guess the state(s) of the diode(s), drawing equivalent circuit given diode states
2. Check to see if your resulting voltages and currents match assumptions.
3. If results don't match assumptions, guess again
4. Repeat until you get a consistent guess

Example:



If $v_s(t) > 0.7$ V, diode is forward biased

If $v_s(t) < 0.7$ V, diode is reverse biased

Bigger Examples on Board

- DC Source with 2 Diodes
- Half-wave rectifier
- Full-wave rectifier
- See written notes

That's all for today

- Next time, maybe a little more diodes and then semiconductor physics and how solar cells, diodes, and MOSFETs work
- Time permitting we may talk about real model of a MOSFET

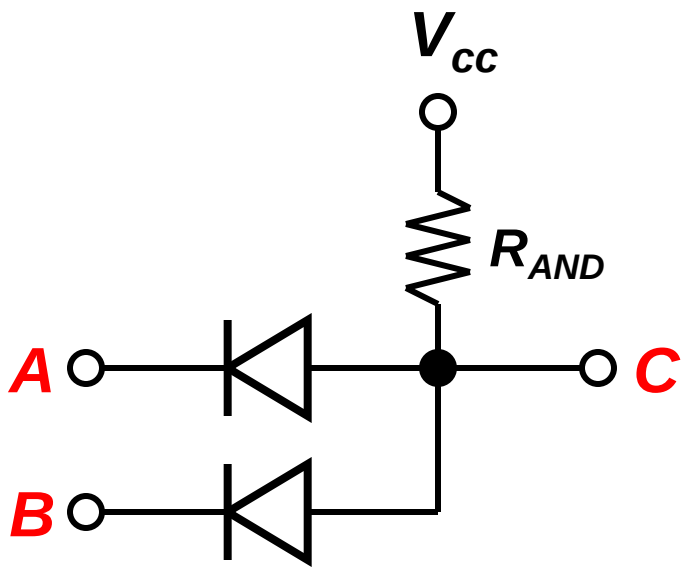
Extra Slides

Diode Logic: AND Gate

- Diodes can be used to perform logic functions:

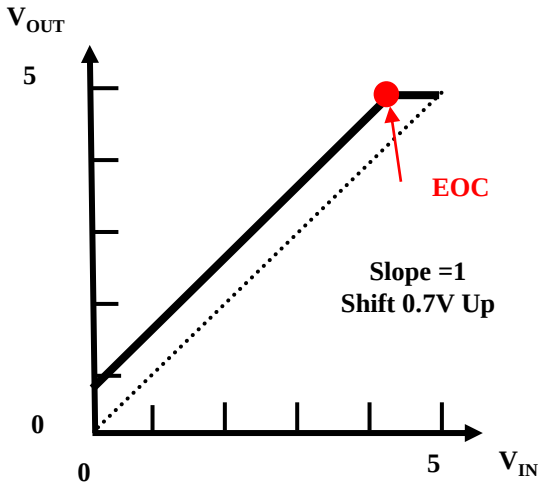
AND gate

output voltage is high only if both A and B are high



Inputs A and B vary between 0 Volts ("low") and V_{cc} ("high")

Between what voltage levels does C vary?



Diode Logic: OR Gate

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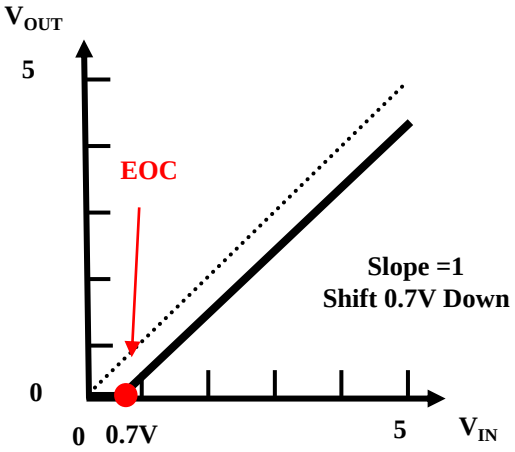
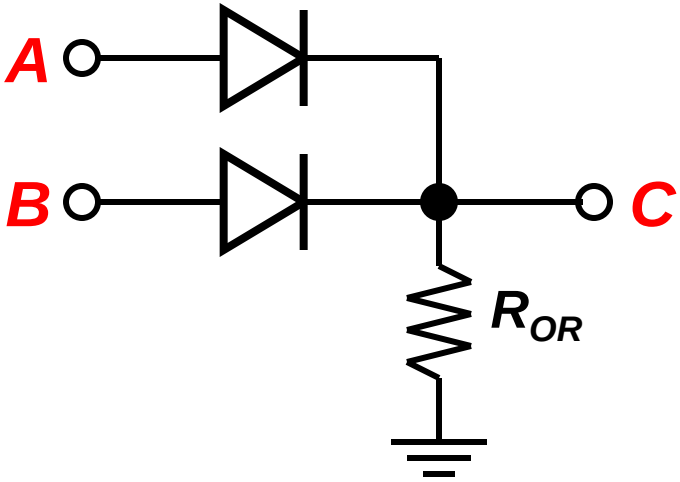


OR gate

output voltage is high if either (or both) A and B are high



Diode Logic: Incompatibility and Decay

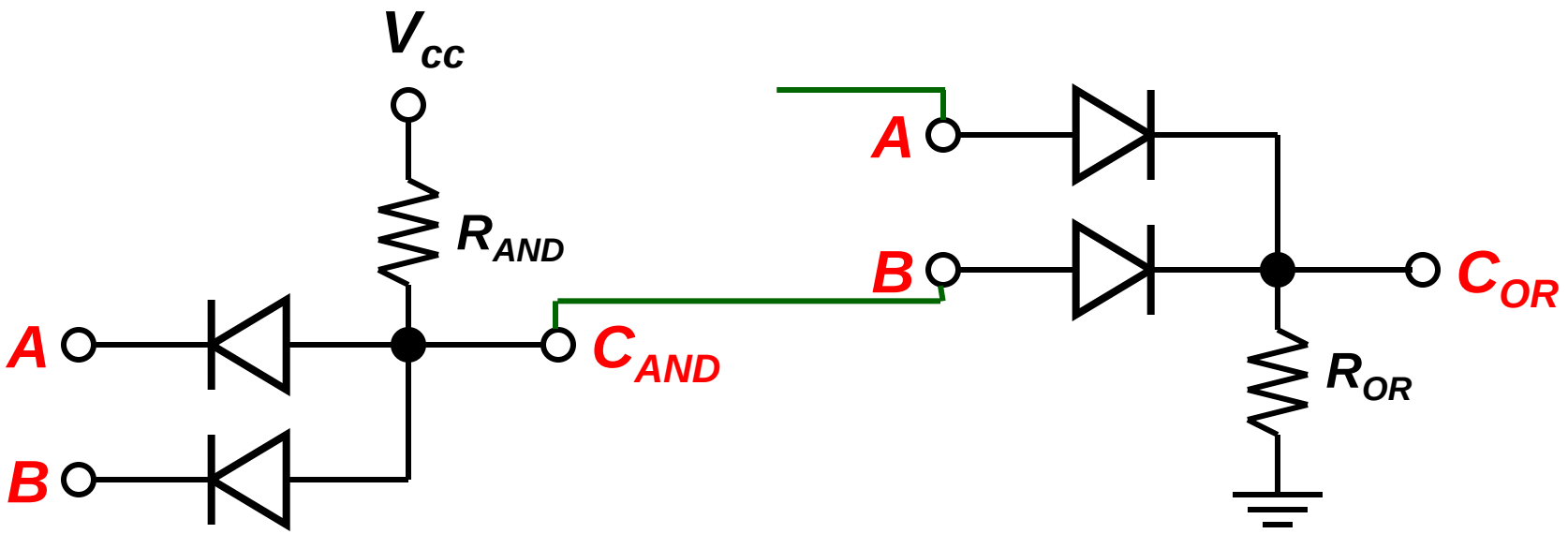
- Diode Only Gates are Basically Incompatible:

AND gate

output voltage is high only if both A and B are high

OR gate

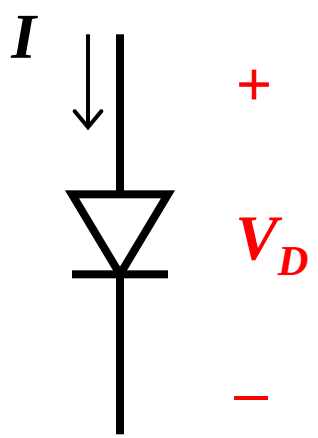
output voltage is high if either (or both) A and B are high



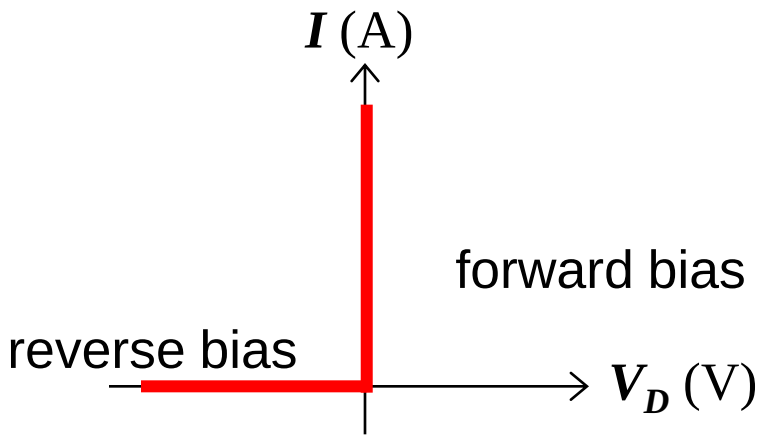
Signal Decays with each stage (Not regenerative)

Switch Model

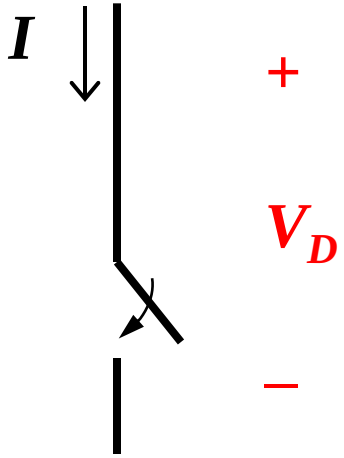
Circuit symbol



***I-V* characteristic**



Switch model



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ON: When $I_D > 0$, $V_D = 0$

OFF: When $V_D < V_{Don}$, $I_D = 0$

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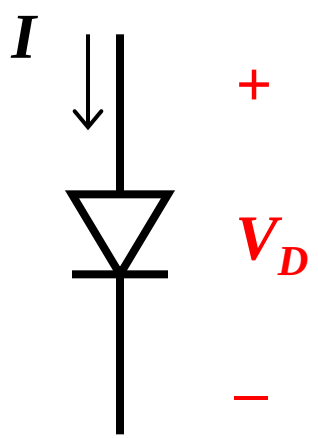
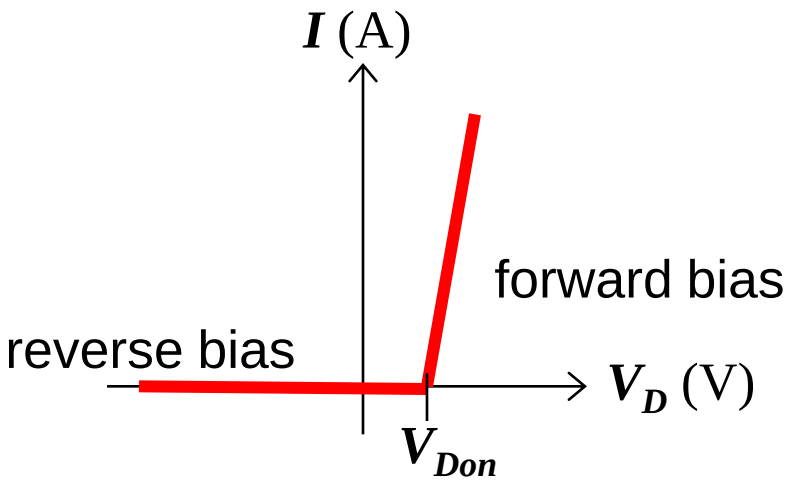
- **open in reverse bias mode**

VSR Model

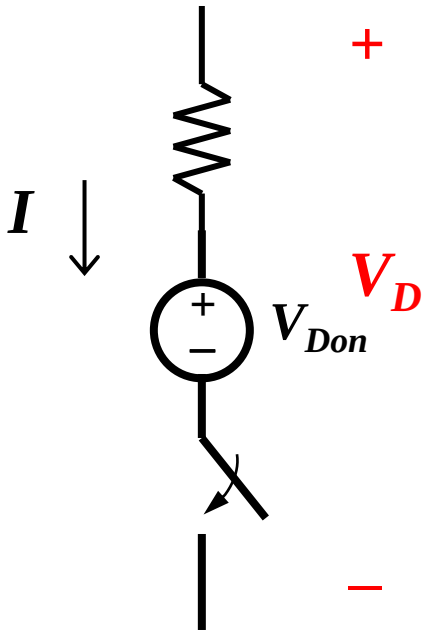
Circuit symbol



***I-V* characteristic**



VSR model



ON: When $V_D \geq V_{D_{on}}$, then $I_D = (V_D - V_{D_{on}})/R_{on}$

OFF: When $V_D < V_{Don}$, $I_D = 0$

Typical $R_{on} = 10\Omega$

Design Problems

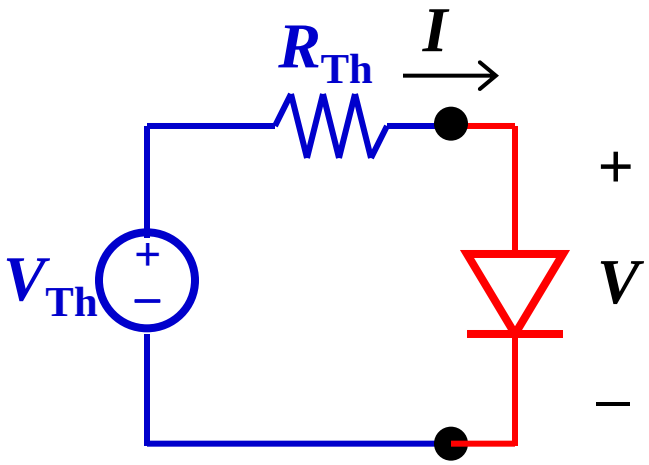
- **ALL WORK MUST BE DONE COMPLETELY SOLO!**
- Maximum allowed time will be **5 hours**
  - Will be written so that it can be completed in approximately 2 hours
- Allowed resources:
  - May use any textbook (incl. Google Books)
  - Anything posted on the EE40 website
  - Only allowed websites are Google Books, wikipedia, and EE40 websites
  - Not allowed to use other websites like facebook answers, yahoo answers, etc. even if you are reading other people's responses
  - When in doubt, email me or text me
  - We will be very serious about cheating on this!

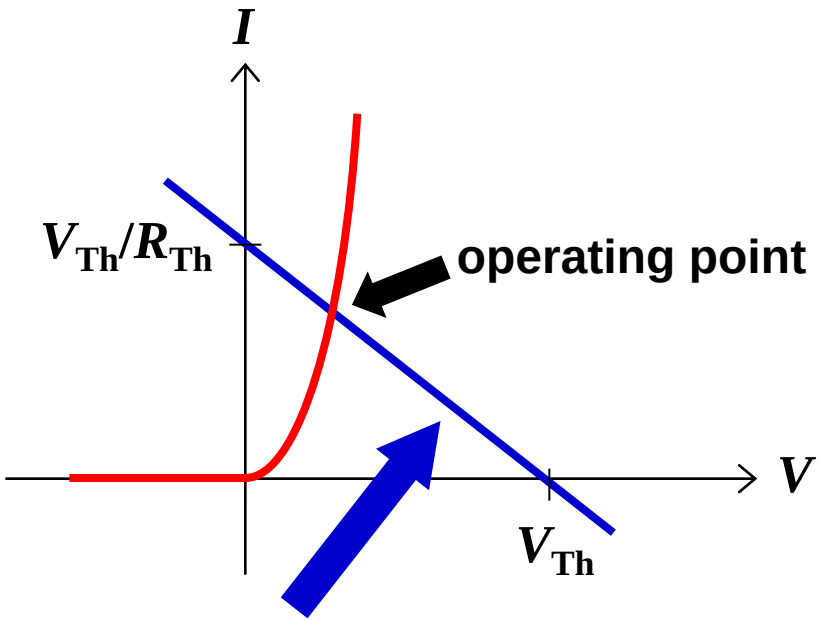
Example Design Problem

- Design a circuit which will sum three sinusoidal input voltages and attenuate any frequencies above 10,000 Hz by at least 20 dB

Example: Diodes in Lab

- What happens if we connect our DC source in the lab to a diode?
  - Will it blow up?



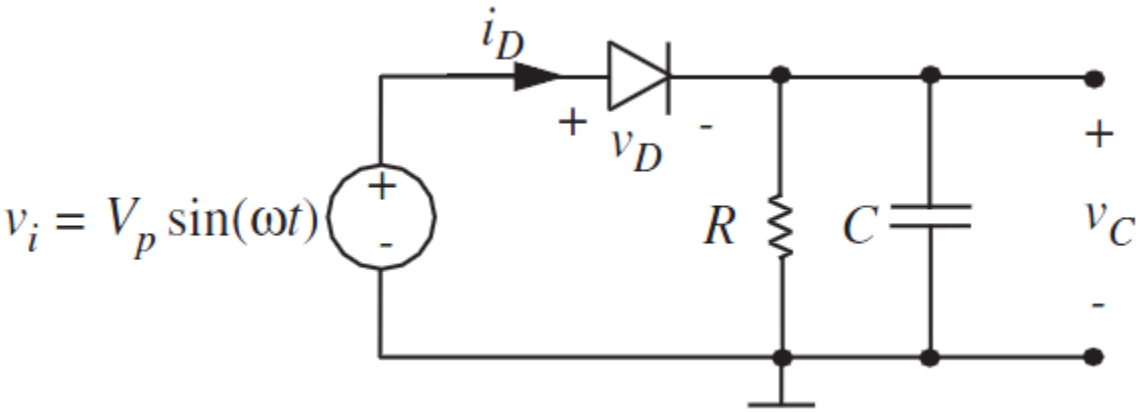


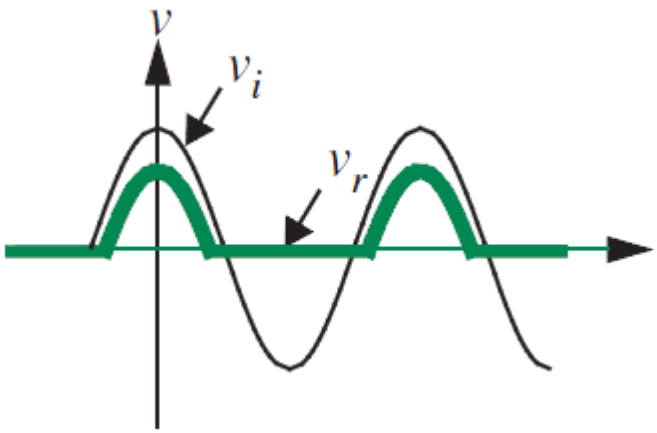
$$\frac{V_{Th} - V}{R_{Th}} = I_O\left(e^{\frac{V}{0.026}} - 1\right)$$

The *I-V* characteristic of all of the circuit except the non-linear element is called the *load line*

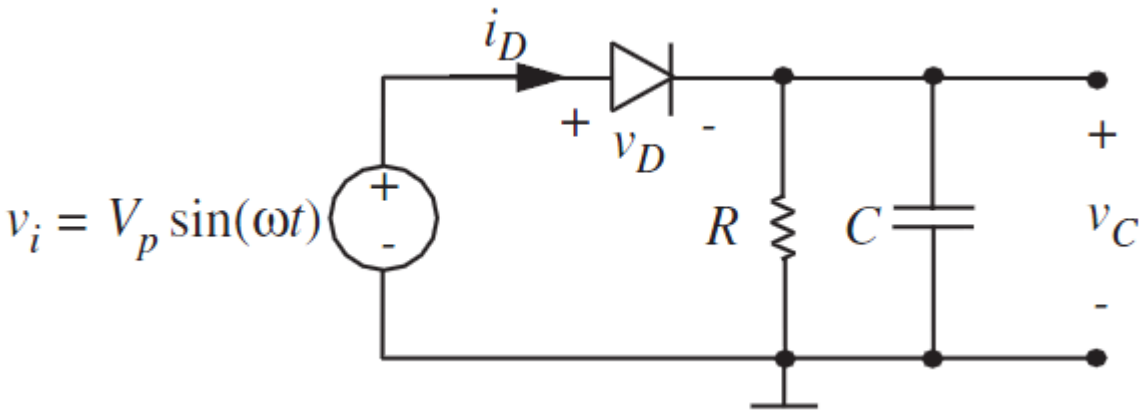
Peak Detection

- Let's go back to our sinusoidal source connected to a diode
- This time, let's add a capacitor in parallel with our output resistor and see what happens





Without Capacitor:



$$i_D = \frac{v_C}{R} + C\frac{dv_C}{dt}$$

$$v_D = v_i - v_C$$

$$i_D = I_s\left(e^{q(v_i - v_C)/kT} - 1\right)$$

$$\frac{dv_C}{dt} = -\frac{v_C}{RC} + \frac{I_s}{C}\left[e^{q(v_i - v_C)/kT} - 1\right]$$