10/11/03 Z = F, OR Gate and Fig Labels

EE 42 Introduction to Digital Electronics

Fall 2003 **Prof. A. R. Neureuther**
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Course Website **www-inst.eecs.Berkeley.edu/~ee42/**

Problem Set # 6

Due:1 PM Wed Oct 15, 2003 in box inside 240 Cory

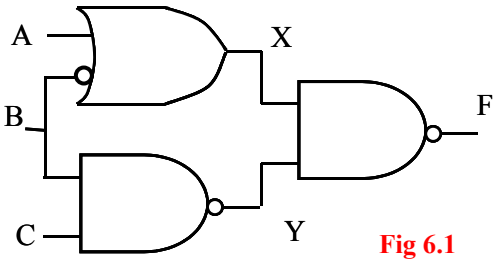

Fig 6.1

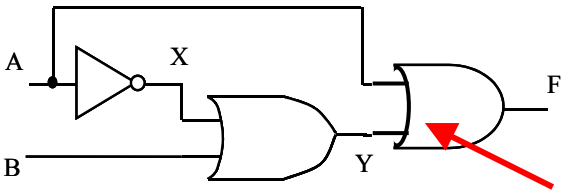

Fig. 6.4

6.1 Logic and Truth Table from Circuit Symbols. Consider the circuit in Fig. P6.1.

a) Write algebraic expressions for the logic functions X and Y.
b) Combine these logic functions to find F.
c) Evaluate the entries in a truth table for X, Y and **F** as computed from A, B and C sequencing through their values.

6.2 Synthesis via Sum of Products. Use a sum of products form to synthesize the truth table you obtained in Problem 6.1.

6.3 Synthesis of your own logic function. Write down a sum of products logic expression of your choice with at least 3 additive product terms. Include the presence of 5 different inputs (A through E)

a) Draw a circuit that realizes your sum of products form in NAND gates.
b) Apply a DeMorgan's law to convert the sum to a product.
c) Apply the other DeMorgan's law to convert the initial products that still appear in b) to sums. (You should now have a product of sums.)
d) Draw a NOR gate only circuit that realizes the product of sums form found in c).

6.4 Timing Diagram. Use the circuit in Fig. P6.4. Note that this is not a good circuit as this circuit could be replaced by a single NAND gate. Assume that B = 0 and A has been 1 for a long time and is then switched to 0 at t = 0. Draw the timing diagram for this circuit for 4 gate delays assuming each gate has an identical delay of 1 ns. (You should observe that this gate 'glitches' in that the output temporarily switches to an incorrect value and then returns to the correct value. This of course wastes energy. Glitching accounts for about 30% of the energy consumed in logic circuits such as cell phones, microprocessors, etc.).