EE 42 – Introduction to Electronics for Computer Science

Fall 2003, **Prof. A. R. Neureuther**
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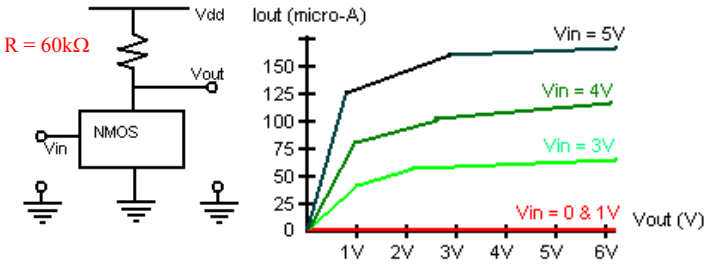
Course Web Site http://www-inst.eecs.berkeley.edu/~ee42/

Problem Set # 8

Due:1 PM Oct 29th, 2003 in box in 240 Cory

8.1 Three Terminal Devices

Assume the device model to the right. Given that the three-terminal device has the given IV characteristic graph for varying input voltage, and assuming that the pull up resistance in the circuit is 60kΩ:



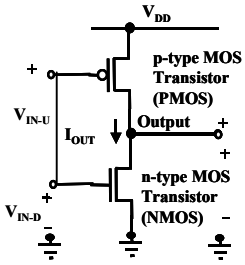
a) Plot the I_{OUT} vs. V_{OUT} graph for the resistor given its voltage on its high side is V_{DD} = 5V.
b) Mark operating I_{OUT} vs V_{OUT} values for VIN = 0, 1, 2, 3, 4, and 5V.
c) Make a rough sketch of the Voltage Transfer Characteristic (V_{OUT} vs. V_{IN}) from your data.

8.2 General Load

Repeat Problem 8.1 with a load resistor of 100kΩ attached from V_{OUT} to a 2.5 V supply. (Hint: First find a Thevenin Equivalent circuit looking out from the device into the rest of the circuit.)

8.3 CMOS

Use the device models at the bottom of the page and assume W/L = 2 and output is open circuit.



a) Draw the I_{OUT} vs. V_{OUT} for the NMOS device assuming a supply voltage V_{DD} of 5V and V_{IN} of 0, 1, 2, 3, 4, and 5V. (Hint: For the NMOS first plot the point at which the device changes from a resistor to a constant current at the saturated level. Then draw the linear and constant lines.)
b) Repeat on the same graph for the PMOS device). (Hint: For the PMOS, switch your thinking to $V_{DD} - V_{IN}$ and $V_{DD} - V_{OUT}$ as the positive voltages and I_{OUT} as the positive downward current. Then repeat the process and label the curves with their values of V_{IN}.)
c) Mark the locations where for each of the six given V_{IN} values the two devices have the same I_{OUT} and V_{OUT}.
d) Sketch the Voltage Transfer Characteristic (V_{OUT} vs. V_{IN}) from your data.

8.4 Sized CMOS Circuits and V_M

a) Use the V_M method to find the voltage of the vertical portion of V_{OUT} vs. V_{IN} curve.
b) Sketch I_{OUT} vs V_{OUT} for NMOS and PMOS device when $V_{IN} = V_M$.
c) Determine the factor by which W/L of the PMOS device must be increased to make V_M = 2.5 V.

V_M comes from setting the two currents equal and constraining $V_{OUT} = V_{IN} = V_M$.

$$I_{OUT-SAT-n} = k_n'\left(\frac{W}{L}\right)_n \left(V_{IN} - V_{Tn}\right)V_{OUT-SAT-n}$$

$$I_{OUT-SAT-p} = k_p'\left(\frac{W}{L}\right)_p \left(V_{DD} - V_{IN} - |V_{Tp}|\right)V_{OUT-SAT-p}$$

	V_T(V)	$V_{OUT-SAT}$ (V)	k' (μA/V²)
NMOS	0.43	0.63	100
PMOS	0.4	1	25

$k_U = k'_P\,(W/L)_P$

$k_D = k'_n\,(W/L)_n$