

Problem Set 9 Solutions

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Problem 1: Delay in Transistor Circuits

- a) For a transition from high to low voltage, where $V_{DD} = 5V$, determine the delay in the system.

From lecture, the formula for delay is $\Delta t = 0.69RC$, where the R is whatever equivalent resistance exists in your closed circuit undergoing a transition, and C is the capacitance on the output.

For a high to low transition, $V(0) = V_{DD}$, and the top switch is open, the bottom is closed (discharging capacitor).

Thus, $\Delta t = 0.69(10k\Omega)(20fF) = 1.38 \times 10^{-10} s = 0.138 ns$

(NOTE: $k = 10^3$, and $f = 10^{-15}$)

- b) For a transition from low to high voltage, determine the delay.

In this case, the upper switch is closed, and the lower switch is open.

Thus, $\Delta t = 0.69(20k\Omega)(20fF) = 2.76 \times 10^{-10} s = 0.276 ns$

- c) What could you do to improve worst case delay by a factor of 2?

Basically, there are two variables that you can control in the system.

You could either take the capacitor and exchange it for a new capacitor with half the capacitance, which would improve both delays by a factor of 2.

You could also take the $20k\Omega$ resistor, because it is involved in the path with the worse delay, and exchange it with a $10k\Omega$ resistor.

9.2 More Delay, and Delay Compensation

- a) Determine the truth table for the circuit. What kind of logic gate is this?

For this problem, the key to the solution is to just try inputting all four possible combinations of input (A & B), and determining which switches are closed.

If the closed switches yield a circuit excluding V_{DD} , then the output is low. If the closed circuit includes V_{DD} , then the output is high.

The following truth table will result:

A	B	F
0	0	1
1	1	0
1	0	1
0	1	1

This kind of gate is recognizable as NAND.

- b) Given that all resistors are $10k\Omega$, determine the worst case delay from low to high voltage, assuming the pull-up and pull-down networks never “pull” at the same time.

For this problem, you have to look at all the possible ways that you can generate a low to high transition. It can happen 3 ways: 1) The switch on pull-up controlled by A is closed, 2) the switch on pull-up controlled by B is closed, 3) both switches on pull-up are closed.

In case 1 & 2, the resistance in your RC circuit is $10k\Omega$. Case 3 has 2 $10k\Omega$ resistors in parallel, yielding an equivalent R lower than $10k\Omega$.

Thus, the worst case delay is $\Delta t = 0.69(10k\Omega)(20fF) = 0.138 ns$.

- c) Determine the worst case delay from high to low voltage.
 For this circuit, there is only one possible transition from high to low—when both switches on pull-down are closed. The equivalent resistance of this path is $2 \times 10\text{k}\Omega = 20\text{k}\Omega$, so $\Delta t = 0.69(20\text{k}\Omega)(20\text{fF}) = 0.276\text{ ns}$.
- d) What could you do to equalize the worst case delays? (Hint: adjust the W/L to adjust the resistance)
 For this problem, you need the equivalent resistance for worst case low-to-high transitions to be the same as the equivalent resistance for the high-to-low transitions. This can be accomplished either by changing the resistors on pull-down to be half their original value (make them $5\text{k}\Omega$) or changing the resistors on pull-up to twice their original value (make them $20\text{k}\Omega$).
 This can be done during fabrication of the circuit by changing the W/L ratios of the pull-up resistors/transistors to make them half their original values, or changing the W/L ratios of the pull-down resistors/transistors to make them twice their original values.

9.3 Review on Op-Amps

**The current through the top op-amp's feedback path will be called I_{F1} and the bottom op-amp's feedback current will be called I_{F2} .

The first step in this problem is the application of ideal op-amp assumptions. These assumptions include the following:

The input terminals have no voltage difference across them.

The current into the op-amp at the input terminals is 0.

The output gain is infinite.

Another additional assumption will be used to simplify the work: the rails on the op-amp can accommodate the output voltages.

Using these assumptions, several observations can be made.

First, the voltage at the negative terminals of both op-amps must be 0V because the positive terminals are grounded.

Second, because both negative terminals are effectively grounded, current through R_2 is going to be 0A, because there is no potential difference across the resistor.

This simplifies the top part of the circuit greatly, because there *is no* feedback current, meaning that output voltage is 0V.

For the bottom op-amp, the voltage across R_1 must equal V_{IN} , so the current through the path on the bottom is $I = V_{IN}/R_1$.

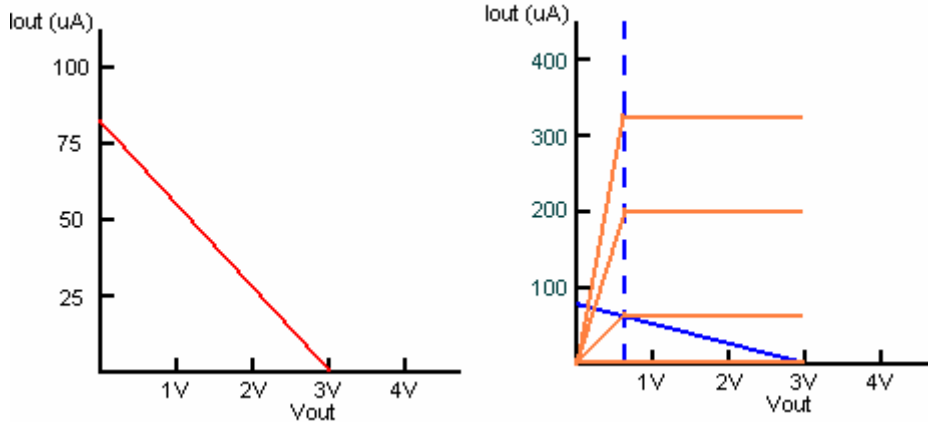
By KCL, since there is no current allowed into the terminals of the op-amp, the current into the feedback path is also $I = V_{IN}/R_1$.

By Ohm's Law, this gives a drop of $V_{R5} = R_5 V_{IN}/R_1$ across the feedback resistor for the lower op-amp. This means $V_{OUT2} = -(R_5/R_1)V_{IN}$.

9.4 Review on Three Terminal Devices

- a) Plot the I_{OUT} vs. V_{OUT} graph for the circuit external to the NMOS.

In order to plot the I_{OUT} vs. V_{OUT} graph, you need to find the Thevenin equivalent of the rest of the circuit. Leaving the NMOS transistor out, this Thevenin equivalent looks like a V_{DD} source with a $60k\Omega$ resistor in series with a $30\mu A$ current source. Taking open circuit voltage, this voltage must be $V_{DD} + 60k\Omega \cdot 30\mu A = 4.8V$. The Thevenin resistance can be found by turning all sources off, so the voltage source becomes a short and the current source becomes an open circuit. This results in a Thevenin resistance of $60k\Omega$, giving the **following graph on the left**:



b) Determine the NMOS current and voltage when $V_{IN} = 0, 1, 2$, and $3V$.

This problem basically involves using the NMOS equations with the device parameters and the specified input voltages.

For $V_{IN} = 0V$, $I_{OUT-SAT-n} = (100\mu A/V^2)(2)(0V - 0.43V)(0.63V)$.

You'll notice that at $0V$, the threshold has not been passed. The resulting current should be $0A$.

For $V_{IN} = 1V$, $I_{OUT-SAT-n} = (100\mu A/V^2)(2)(1V - 0.43V)(0.63V) = 71.82\mu A$

For $V_{IN} = 2V$, $I_{OUT-SAT-n} = (100\mu A/V^2)(2)(2V - 0.43V)(0.63V) = 197.82\mu A$

For $V_{IN} = 3V$, $I_{OUT-SAT-n} = (100\mu A/V^2)(2)(3V - 0.43V)(0.63V) = 323.82\mu A$

The plot on the right above results.

For $0V$ input, the MOSFET voltage is $3V$. Current is $0\mu A$

For $1V$ input, the MOSFET voltage is $\sim 0.63V$. Current is $\sim 70\mu A$

For $2V$ input, the MOSFET voltage is $\sim 0.2V$. Current is $\sim 77\mu A$

For $3V$ input, the MOSFET voltage is $\sim 0.15V$. Current is $\sim 78\mu A$

c) Sketch a rough plot of V_{OUT} vs. V_{IN} from your data in b).

This problem specifically uses load-line analysis to determine the operating points of the entire circuit given certain input voltages. You can plot the output voltages at the intersections versus the input voltages to get the following plot:

