# UNIVERSITY OF CALIFORNIA, BERKELEY <br> College of Engineering 

 Department of Electrical Engineering and Computer SciencesLast modified on December 3, 2003 by Isaac Seetho (i_seetho@uclink.berkeley.edu)
Prof. Neureuther

## Homework 12 Solutions

### 12.1 Diode Model Comparison

Gallium arsenide diodes are pn-junctions that use a different substrate material, resulting in different diode characteristics. Suppose for this problem only that all diodes carry a large signal voltage of 1.4 V , and have a saturation current $\mathrm{Io}=10^{-25}$.
a) Given the provided gallium arsenide diode circuit to the right, draw a sketch of the IV characteristic of the diode using the exponential equation provided in lecture.
Then, use load line analysis to determine the operating point of the circuit.
The IV characteristic of the diode is given by the equation $I=I_{0}\left(\mathrm{e}^{\mathrm{v} / \mathrm{vth}}-1\right)$. For the circuit's IV characteristic, take the circuit and find its Thevenin equivalent. The equivalent open circuit voltage is given by a voltage divider across the 4 k resistor, resulting in:
$\mathrm{V}_{\mathrm{Th}}=(4 /(4+1))^{*} 3 \mathrm{~V}=2.4 \mathrm{~V}, \mathrm{R}=(1 \mathrm{k} \| 4 \mathrm{k})=800 \Omega, \mathrm{I}=2.4 \mathrm{~V} / 800 \Omega=3 \mathrm{~mA}$


Looking at the diagram, a voltage and current of $(1.3 \mathrm{~V}, 1.35 \mathrm{~mA})$ can be determined.
b) Repeat the above exercise, this time using the large signal model of the diode.


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The results from either model are nearly identical $\rightarrow$ the large signal model is a good approximation.

### 12.2 Usage of Diodes in Circuits

Use the circuit provided to the right. Assume the provided diode is silicon.
a) Assuming that the diode in the circuit acts as a perfect rectifier, and that the input voltage source generates a square wave with a frequency of 1 kH , a high voltage of 100 mV and a low voltage of 0 , draw a sketch of the voltage on the output resistor over a 10 ms interval.

b) Repeat part (a), using the large signal diode model.

c) What kind of circuit is this? What kinds of applications could it be used for?

The ability to follow a rising input voltage closely and the slow discharge of the capacitor when the diode is reverse biased make this circuit a useful envelope detector.
12.3 IC Resistors, MOS as Voltage Controlled Resistors
a) Suppose a silicon resistor with a Group III dopant concentration of $10^{16} \mathrm{~cm}^{-3}$. If the resistor is sized at $9 \mu \mathrm{~m}$ length, $3 \mu \mathrm{~m}$ width and $1 \mu \mathrm{~m}$ thickness, what is the resistance? (Be sure to use the mobility values provided in lecture). Determine also the sheet resistance of this resistor.
$\mathrm{R}=1 /(\mu \mathrm{nq})(\mathrm{L} / \mathrm{Wt})=1 /\left[\left(500 \mathrm{~cm}^{2} / \mathrm{Vs}\right)\left(10^{16} \mathrm{~cm}^{-3}\right)\left(1.602 \times 10^{-19} \mathrm{C}\right)\right]^{*} 9 \times 10^{-4} \mathrm{~cm} /\left[\left(3 \times 10^{-4} \mathrm{~cm}\right)\left(1 \times 10^{-4} \mathrm{~cm}\right)\right]$
$=37.45 \mathrm{k} \Omega$
The sheet resistance is $R=R(W / L)$
b) Suppose you have a MOS transistor or capacitor where the oxide thickness is 70 nm . Using the notion that capacitance is Cox $=\varepsilon \mathrm{A} / \mathrm{d}$, where A represents cross-sectional area and d represents thickness, and determine the capacitance across the gate of the transistor (determine capacitance of the oxide) per unit area.
$\mathrm{C}=\varepsilon / \mathrm{t}=(3.9)\left(8.85 \times 10^{-14} \mathrm{~F} / \mathrm{cm}\right) /\left(70 \times 10^{-7} \mathrm{~cm}\right)=4.93 \times 10^{-8} \mathrm{~F} / \mathrm{cm}^{2}$
c) It is often the case that when the transistor is biased at an operating voltage, the equation $\mathrm{Q}=\left(\mathrm{V}-\mathrm{V}_{\mathrm{T}}\right)$ C for some range of input voltages V , given a threshold $\mathrm{V}_{\mathrm{T}}=0.43 \mathrm{~V}$ and total gate capacitance C . If the transistor gate has a 360 nm width and a 180 nm length, what is the total charge in the channel of the transistor?
$\mathrm{Q}=(2.5 \mathrm{~V}-0.43 \mathrm{~V})\left(4.93 \times 10^{-8} \mathrm{~F} / \mathrm{cm}^{2}\right)\left(360 \times 10^{-7} \mathrm{~cm}\right)\left(180 \times 10^{-7} \mathrm{~cm}\right)=6.61 \times 10^{-17} \mathrm{C}$
d) Use this amount of mobile charge and the fact that mobility is the standard set of numbers from lecture, and calculate the resistance of the MOSFET. Determine how resistance would vary from NMOS to PMOS.
$\mathrm{R}=1 /(\mathrm{Q} \mu)(\mathrm{L} / \mathrm{W})$
Using this equation,
$\begin{array}{ll}\mathrm{R}_{\text {NMOS }}=1 /\left[\left(6.61 \times 10^{-17} \mathrm{C}\right)\left(500 \mathrm{~cm}^{2} / \mathrm{Vs}\right)\right](180 \mathrm{~nm} / 360 \mathrm{~nm}) \\ \mathrm{R}_{\mathrm{PMOS}}=1 /\left[\left(6.61 \times 10^{-17} \mathrm{C}\right)\left(150 \mathrm{~cm}^{2} / \mathrm{Vs}\right)\right](180 \mathrm{~nm} / 360 \mathrm{~nm}) & =1.51 \times 10^{13} \Omega \\ =5.04 \times 10^{13} \Omega\end{array}$
e) If this were NMOS, what would be the size ratio of an equivalent resistance PMOS?

An equivalent resistance PMOS would have a (L/W) ratio that was ( $10 / 3$ ) ( $\mathrm{L}_{\text {NMOS }} / \mathrm{W}_{\text {NMOS }}$ )
In other words, the W/L value for an equivalent resistance PMOS at this dopant concentration would be 0.3 times the value for an NMOS.

