University of California
Department of Electrical Engineering
and Computer Science

Prof. J. S. Smith
Fall 2004
EECS42

Final Exam

December 18, 2004

NAME: SOLUTION
Last, First

Student ID:_____

TA name:_____

Signature:_____

- CLOSED BOOK, CLOSED NOTES except one sheet (both sides) of notes is allowed
- Calculators are allowed.
- Do not unstaple the exam.
- Show all of your work and reasoning to receive full or partial credit.
- Ask questions only if you think the problem is unclear, or there is an error in the statement of the problem.

Problem	Possible points	Score
1	20	
2	20	
3	20	
4	20	
5	20	
Total	100	

PROBLEM (1)

Consider the following circuits, and answer the questions.

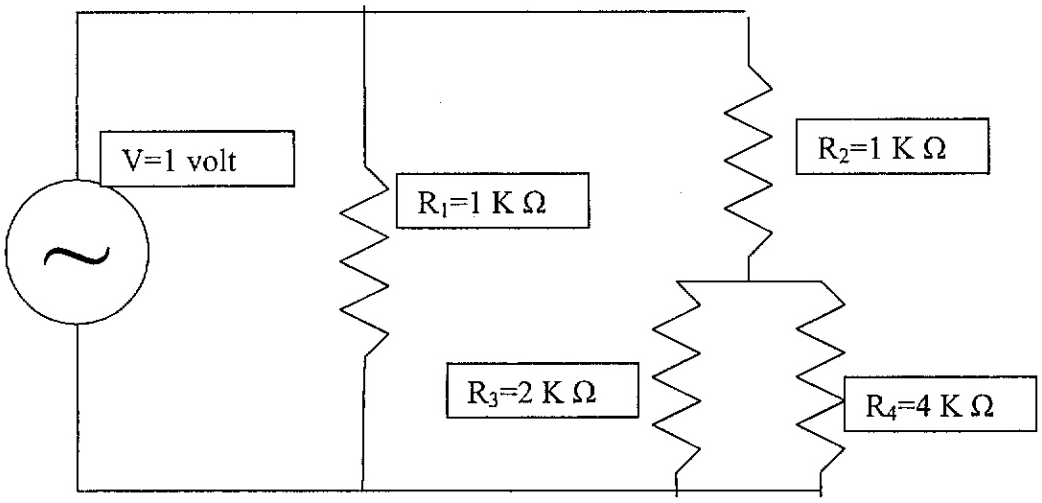


Figure 1

1a) (2 points) In the circuit of figure 1, what is the current through R_1? I_{R1}= 1 mA

$1V / 1k$

1b) (2 points) In the circuit of figure 1, what is the current through R_2? I_{R2}= 3/7 mA .4285

$\frac{1V}{(1k+2k\|4k)} = \frac{3}{7}$ mA

1c) (2 points) In the circuit of figure 1, what is the current through R_3? I_{R3}= 2/7 mA .2856

$I_{R3} = I_{R2} \cdot \left(\frac{4k}{6k}\right)$

1d) (2 points) In the circuit of figure 1, what is the current through R_4? I_{R4}= 1/7 mA .1428

$I_{R4} = I_{R2} \cdot \left(\frac{2k}{6k}\right)$

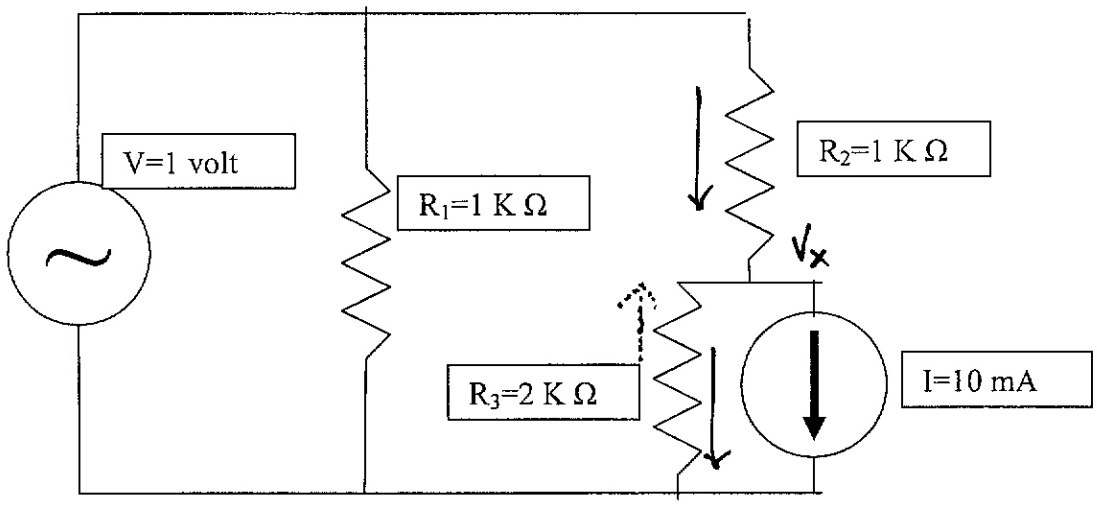


Figure 2

$$10mA + \frac{V_x}{2k} = \frac{1 - V_x}{1k} \quad \Rightarrow \quad V_x = -6V$$

$$20 + V_x = 2 - 2V_x$$

1e) (3 points) In the circuit of figure 2, what is the current through R_1? I_{R1}= 1mA

1f) (3 points) In the circuit of figure 2, what is the current through R_2? I_{R2}= 7mA

$$I_{R_2} = \frac{1 - (-6)}{1k} = 7mA$$

1g) (3 points) In the circuit of figure 2, what is the current through R_3? I_{R3}= -3mA

$$I_{R_3} = \frac{-6}{2k} = -3mA$$

1h) (3 points) In the circuit of figure 2, what is the power supplied by the current source?

P= 60mW

$$10mA \cdot -6V = 60mW$$

PROBLEM (2)

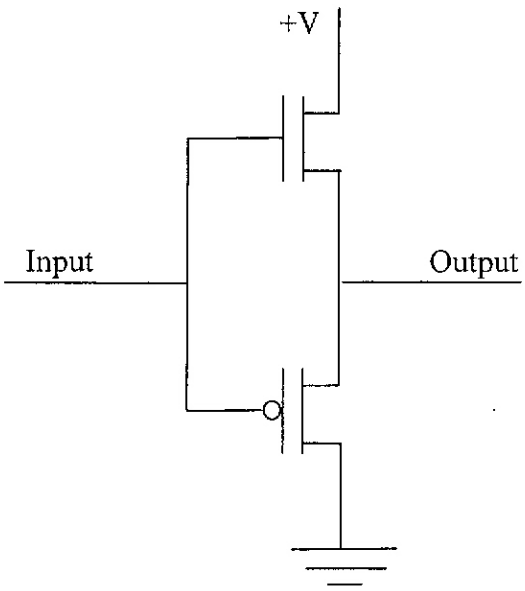


Figure 3

2a) (3 points) The circuit shown in figure 3 is not an inverter. Explain why.

Pmos & Nmos are switched.

2b) (3 points) Does the circuit in figure 3 perform some digital function? If not explain why not, if it does, explain what it does.

Lossy identity function (buffer)

2c) (5 points) If the input is 1 volt, and +V is 1 volt, what is the output voltage, given the transistor characteristics shown in the following figures (figures 4 and 5) for a 2 micron wide PMOS device and a 1 micron wide NMOS device?

$V_{output} = V_{DD} - V_T = .8\ V \pm 0.1V$

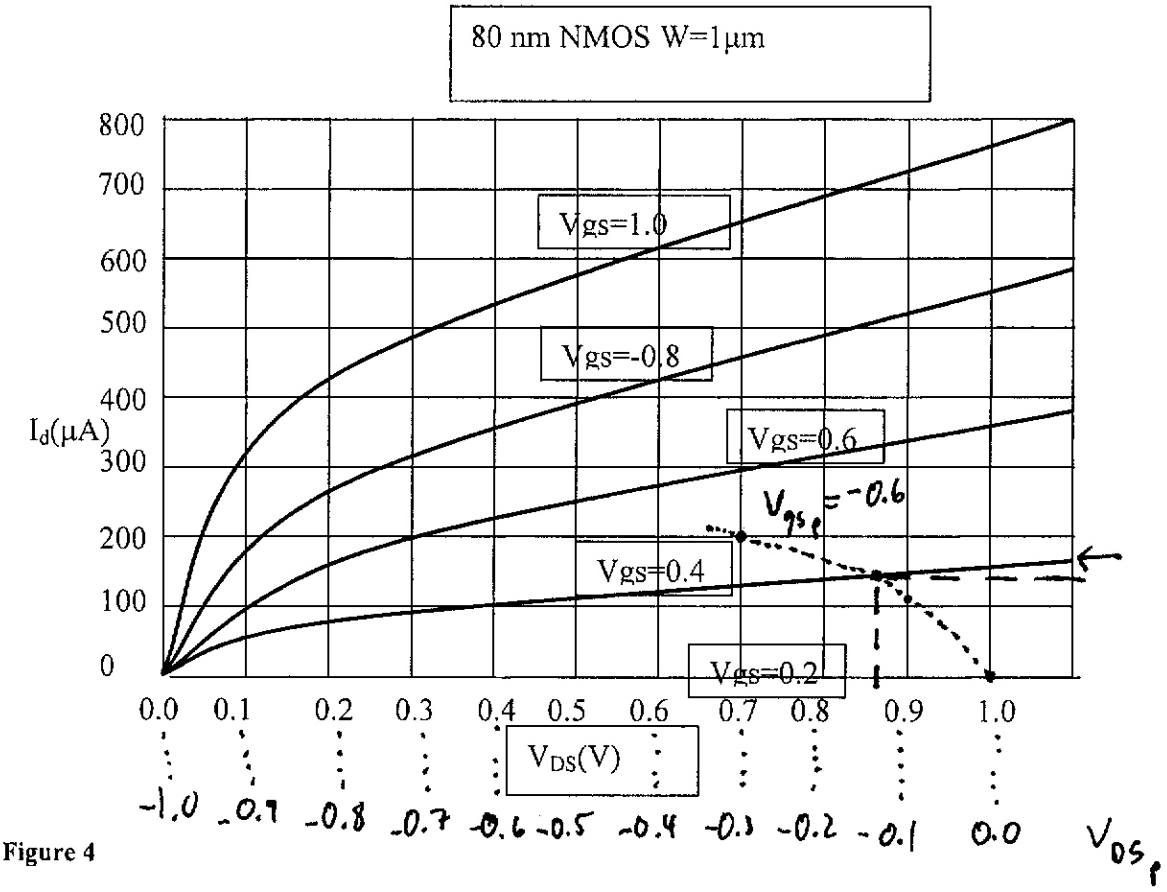


Figure 4

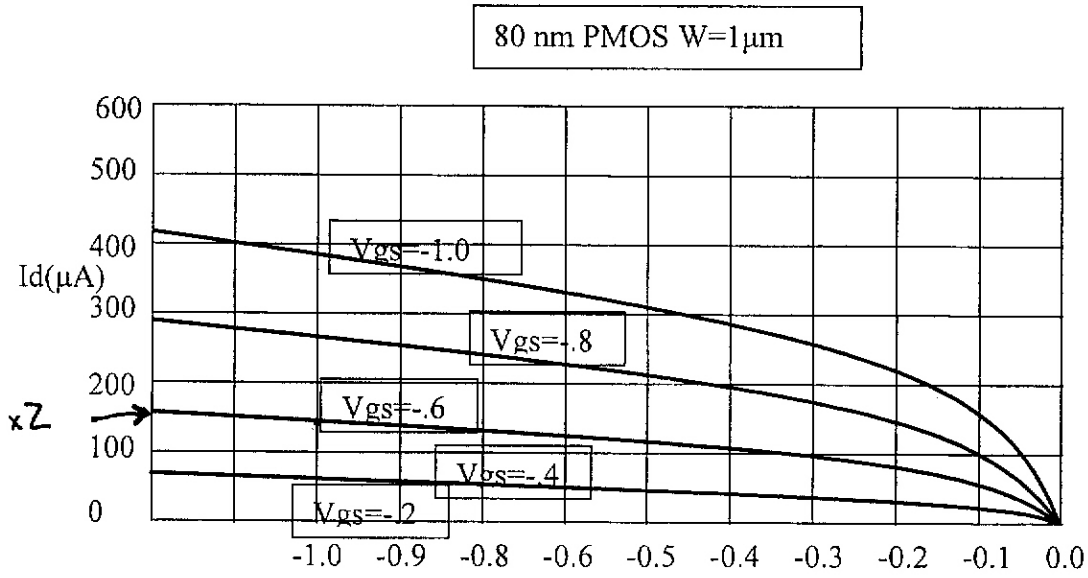


Figure 5

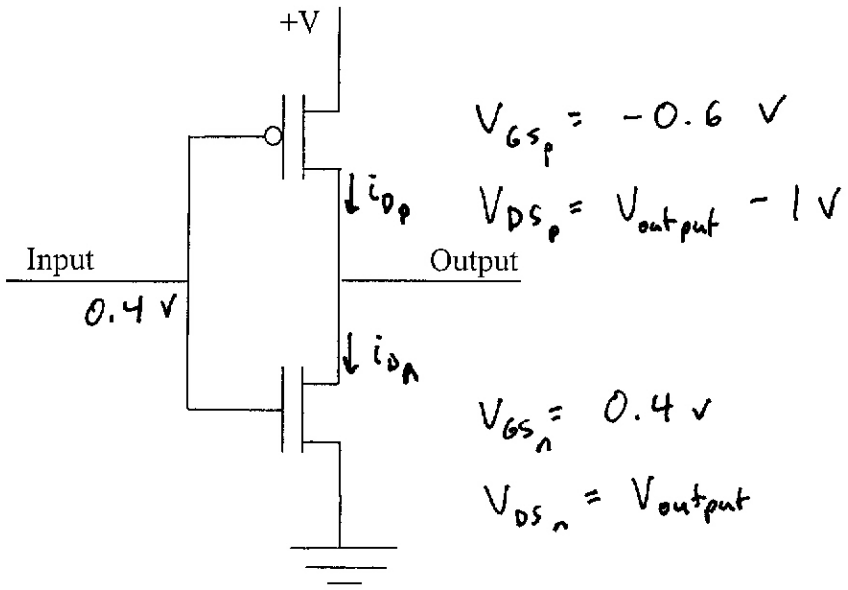


Figure 6

2d) (3 points) If the input to the inverter shown in figure 6 is 0.4 volt, and +V is 1 volt, what is the approximate output voltage, given the transistor characteristics shown in figure 4 and 5 for a 2 micron wide PMOS device and a 1 micron wide NMOS device?

$V_{DS_p} = V_{DS_n} - 1$ (see graphs on previous page)

$V_{output} = 0.86 \pm 0.04$

2e) (6 points) Approximately what current will flow in from +V to ground when the input is at .4 volts as in part (2d)

$i_{D_p} = i_{D_n} = 138.2\ \mu A$

(~140 is acceptible...)

~150

~130

Problem (3)

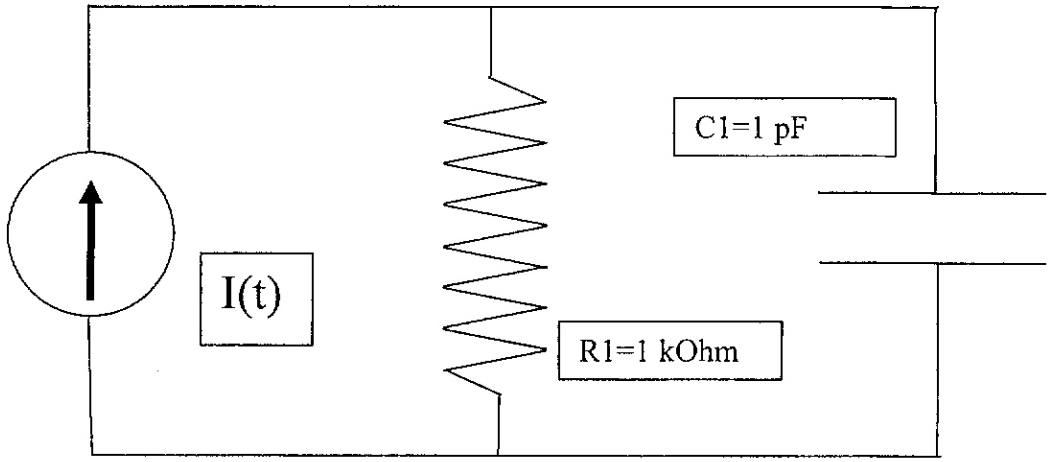
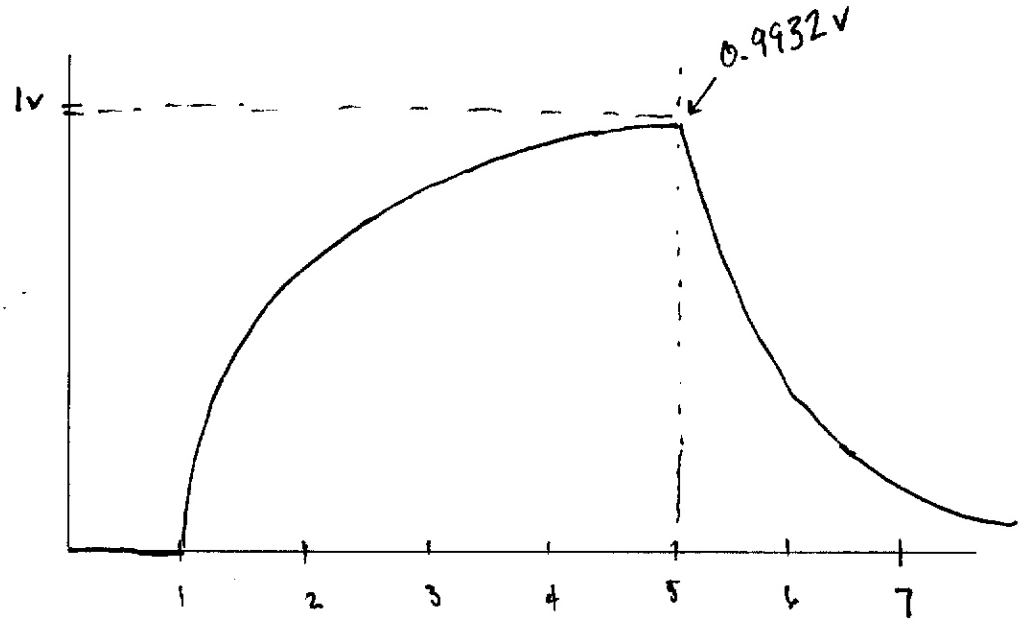


Figure 7

3a) (10 points)In the circuit in figure 7, the current source shown is off until time t=1 ns, and at t=1 ns it is turned on to 1 milliamp. At time t=5 ns the current is turned off. Show a sketch of the voltage across the capacitor as a function of time, indicating the voltages (pico=10^{-12}, nano=10^{-9})



3b) (10 points) The circuit shown in figure 8 includes a black box with the IV curve in the figure 9. Find the voltage which will appear across the black box, and the current which will flow through the black box

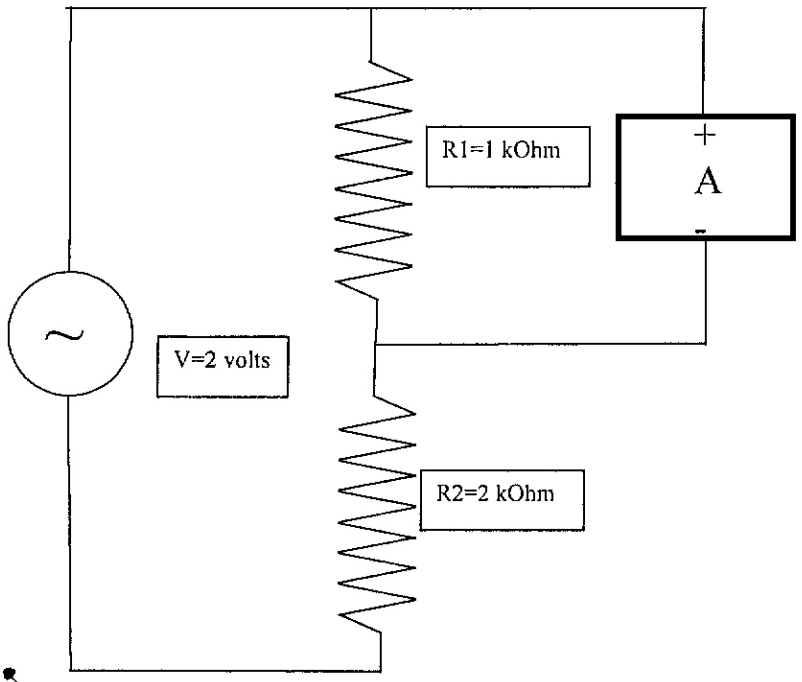
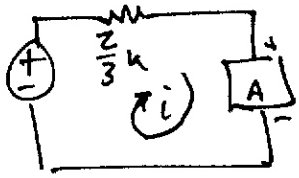


Figure 8

Convert to Thevenin:



(5 points)
Voltage=
0.46V

(5 points)
Current=
~300μA

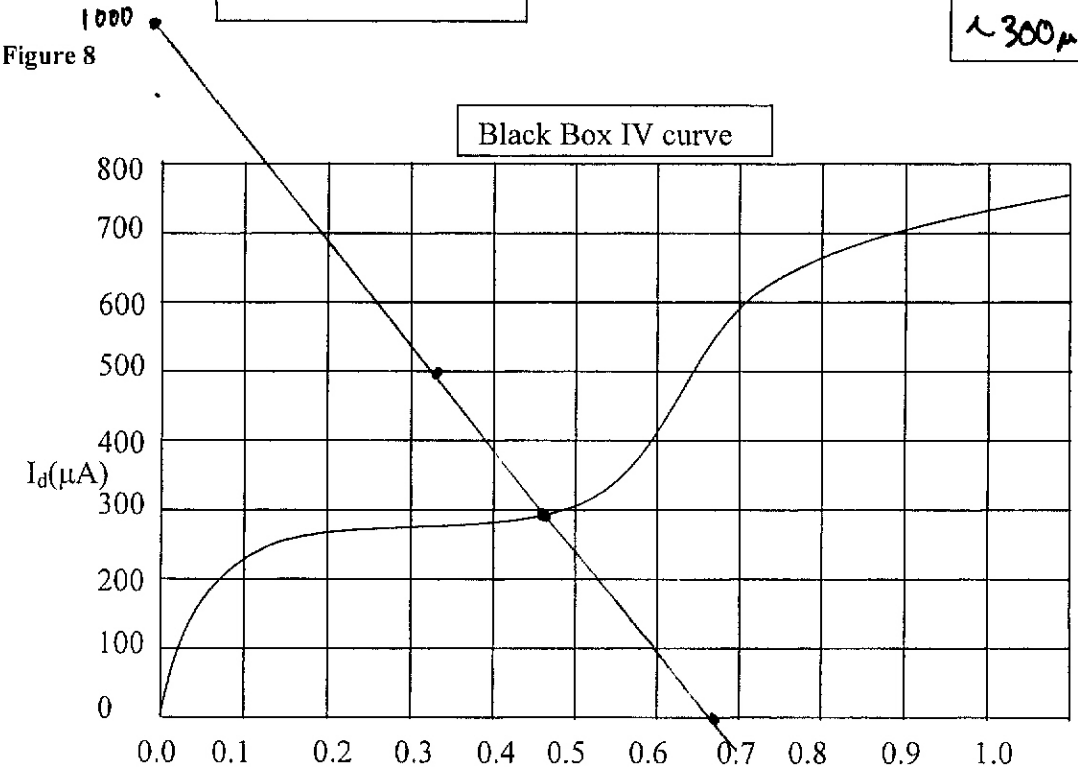


Figure 9

Problem (4)

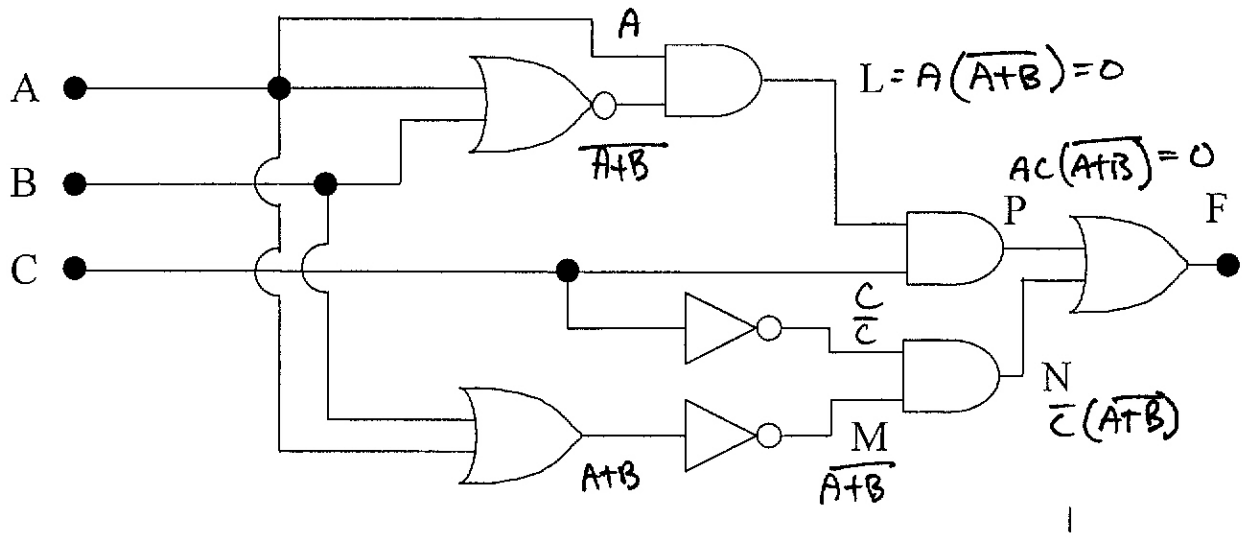


Figure 10

4a) (3 points) For the circuit in figure 10, find F as a Boolean function of the inputs A B and C.

$$F = \overline{C}(\overline{A+B}) + AC(\overline{A+B})$$
$$= \overline{A}\,\overline{B}\,\overline{C}$$

4b) (3 points) Draw a truth table for the circuit in figure 10.

A	B	C				F
0	0	0				1
0	0	1				0
0	1	0				0
0	1	1				0
1	0	0				0
1	0	1				0
1	1	0				0
1	1	1				0

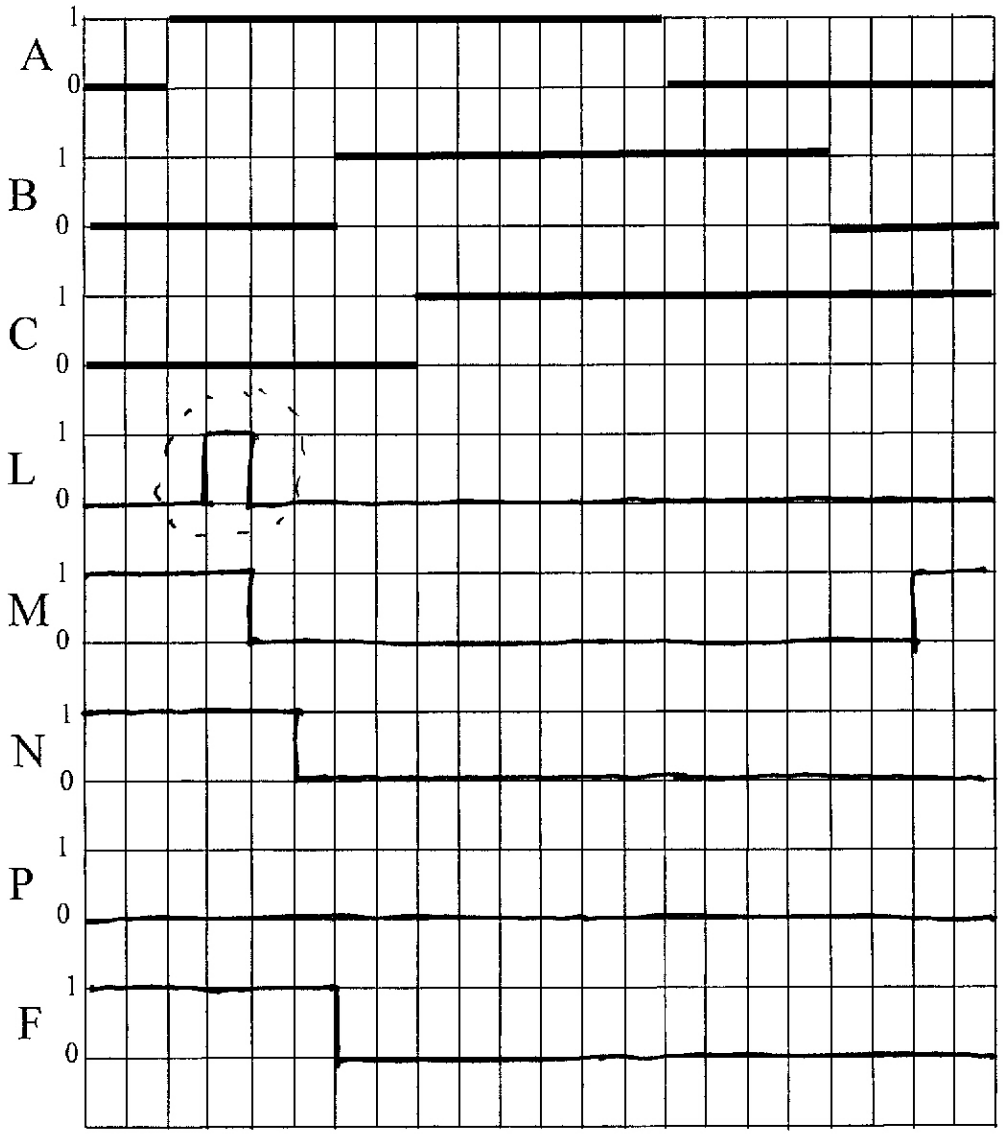
-2 for not having F close

-1 for close F

4c) (3 points) For the circuit of figure 10, express F as a function of A, B, and C, as a sum of products.

$$F = \overline{A}\,\overline{B}\,\overline{C}$$

4d) (3 points) Draw a timing diagram for the circuit of figure 10 Each grid line is 1 gate delay. Point out any glitches that you find.

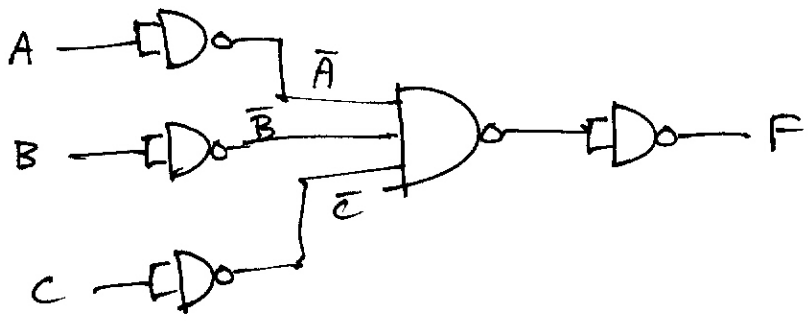


1pt for have correct waveforms but F

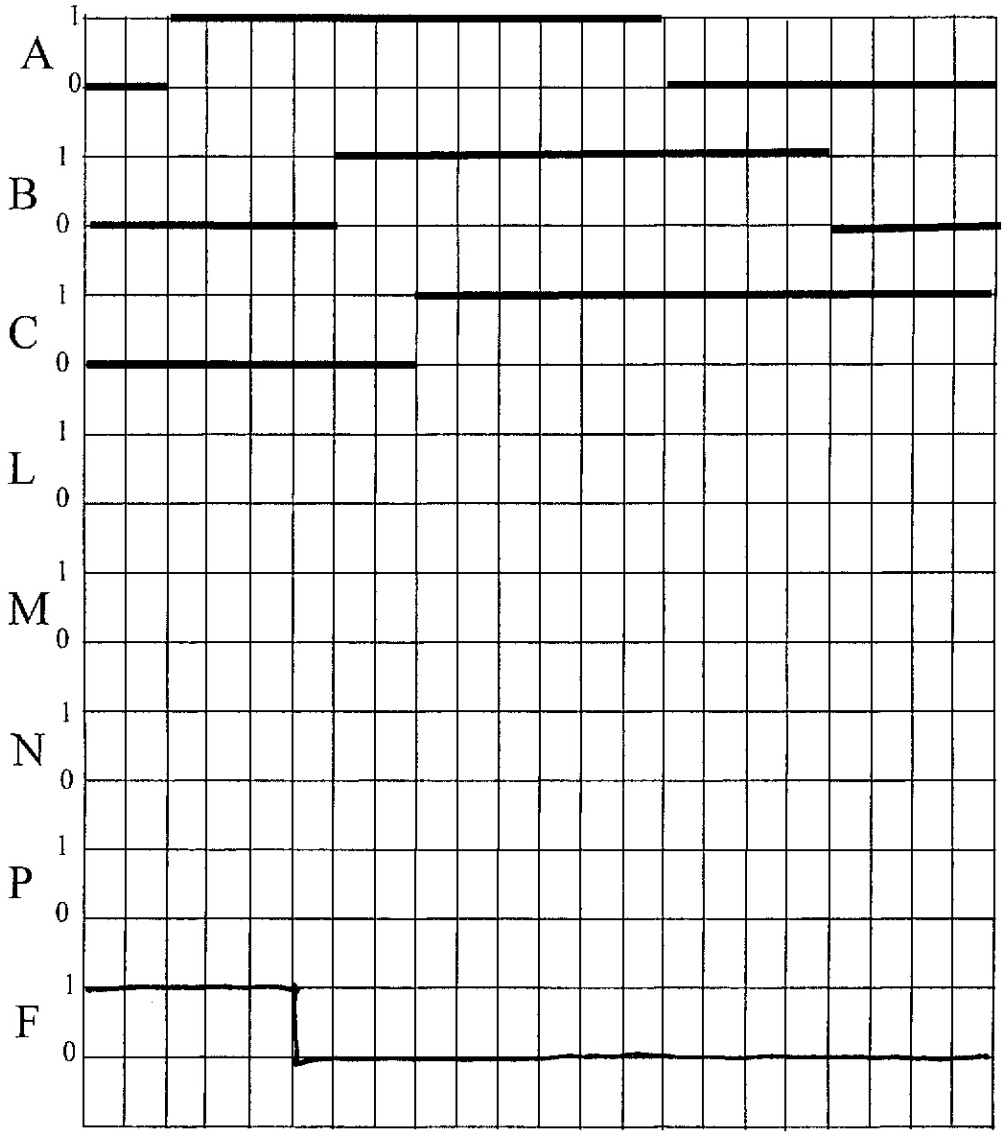
1pt for glitch

1pt for F

4e) (3 points) Implement the function F of A, B, and C (from problem part 4c) using a circuit with NAND gates only.



4f) (5 points) Fill in the timing diagram for the circuit of 4e. Point out differences between the timing diagram for the circuit you designed in 4e, and the timing diagram of 4d from the original circuit



2 pts for F

2 pts for differences.

5a) (3 points) Explain what a latch is, what a flip-flop is, and explain the difference.

Memory elements which store a value depending on a clock (i.e. sequential). A Latch is level sensitive while a flip-flop is edge sensitive.

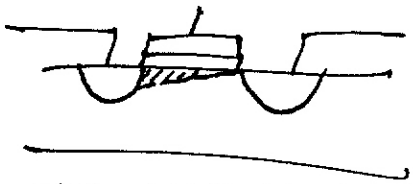
5b) (3 points) In a CMOS circuit, if you double the width of all the transistors, that increases the amount of current that they can drive. Will that make the logic run faster? Explain why or why not the logic is proportionally faster if the transistors are made wider.

On average the speed will not change because doubling the width decreases the resistance but increases the capacitance.

5c) (3 points) In long cables between devices which are used for high bit rate communications, there almost always a resistor to ground in parallel with the input to a CMOS device, called a "terminator". Why is this resistor there? If it was removed, would the signal seen by the input decrease? What other effects would removing this resistor have?

The resistor is there to manage transmission-line effects (i.e. reflections). If it were removed the signal would double (inf. gate input). Reflected wave would travel back down the wire towards the source.

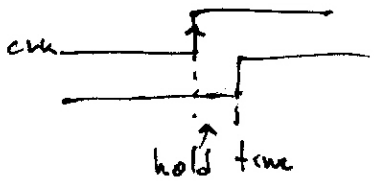
5d) (3 points) In a MOS transistor, for a particular value of the gate to source voltage, if the source to drain voltage is increased the current increases. At first the increase is proportional to the voltages, but then as the voltage is increased further the increase of current is slower. (The IV curves flatten out) Explain why this happens.



This happens because in saturation the inversion layer under the gate "pinches off"

5f) (3 points) Explain what a hold time is for a flip-flop. What might happen if the hold time is violated?

The hold time is the time to hold the input constant after the triggering edge.



IF its violated, then the output may be an unknown value.

5g) (3 points) A transmission line can not be split along its length to go to two or more inputs, it must be either run point to point, or be configured as a bus with close connections to the devices along its length. Explain why you can not simply go to multiple destinations with separate wires with branching connections.

There would be reflections at the branching point.

5h) (2 points) Explain what a ground plane is, and why it is commonly used for high speed digital circuits. What is the alternative, if any, to having a ground plane?

The ground plane is a metal layer in the PCB to give return path for metal traces. Alternate: have current return traces.