LECTURE 25/26

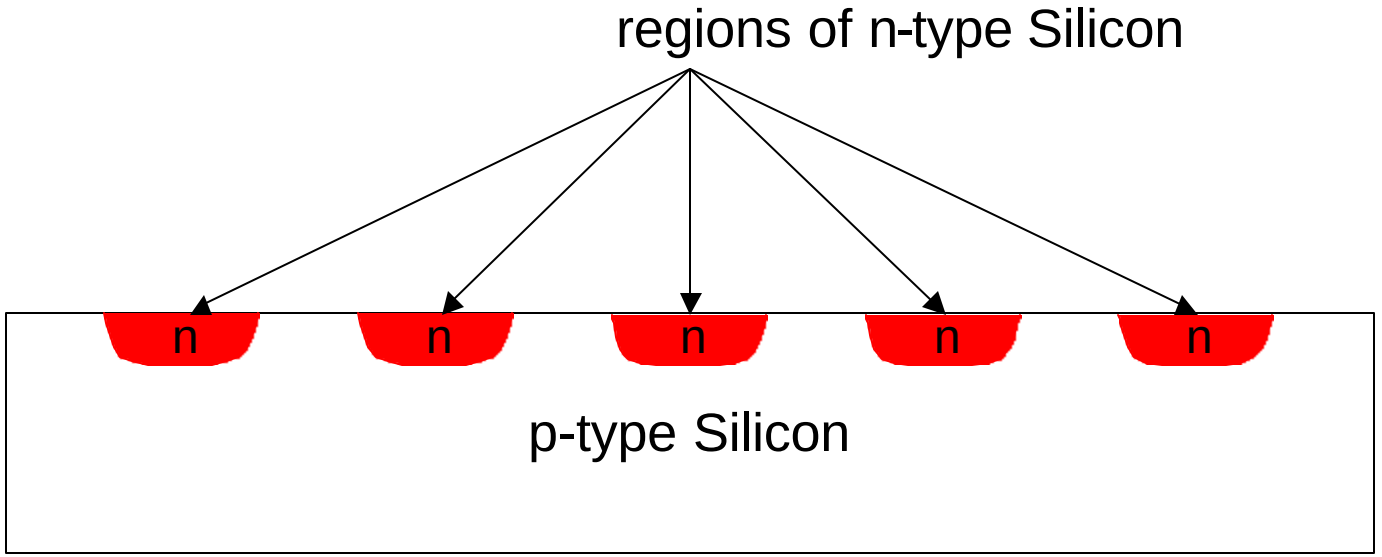
Lecture 24 Review:

- Diode Structure and I vs V
- Diode Circuits

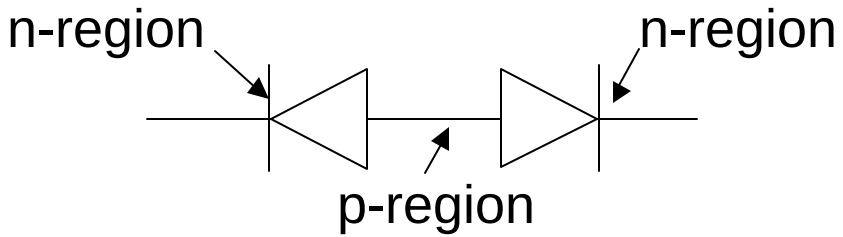
Today:

- NMOS Structure (diode isolation)
- NMOS “Controlled resistors”
- Current Saturation
- Complete NMOS I vs V characteristics

WHY DIODES ARE IMPORTANT IN INTEGRATED CIRCUITS --- ISOLATION



No current flows if voltages are applied between N-type regions because two P-N junctions are “back to back”

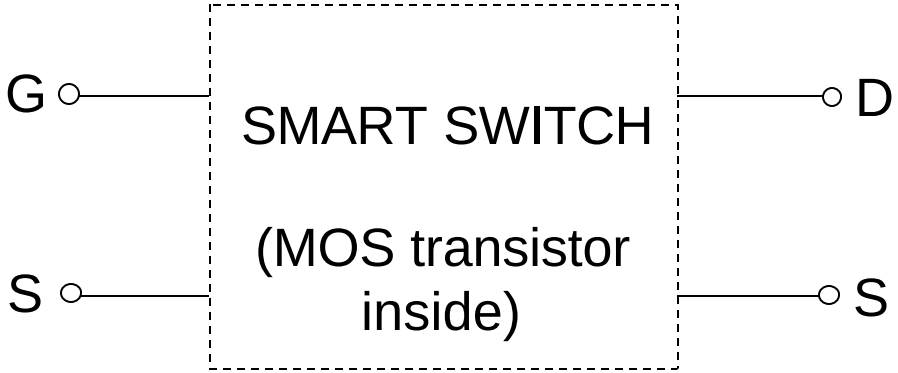


Thus, diodes **isolate** n-regions in p-type substrate and vice versa.

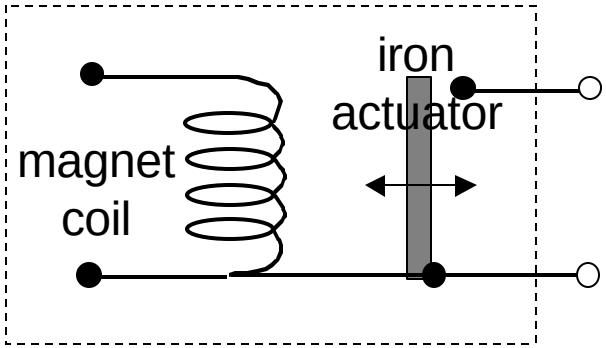
BACK TO THE BEGINNING

We began this section with the goal of coming up with the “smart switch” – a device we can control with a voltage that operates like a switch – open circuit or short circuit.

The “smart switch” is realized in MOS transistors – they control the current flow between their “source” and “drain” according to the voltage we apply to their “gate.” The basis for this is the field effect.



voltage applied to gate (V_{GS}) controls current between drain and source

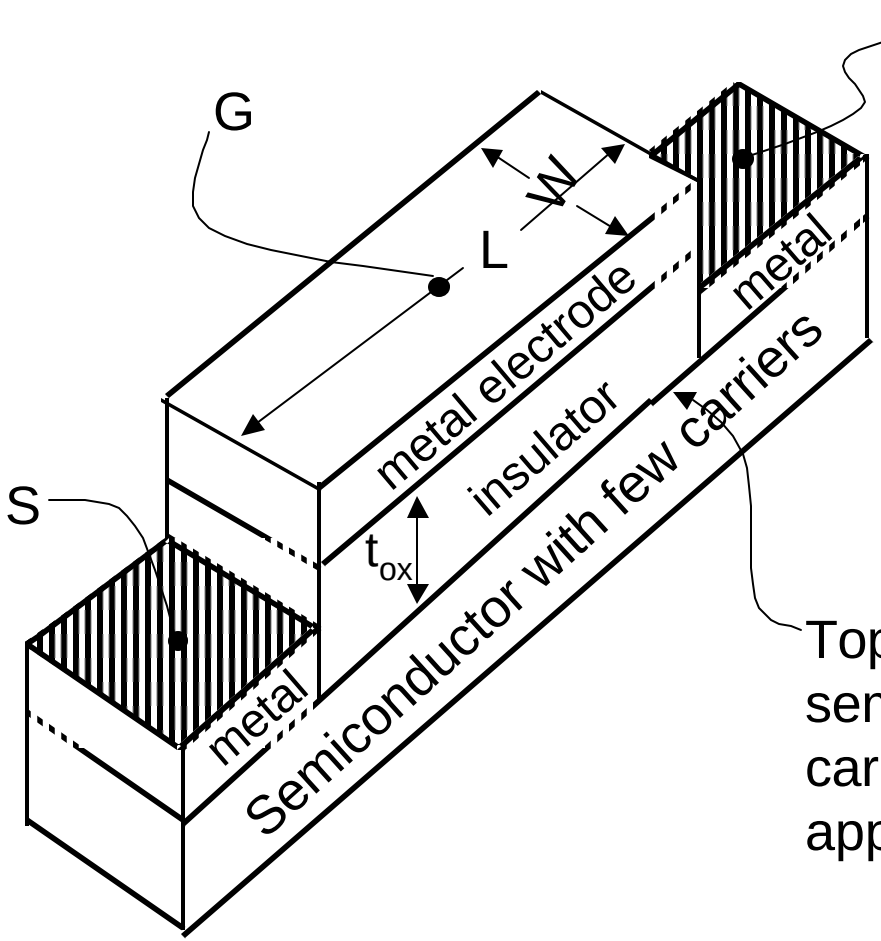


like a “relay” (but better)

THE "CHARGE CONTROL DEVICE" OR HOW TO MAKE A SMART SWITCH

Concept:

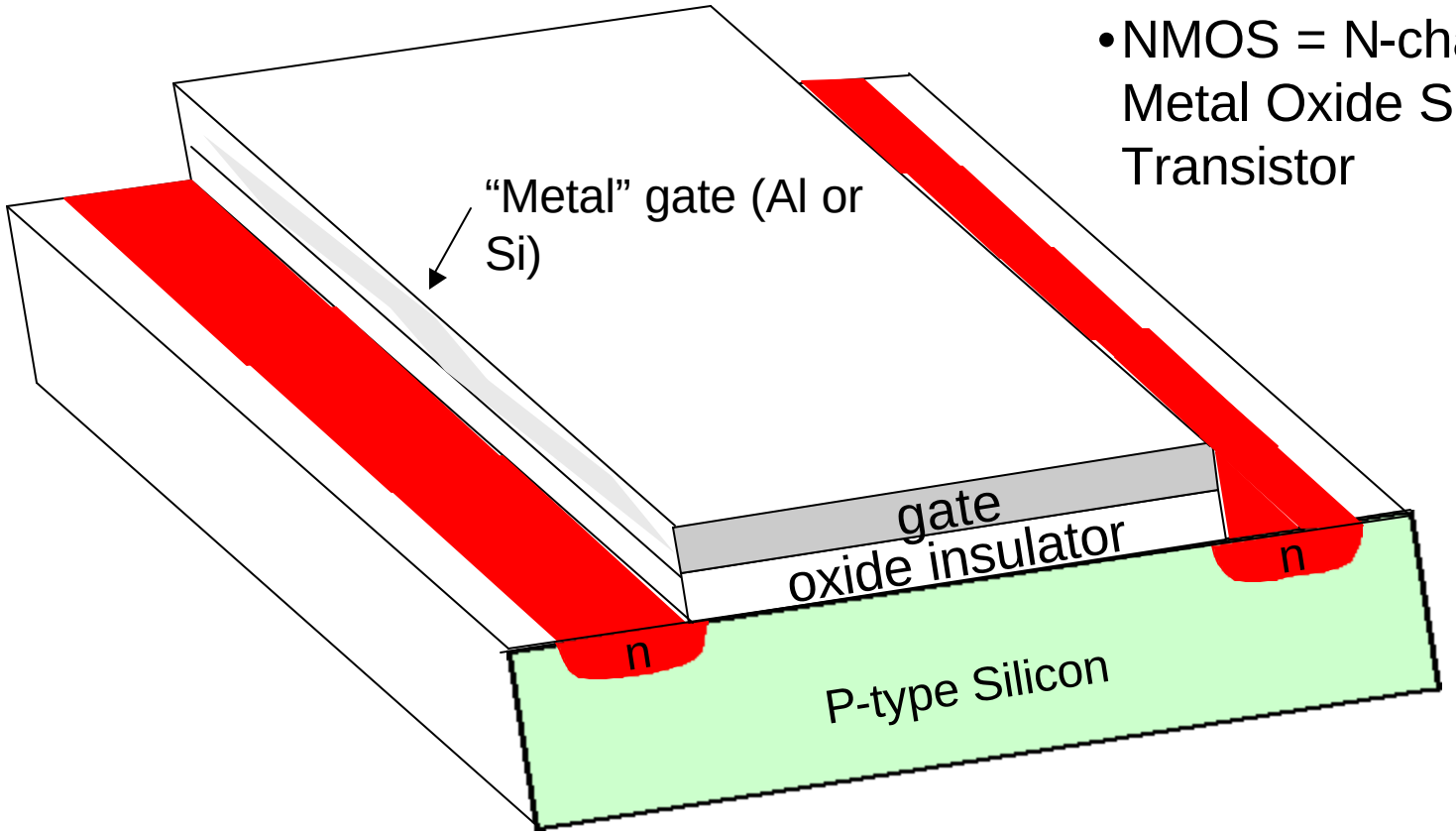
Apply positive voltage to gate with respect to semiconductor. This will induce +Q on gate, –Q on surface of semiconductor. Resistance between D and S will drop.



Top surface of semiconductor can have carriers induced by applying voltage to G

Thus, we can control current from D to S.

NMOS TRANSISTOR STRUCTURE

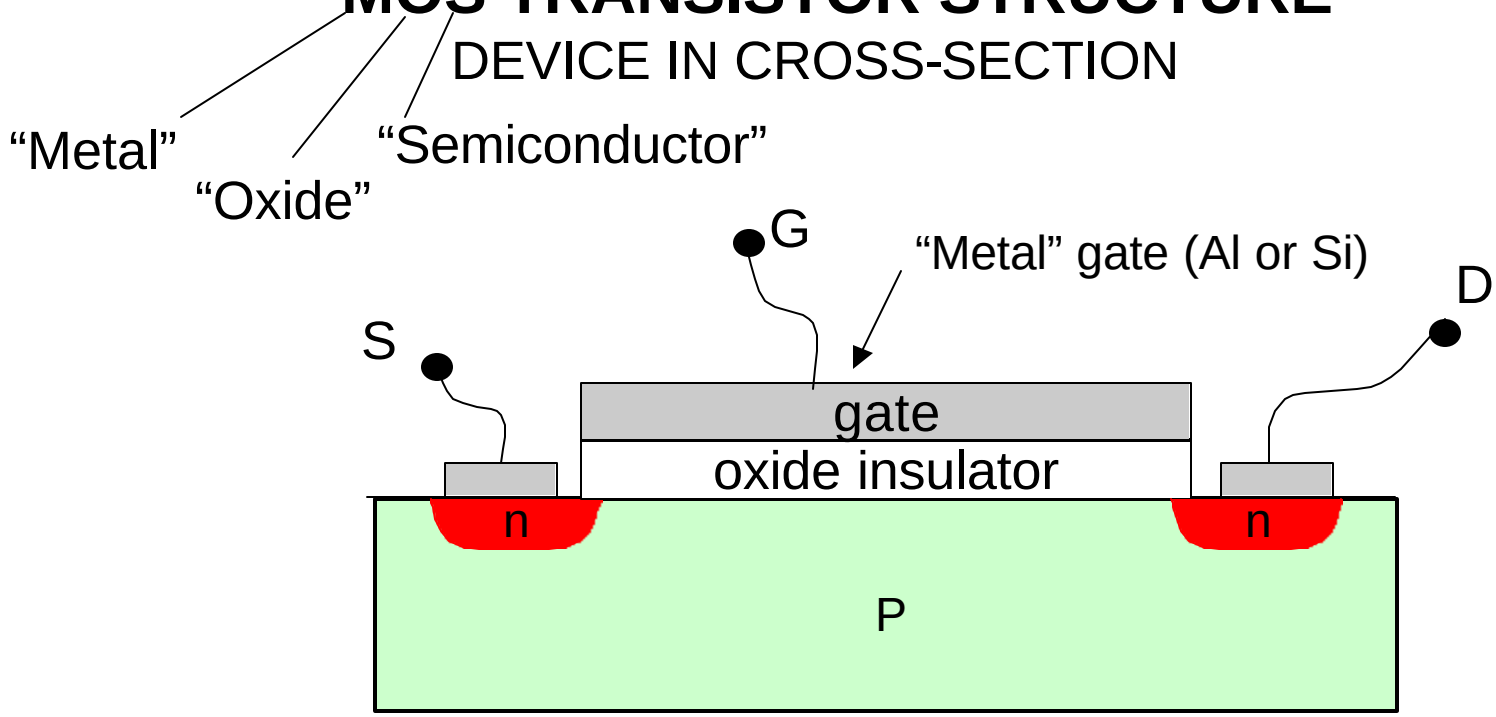


- NMOS = N-channel Metal Oxide Silicon Transistor

- An insulated gate is placed above the silicon
- Its purpose is to control the current between n-type regions (by inducing a "channel" of electrons when a positive V is applied).

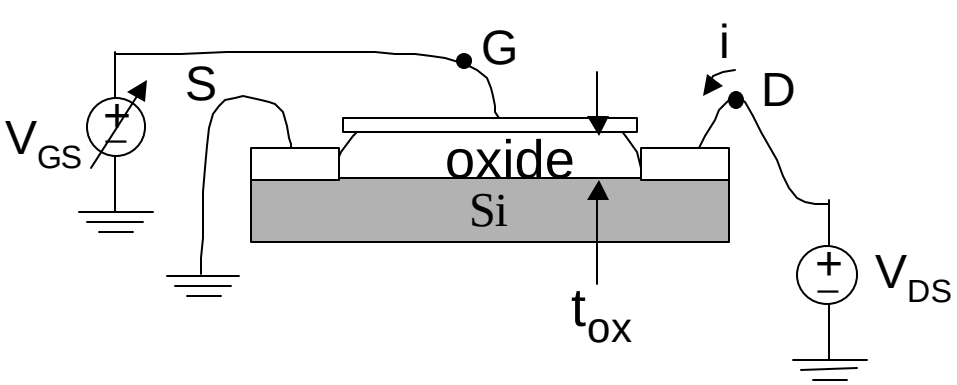
MOS TRANSISTOR STRUCTURE

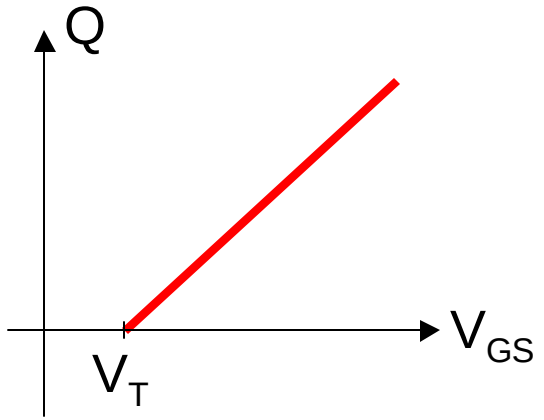
DEVICE IN CROSS-SECTION



- In the absence of gate voltage, no current can flow between S and D.
- Above a certain gate to source voltage V_t (the "threshold"), electrons are induced at the surface beneath the oxide. (Think of it as a capacitor.)
- These electrons can carry current between S and D if a voltage is applied.

CHARGE-CONTROL EXPERIMENT – "THE FIELD EFFECT"





Above some "threshold" voltage V_T, the number of electrons per square cm under the gate is proportional to $\mathbf{v_{GS}} - V_T$, i.e., the charge Q_N is proportional to $\mathbf{v_{GS}} - V_T$.

$$Q_N = C_{ox}(V_{GS} - V_T)$$

charge for unit area

capacitance for unit area

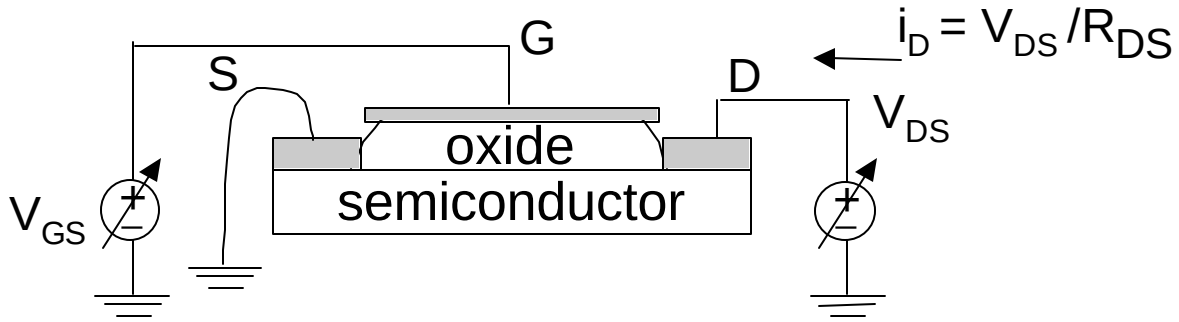
onset of charge formation by field effect

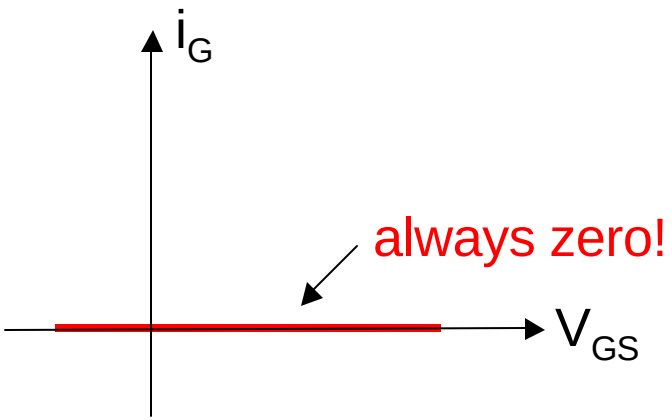
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

These charge carriers can carry current from D to S, so we can make low resistance (R_{DS}) by making $\mathbf{v_{GS}} - V_T$ very large

I-V CHARACTERISTICS IN THE LOW V_{DS} REGIME

Consider first gate current and drain current versus GATE voltage

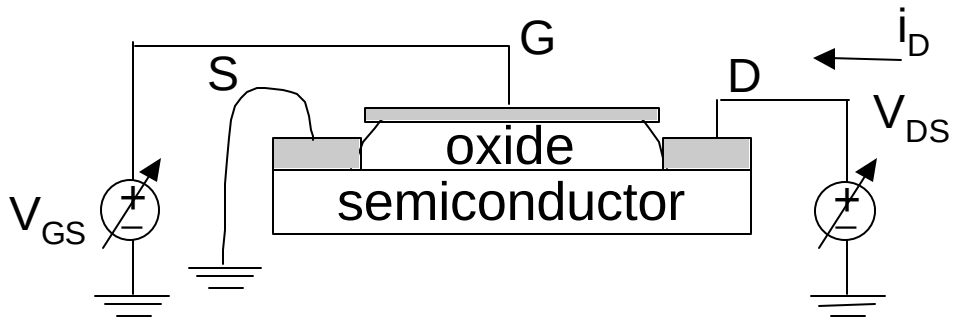


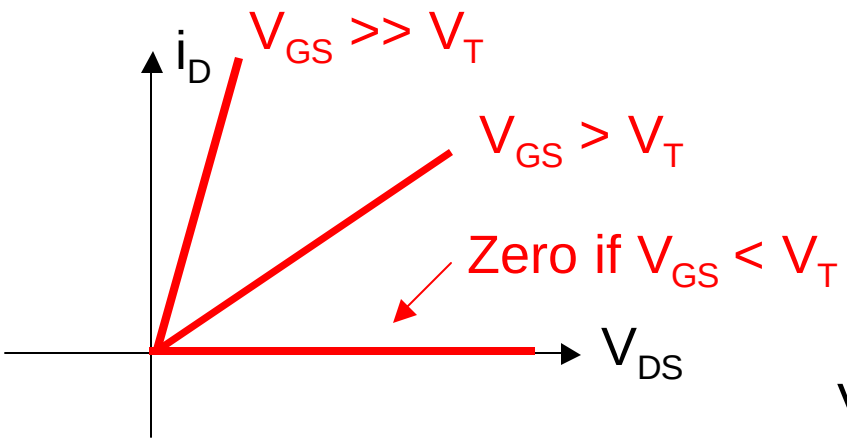


The gate is insulated, so there can never be any gate current.

I-V CHARACTERISTICS IN THE LOW V_{DS} REGIME

Consider I_{DS}, the current from D to S :





Below "threshold" no charge, so no conduction. ($V_{GS} < V_T$)

Above threshold ($V_{GS} > V_T$), Q appears so drain to source conduction is possible

Very low resistance (R_{DS}) for increasing gate voltage ($V_{GS} >> V_T$)

We have a controlled switch !

MOSFET Terminology

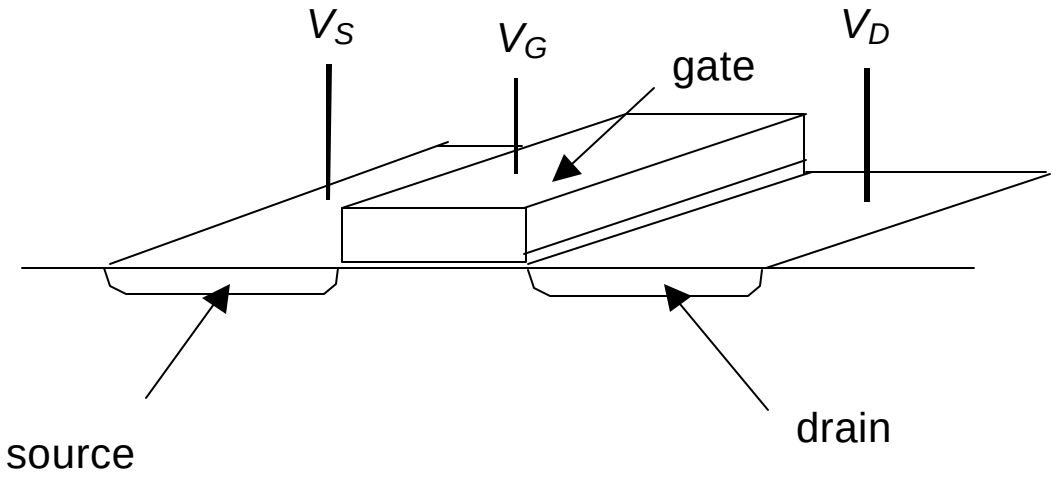
Label the three electrical terminals on the top surface:

Gate: controls whether the switch is conducting or not

Source: NMOS: the lower potential of the two n regions, often GND

Drain: NMOS: the higher potential of the two n regions

Body: Often connected to source, we will assume this in EECS 40, and ignore the body connection (except to include the contacts in layouts).

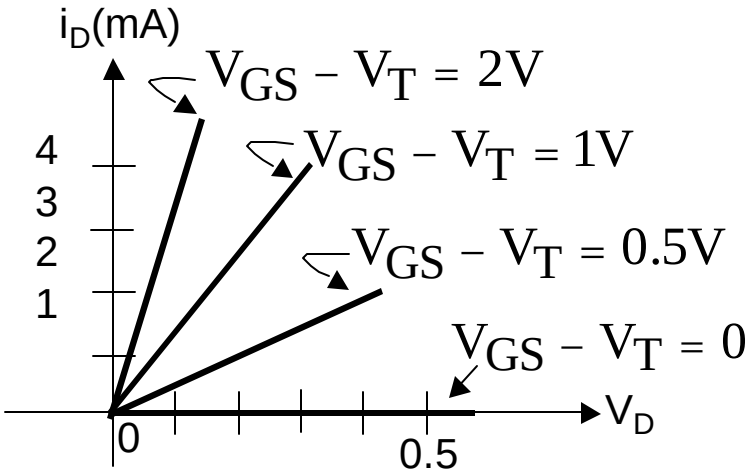


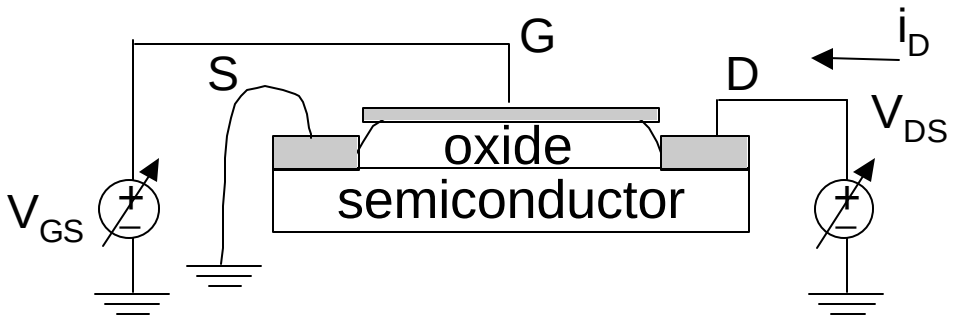
I-V CHARACTERISTICS IN LOW V_{DS} REGIME (cont.)

The drain current is a linear function of drain voltage at low drain voltages

MOS is just a (linear) controlled resistor in the low V_{DS} regime with the drain-to-source resistance depending on how much voltage is applied to the gate (compared to threshold).

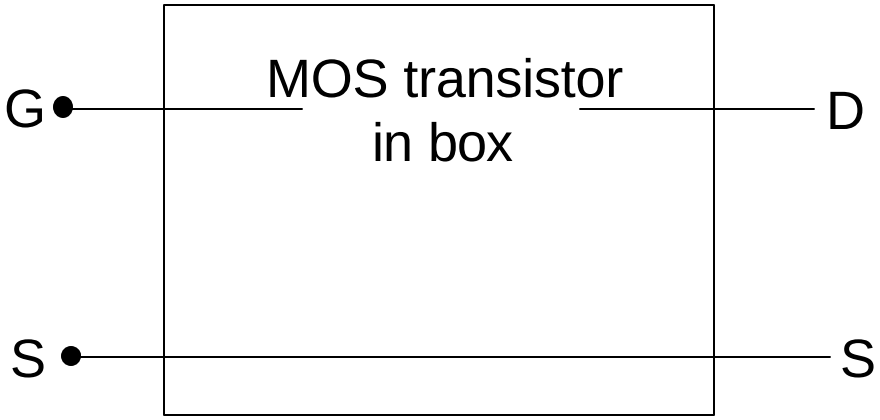
Example of a device characteristic for low V_{DS}

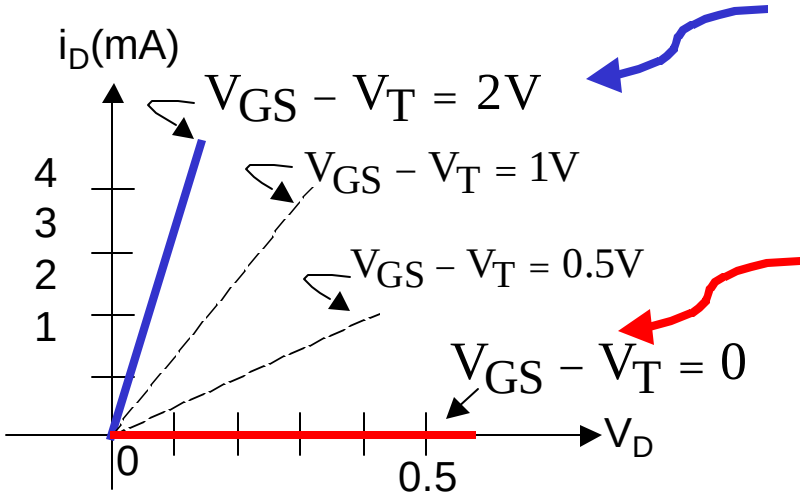




CLEARLY A "CONTROLLED SWITCH"

I-V CHARACTERISTICS IN LOW V_{DS} REGIME (cont.)





This is a very useful device:

A. A large V_{GS} draws no current, but results in a very low resistance between D and S. **Closed switch**.

B. A small V_{GS} ("< V_T") results in an open circuit between D and S. **Open switch**.

What about Larger Drain-Source Voltages -- What Happens?

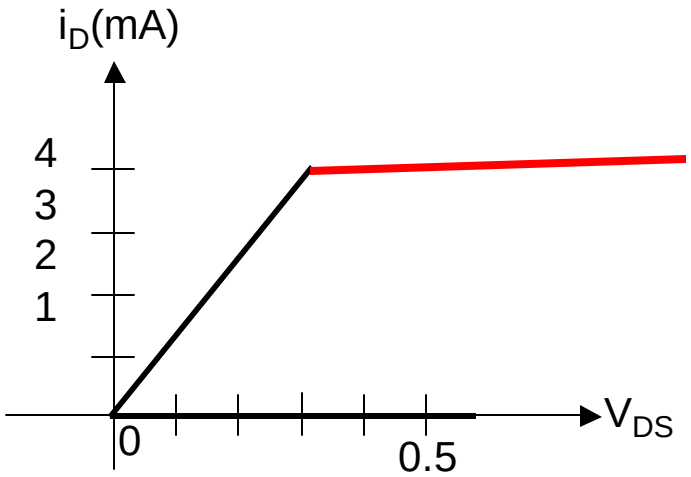
In digital circuits we always use the "shortest" gate length devices possible for reasons of speed. Fortunately this makes the answer to the question above very simple:

For such short-channel devices the drain current saturates because the carriers can only move at a limited speed

We can approximate the I-V characteristics as two straight lines:

a) the linear "resistance" region at low V_{DS} and

b) the saturation region (almost horizontal) at larger V_{DS}.



The Family of I_D vs V_{GS} Curves

For short-channel devices used in digital logic, velocity saturation causes the I_D vs V_{DS} curves to be decidedly nonlinear! Curves which start out as simple linear resistors saturate when the drift velocity reaches 10^7 cm/sec.

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a) the linear "resistance" region at low V_{DS} and

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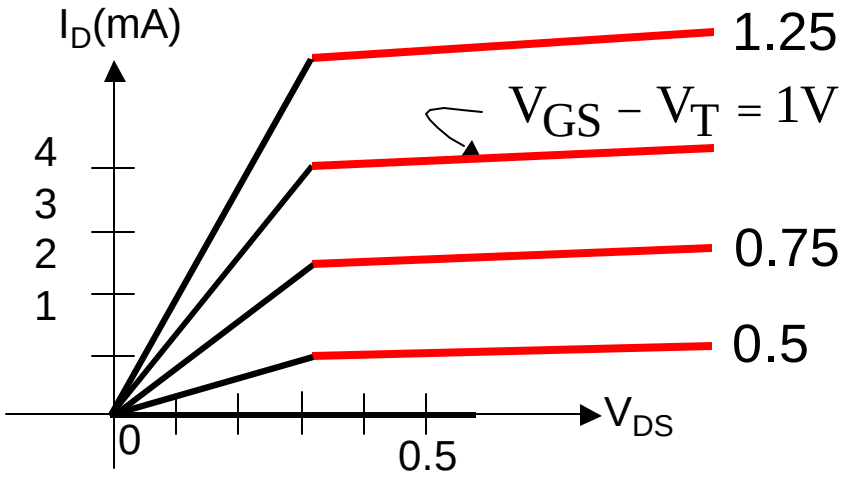


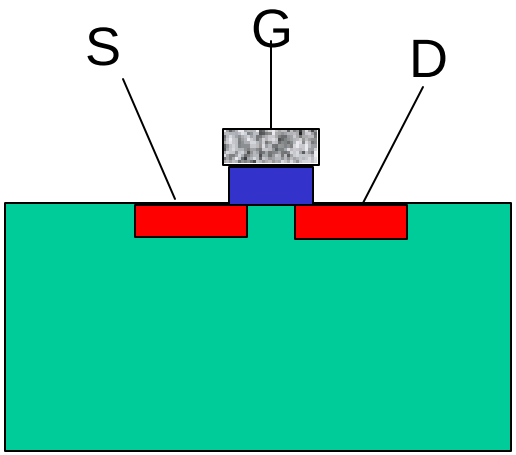
We can write simple empirical equations for the I vs V

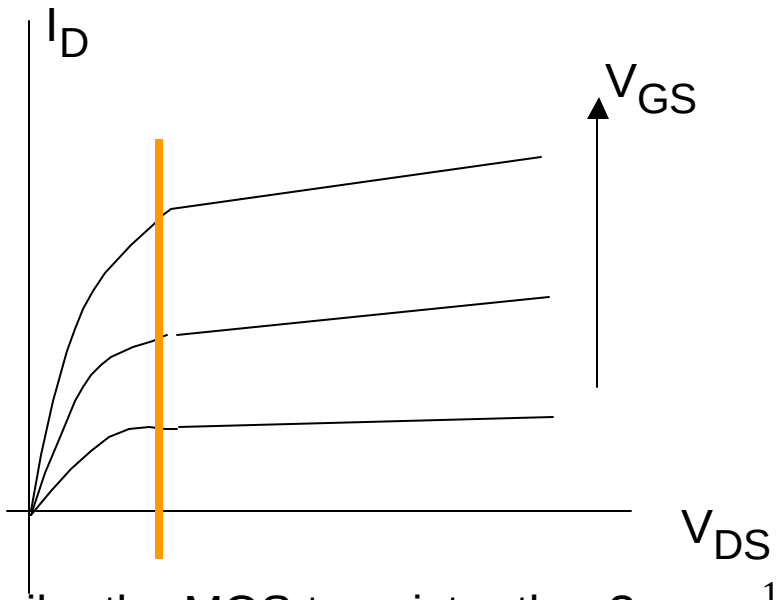
Short Channel MOS "Theory"

We have two regions: the *resistive* region at smaller V_{DS} and the *saturation* region at higher V_{DS} .

In the resistive region we start out like a simple resistor between source and drain (whose value depends on gate voltage) and gradually the curve "bends over" as we approach saturation

In the saturation we have a small gradual increase of I with V_{DS}





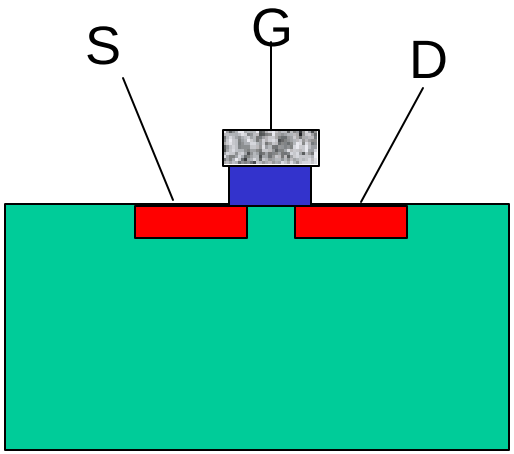
What Equations will we use to describe the MOS transistor then?

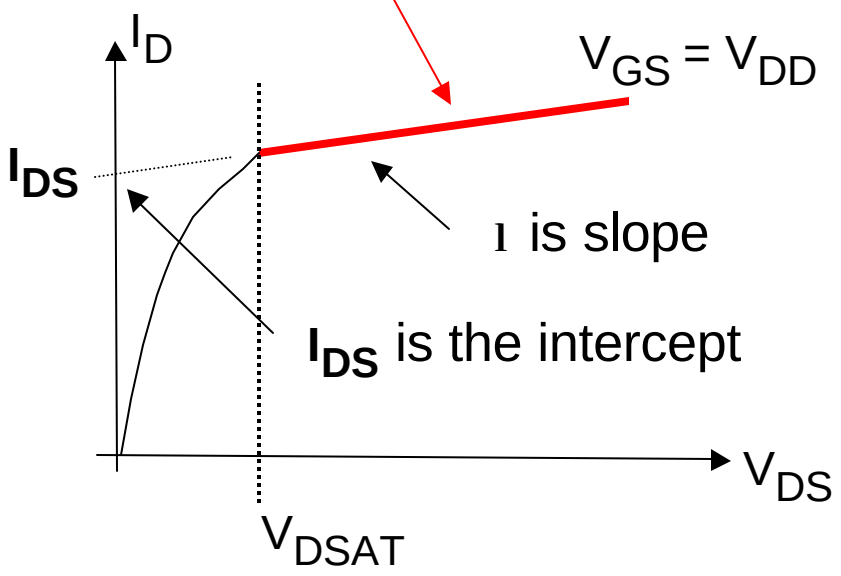
Short Channel MOS "Theory" (cont')

For simple digital circuit calculations the MOS transistor will be essentially off ($\mathbf{V_{GS} < V_T}$) or fully turned on ($\mathbf{V_{GS} = V_{DD}}$, the power supply voltage). In other words we need a single I_D vs $\mathbf{V_{DS}}$ curve, the one for $\mathbf{V_{GS} = V_{DD}}$.

We need to describe the variation of I_D with V_{DS} in the saturation region. For $V_{DS} > V_{DSAT}$ we will use an essentially **empirical** equation for I_D of the form:

$$\mathbf{I_D = I_{DS} \times (1 + \lambda V_{DS})}$$

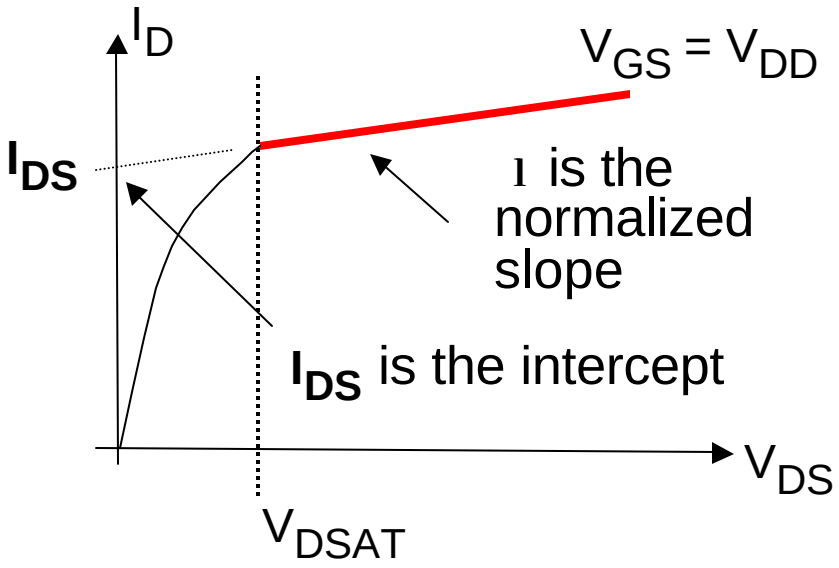




SUMMARY Short Channel MOS

For our digital circuit calculations we will only need to describe the variation of I_D with V_{DS} in the saturation region for the single gate voltage, $V_{GS} = V_{DD}$. We use:

$I_D = I_{DS} \times (1 + \lambda V_{DS})$ in which I_{DS} is proportional to the channel width W.



Thus for our hand calculations we need only to have the following MOS properties specified:

1) Saturation Current I_{DS}

2) The slope λ. This is the fractional increase of current for one volt increase in V_{DS}.