EECS 42 Introduction to Electronics for Computer Science

Andrew R. Neureuther

Lecture # 16 Logic with a State Dependent Device

S&O pp. 593-595, 604-606 (read for graphs and not physics or equations), plus Handout of these viewgraphs.

A) State Dependent Device I_{OUT} vs. V_{OUT}

B) Load Line Analysis for Logic Levels

C) Voltage Transfer Characteristics

VTC = plot of V_{OUT} vs. V_{IN}

D) 42S_NMOS Pull-Down Device and Logic

http://inst.EECS.Berkeley.EDU/~ee42/

Game Plan 03/31/03

Monday 03/31/04

- Welcome back plus HW#8 coaching
- State Dependent Devices (Transistors)
- Load Line, VTC, Pull Down Device (42S_NMOS)

Wednesday 04/02/03:

- Pull-Up Device (42S_PMOS)
- VTC and V_{MID}

Next (11^{th}) Week:

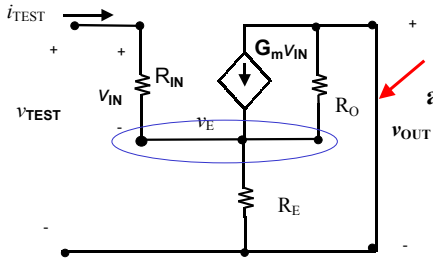
- Monday: 4/7/03 Logic Dynamic via Switched Resistor
  Wednesday: 4/09/03 Quiz; Complementary Gates

Problem set #8: Half-Set - out Monday 3/17 and due at 2:30 4/02 in box in 240 Cory – input/output impedance, comparators

Problem set #9: Monday 3/31 and due at 2:30 4/09 in box in 240 Cory – Static Analysis of an Inverter with simplified EE 42 Device Models

EXAMPLE CIRCUIT: INCREASED INPUT RESISTANCE

Add resistor R_E



The output has been assumed to be shorted

$v_{OUT} = 0$

Analysis: apply i_{TEST} and evaluate v_{TEST}

$$v_{IN} = R_{IN} i_{TEST} \qquad v_{TEST} = R_{IN} i_{TEST} + v_E$$

Similar to the homework

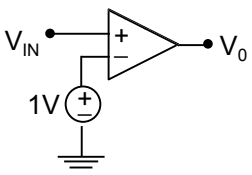
KCL $$\frac{v_E}{R_E} + \frac{v_E}{R_0} - i_{TEST} - G_m R_{IN} i_{TEST} = 0$$

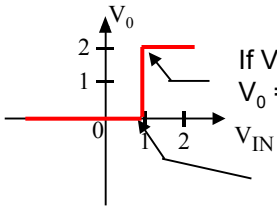
Check for special case for R_0 infinite $$\frac{v_{TEST}}{i_{TEST}} = R_{IN} + (1 + G_m R_{IN}) R_E$$

Intuitive Explanation: R_E puts R_{IN} on a node whose voltage increases in response to current in R_{IN}.

OP-AMP USE AS COMPARATOR (A/D) MODE

Simple comparator with threshold at 1V. Design lower rail at 0V and upper rail at 2V (logic "1"). A = large (e.g. 10^2 to10^5)

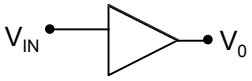




If V_{IN} > 1.010 V, V_0 = 2V = Logic "1"

If V_{IN} < 0.99 V, V_0 = 0V = Logic "0"

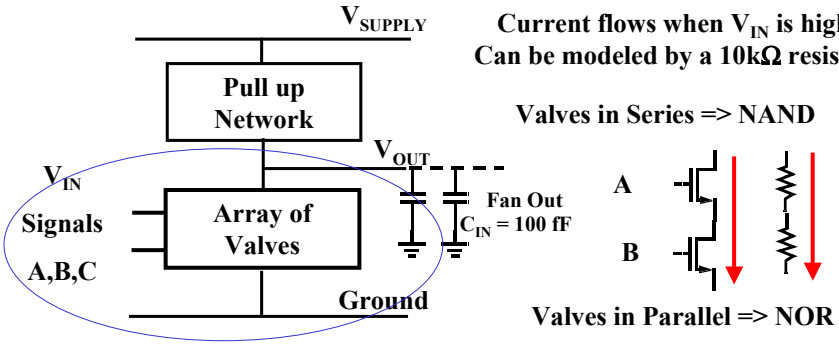
NOTE: The actual diagram of a comparator would not show an amplifier with "offset" power supply as above. It would be a simple triangle, perhaps with the threshold level (here 1V) specified.



Comparator

Logic Gates – How are they built in practice?

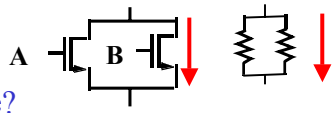
A Valve is a Transistor V_{IN}



Current flows when V_{IN} is high
Can be modeled by a 10kΩ resistor

Valves in Series => NAND

Valves in Parallel => NOR



What goes in this box?

How does it affect digital performance?

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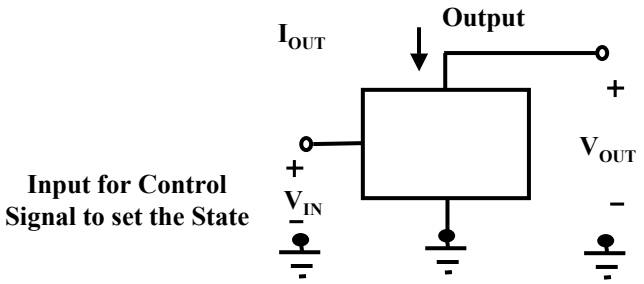
Digital Logic from State-Dependent Three-Terminal Devices

Three-terminal devices such as MOS transistors have characteristics (such as I_{OUT} vs. V_{OUT} curves) on the output side that can be programmed by changing signals on the input side (such as the input voltage).

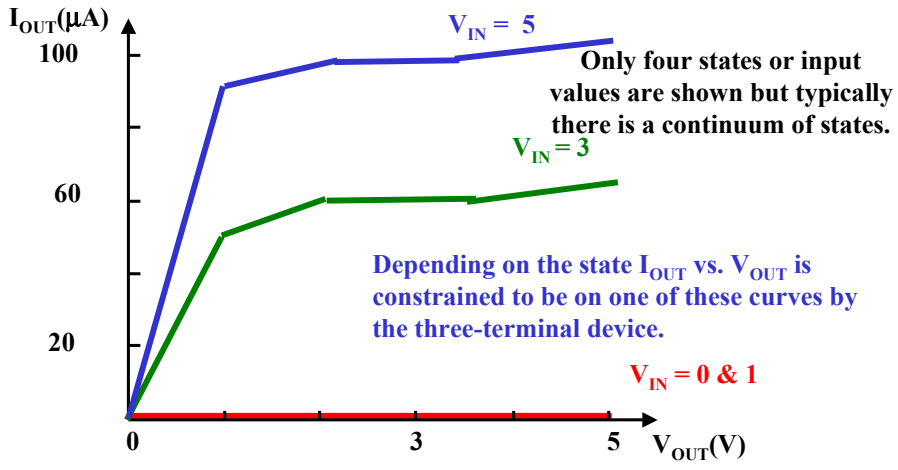
The input can thus be viewed as changing or programming the 'State' of the output of the device.

Three-terminal devices whose 'State' can be programmed can be used to make digital logic devices for computers that respond to input signals.

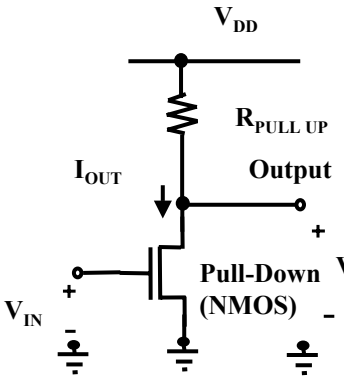
State-Dependent Three-Terminal Device Element



State-Dependent Device I_{OUT} vs. V_{OUT}



Terminology for a Logic Circuit



V_{DD} = Power supply voltage (D is from Drain)

Pull-Down Network = Set of devices used to carry current from the output node to ground to discharge the output node to ground.

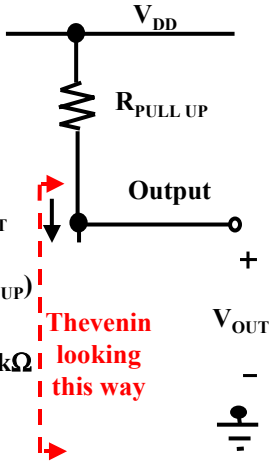
Pull-Up Network = Set of devices used to carry current from the power supply to the output node to charge the output node to the power supply voltage.

I_{OUT} = Current for the device under study.

V_{TD} = Threshold Voltage value of V_{IN} at which the Pull-Down (NMOS transistor) begins to conduct.

$V_{OUT-SAT-D}$ = Value of V_{OUT} beyond which the current I_{OUT-D} saturates at the (drain) current saturation value $I_{OUT-SAT-D}$.

Thevenin Model For Pull-Up Device



$V_{THEVENIN} = V_{DD}$

$I_{OUT\ SHORT\ CIRCUIT} = (V_{DD}/R_{PULL\ UP})$

Example:

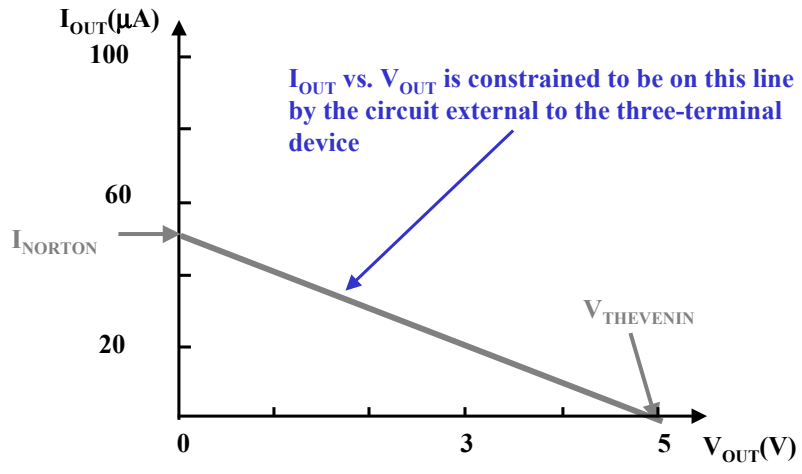
$V_{DD} = 5V$ and $R_{PULL\ UP} = 100k\Omega$

$V_{THEVENIN} = 5V$

$I_{OUT\ SHORT\ CIRCUIT} = 50\ \mu A$

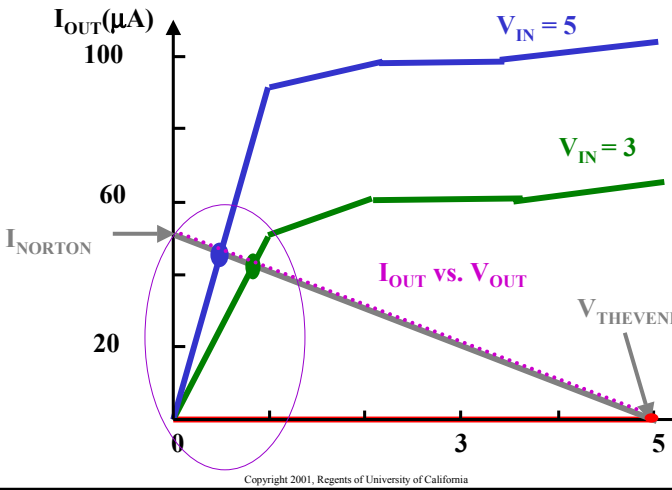
Thevenin Model For Pull-Up Device

I_{OUT} vs. V_{OUT}
For the Pull-Up Resistor and V_{DD}



Composite Current Plot for the Logic Circuit

Three-Terminal Device
Plus Load Line for the Pull-Up Device

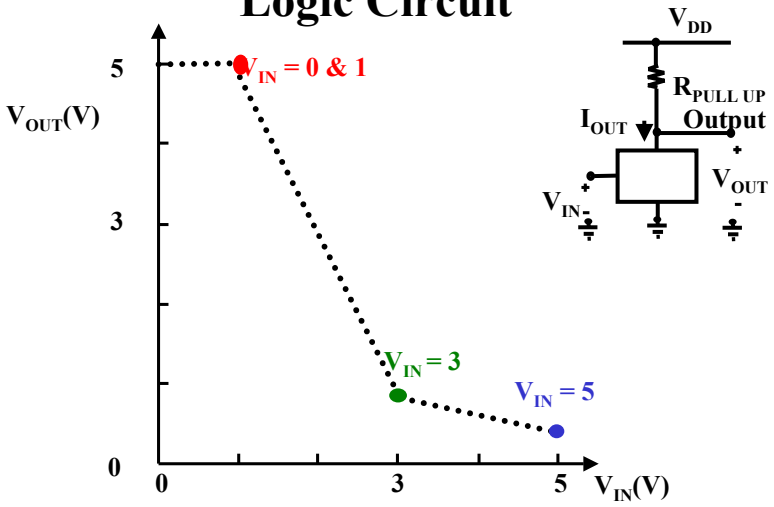


For a given state only one point satisfies both the external circuit and the three-terminal device

Note that when V_{OUT} is low current flows and power is consummed

$V_{IN} = 0$ & 1

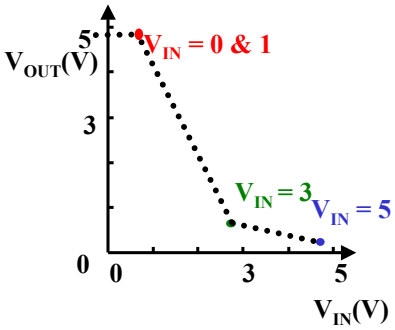
Voltage Transfer Function for the Logic Circuit



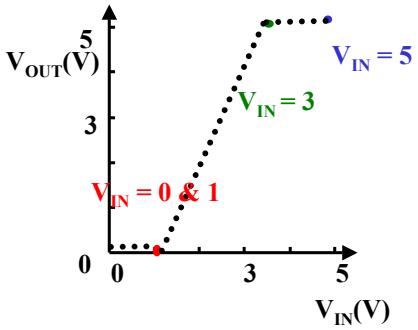
Voltage Transfer Function: V_{OUT} vs. V_{IN}

The V_{OUT} vs. V_{IN} characteristic is another view of the logic gate that is used to determine the inverting and noninverting nature of a gate.

Inverting type



Noninverting type



Saturation Current 42S_NMOS Model

Current I_{OUT} only flows when V_{IN} is larger than the threshold value V_{TD} and the current is proportional to V_{OUT} up to $V_{OUT-SAT-D}$ where it reaches the saturation current

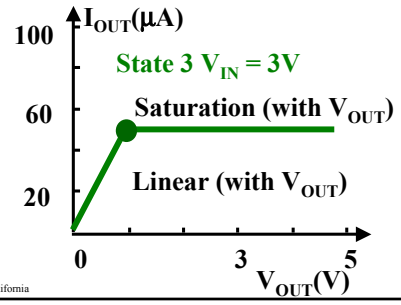
$$I_{OUT-SAT-D} = k_D\left(V_{IN} - V_{TD}\right)V_{OUT-SAT-D}$$

Note that we have added an extra parameter to distinguish between threshold (V_{TD}) and saturation ($V_{OUT-SAT-D}$).

Example:
k_D = 25 μA/V²
V_{TD} = 1V
$V_{OUT-SAT-D}$ = 1V

Use these values in the homework.

$$I_{OUT-SAT-PD} = 25\frac{\mu A}{V^2}(3V - 1V)1V = 50\mu A$$



Drawing I_{OUT} as function of V_{IN} and V_{OUT} for the 42S_NMOS Pull-Down Device

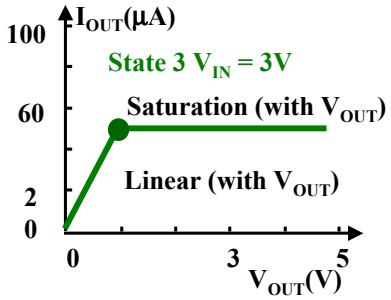
The equations are expressly designed for EE42 to make it very simple to draw I_{OUT} vs. V_{OUT}

1) For $V_{IN} < V_{TD}$, the current is zero.

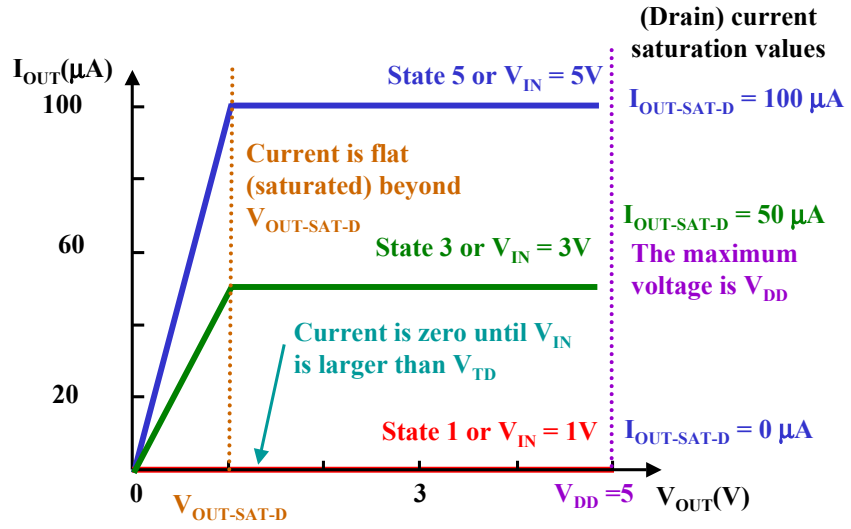
2) For $V_{IN} > V_{TD}$, first evaluate the current I_{OUT} at $V_{OUT} = V_{TD}$ and plot the single point (I_{OUT}, V_{OUT})

3) Draw a line from this point to the origin to create the linear region.

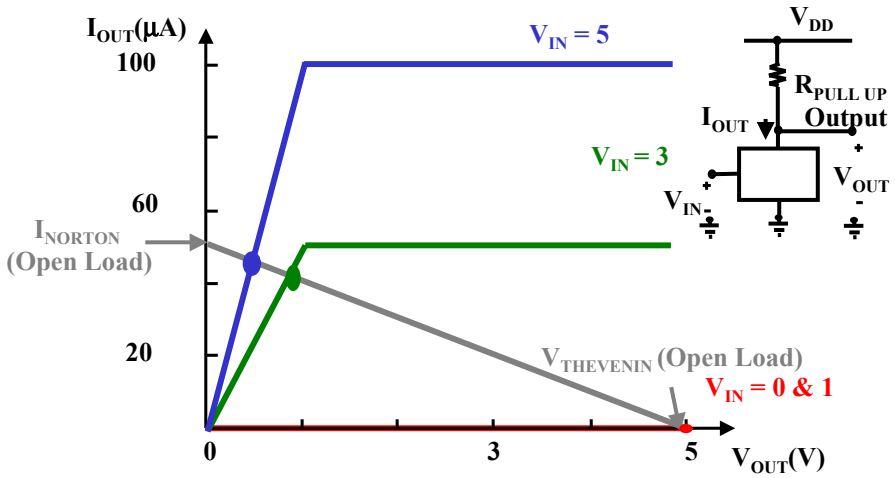
4) Draw a horizontal line from this point to create the saturation region



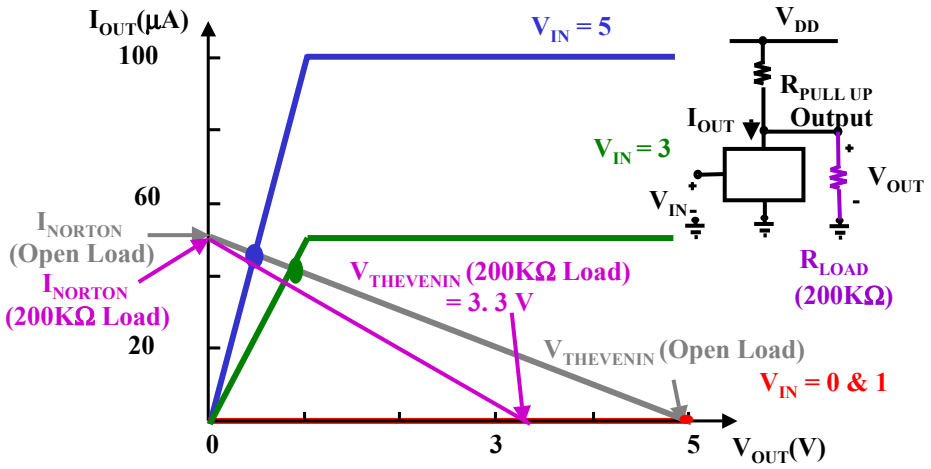
States of 42S_NMOS are Voltage Levels of V_{IN}



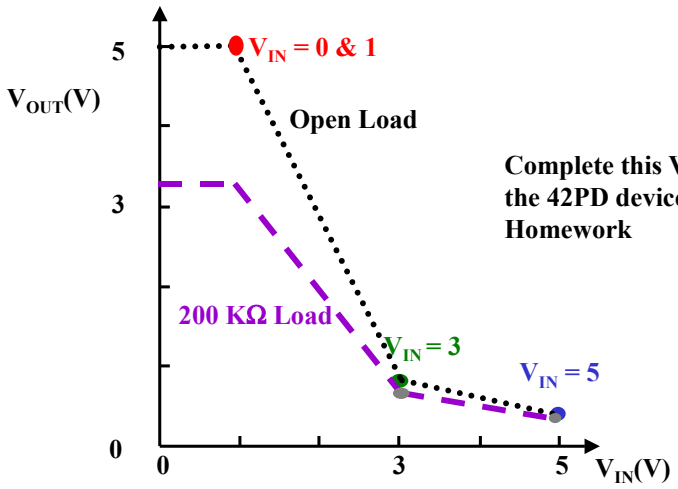
Composite Current Plot for the 42S_NMOS Logic Circuit



Composite Current Plot for the 42S_NMOS Circuit with 200kΩ Load to Ground



Voltage Transfer Function for the 42S_NMOS Logic Circuit w/wo Load



Complete this VTC for the 42PD device in the Homework