

EECS 42 Introduction to Electronics for Computer Science

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Lecture # 18 Logic Transients

Handout of Mon Lecture.

- A) Quiz 4/9 and Midterm 4/16 review
- B) Transient as Capacitor Charging
- C) Equivalent Resistance for MOS
- D) Inverter Propagation Delay
- E) Complementary MOS Operation

<http://inst.EECS.Berkeley.EDU/~ee42/>

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Game Plan 04/07/03

Last Week: Static Logic: NMOS, CMOS; Graphical Solution and VTC) {All of this will be on 2nd Midterm}

Monday 4/07/03:

- Discharging Capacitors with NMOS and Eq. Resistance
- CMOS Logic and Propagation delay

Wednesday 04/09/03:

- QUIZ: Digital Blocks including timing diagrams and Dependent sources including Op-Amps
- Worst Case CMOS delay, Cascade and CMOS Latch

Next (11th) Week: Diodes and MOS Operation

Problem set #9: Monday 3/31 and due at 2:30 4/09 in box in 240 Cory – Static Analysis of an Inverter with simplified EE 42 Device Models

No Problem set for 4/16 as Midterm 4/16: Lectures 1-17 with emphasis on Lectures 10-17; Review Session Monday 5:30-7PM

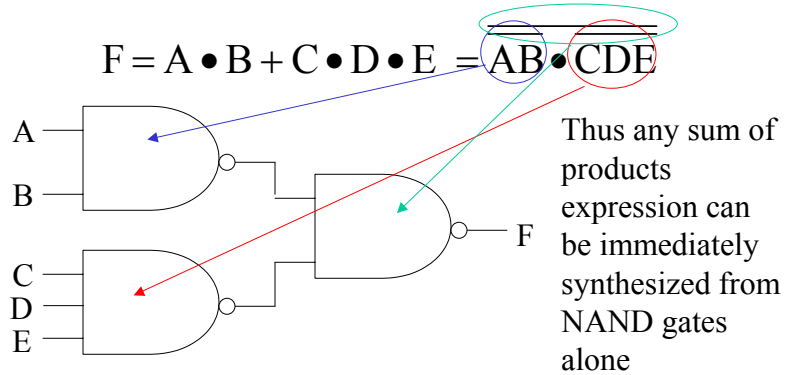
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Logical Synthesis Guided by DeMorgan's Theorem

DeMorgan's Theorem :

$$A + B + C = \overline{\overline{A} \overline{B} \overline{C}} \quad \text{or} \quad \overline{A} + \overline{B} + \overline{C} = \overline{[A B C]}$$

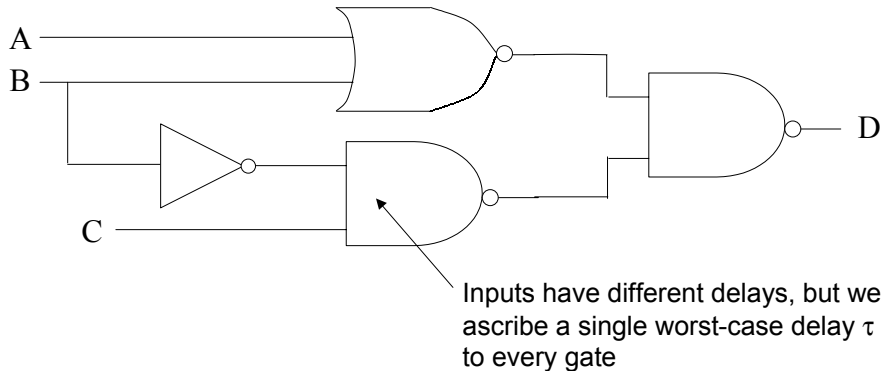
Example of Using DeMorgan's Theorem:



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EFFECT OF GATE DELAY

Cascade of Logic Gates



How many "gate delays for shortest path? ANSWER : 2

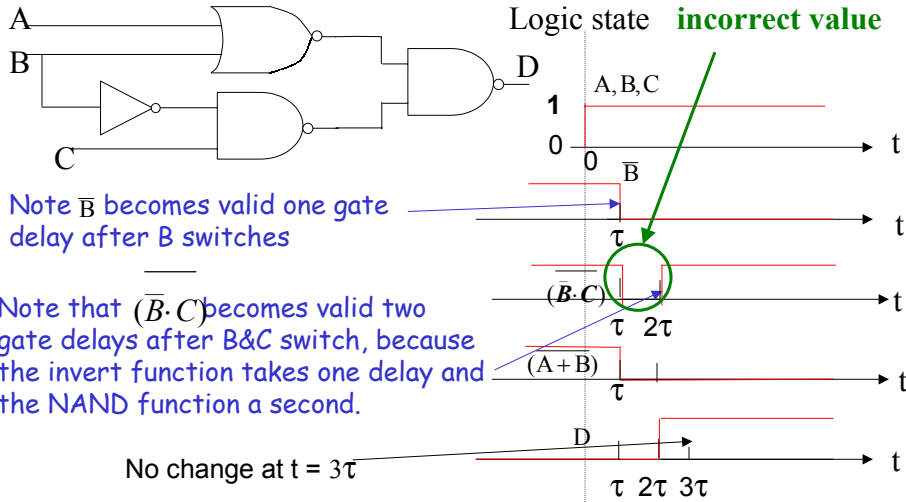
How many gate delays for longest path? ANSWER : 3

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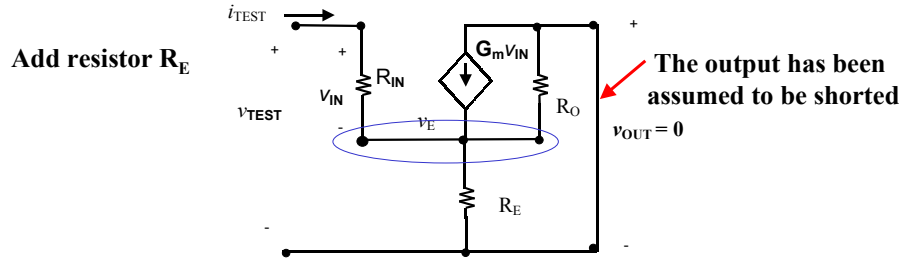
TIMING DIAGRAMS

Show transitions of variables vs time

Glitching: temporary switching to an incorrect value



EXAMPLE CIRCUIT: INCREASED INPUT RESISTANCE



Analysis: apply i_{TEST} and evaluate v_{TEST}

$$v_{IN} = R_{IN}i_{TEST} \quad v_{TEST} = R_{IN}i_{TEST} + v_E$$

KCL $\frac{v_E}{R_E} + \frac{v_E}{R_0} - i_{TEST} - G_m R_{IN} i_{TEST} = 0$

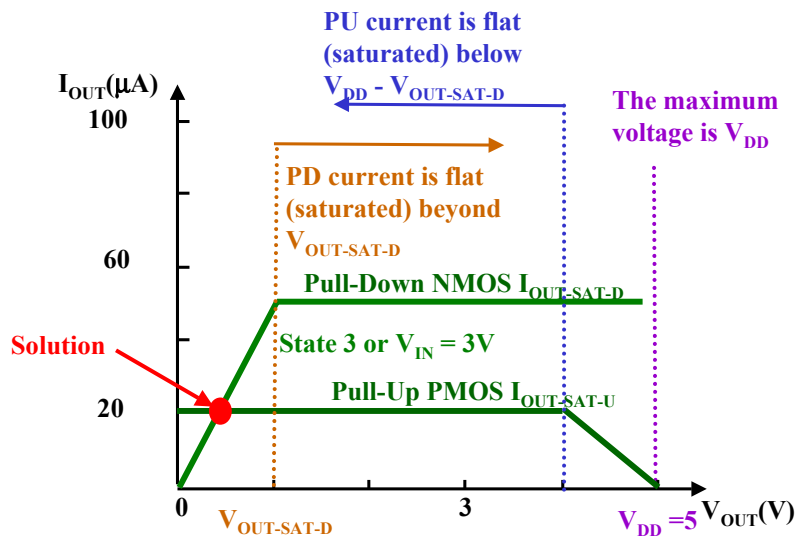
Check for special case for R_0 infinite $\frac{v_{TEST}}{i_{TEST}} = R_{IN} + (1 + G_m R_{IN})R_E$

The output has been assumed to be shorted $v_{OUT} = 0$

Similar to the homework

Intuitive Explanation: R_E puts R_{IN} on a node whose voltage increases in response to current in R_{IN} .

Composite I_{OUT} vs. V_{OUT} for CMOS



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Method for Finding V_M

At V_M ,

- 1) $V_{OUT} = V_{IN} = V_M$
- 2) Both devices are in saturation
- 3) $I_{OUT-SAT-D} = I_{OUT-SAT-U}$

$$I_{OUT-SAT-D} = k_D (V_{IN} - V_{TD})^2 V_{OUT-SAT-D}$$

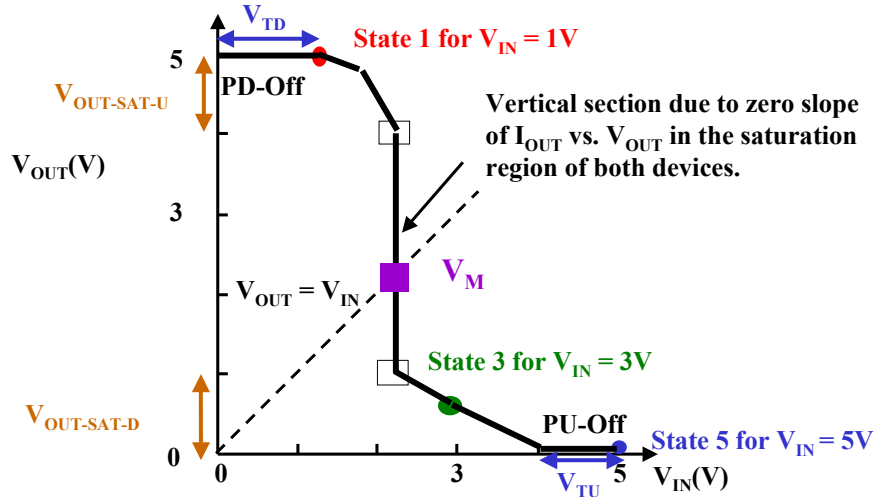
$$= I_{OUT-SAT-U} = k_U (V_{DD} - V_{IN} - V_{TU})^2 V_{OUT-SAT-U}$$

Substitute V_M Solve for V_M

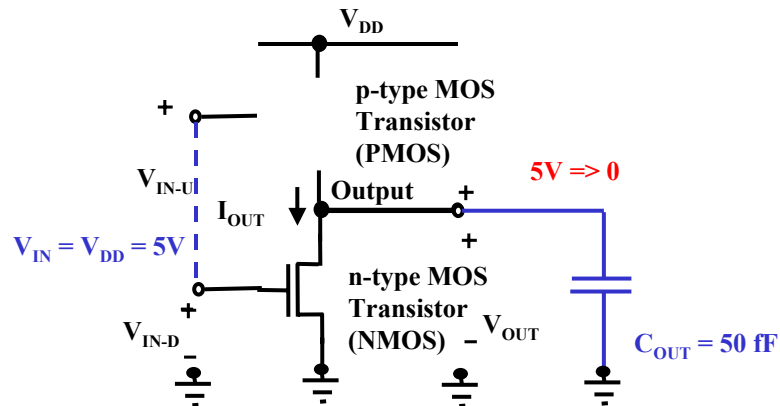
Example Result: When $k_D = k_U$, $V_{OUT-SAT-D} = V_{OUT-SAT-U}$
and $V_{TD} = V_{TU}$, then $V_M = V_{DD}/2$

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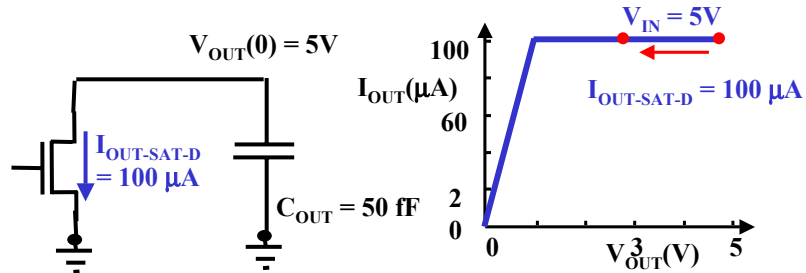
Voltage Transfer Function for the Complementary Logic Circuit



Transient Gate Problem: Discharging and Charging Capacitance on the Output



Output Propagation Delay High to Low

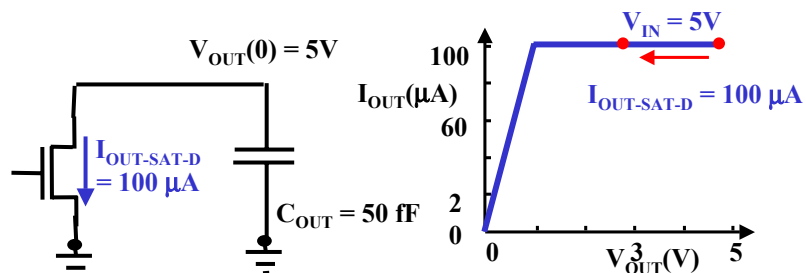


When V_{IN} goes High V_{OUT} starts decreases with time

Assume that the necessary voltage swing to cause the next downstream gate to begin to switch is $V_{DD}/2$ or 2.5V.

That is the propagation delay τ_{HL} for the output to go from high to low is the time to go from $V_{DD} = 5V$ to to $V_{DD}/2 = 2.5V$

Output Propagation Delay High to Low (Cont.)



When $V_{OUT} > V_{OUT-SAT-D}$ the available current is $I_{OUT-SAT-D}$

For this circuit when $V_{OUT} > V_{OUT-SAT-D}$ the available current is constant at $I_{OUT-SAT-D}$ and the capacitor discharges.

The **propagation delay** is thus

$$\Delta t = \frac{C_{OUT} \Delta V}{I_{OUT-SAT-D}} = \frac{C_{OUT} V_{DD}}{2 I_{OUT-SAT-D}} = \frac{50 \text{ fF} \cdot 2.5V}{100 \mu A} = 1.25 \text{ ns}$$

Switched Equivalent Resistance Model

The above model assumes the device is an ideal constant current source.

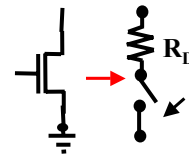
- 1) This is not true below $V_{OUT-SAT-D}$ and leads to inaccuracies.
- 2) Combining ideal current sources in networks with series and parallel connections is problematic.

Instead define an equivalent resistance for the device by setting $0.69R_D C$ equal to the Δt found above

$$\Delta t = \frac{C_{OUT} V_{DD}}{2I_{OUT-SAT-D}} = 0.69R_D C_{OUT}$$

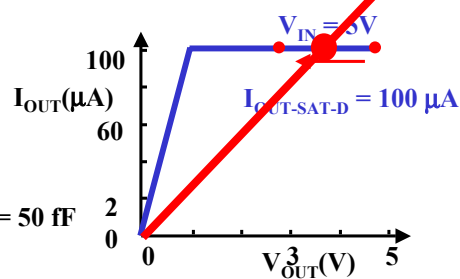
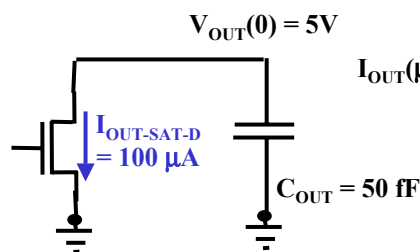
This gives

$$R_D = \frac{V_{DD}}{2 \cdot (0.69)I_{OUT-SAT-D}} \approx \frac{3}{4} \frac{V_{DD}}{I_{OUT-SAT-D}} = \frac{3}{4} \frac{5V}{100\mu A} = 37.5k\Omega$$



Each device can now be replaced by this equivalent resistor.

$\frac{3}{4} V_{DD}/I_{SAT}$ Physical Interpretation



$\frac{3}{4} V_{DD}$ is the average value of V_{OUT}

Approximate the NMOS device curve by a straight line from $(0,0)$ to $(I_{OUT-SAT-D}, \frac{3}{4} V_{DD})$.

Interpret the straight line as a resistor with

$$\text{slope} = 1/R = \frac{3}{4} \frac{V_{DD}}{I_{SAT}}$$

Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.

The resistance is inversely proportion to the gate width/length in the geometrical layout.

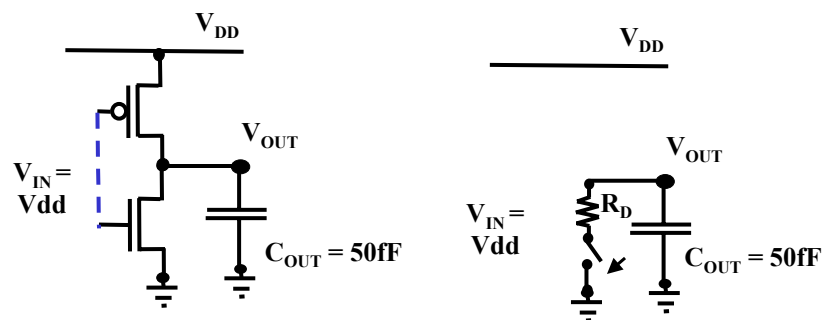
Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.

The current per unit width of the gate increases nearly inversely with the linewidth.

For convenience in EE 42 we assume $R_D = R_U = 10 \text{ k}\Omega$

Inverter Propagation Delay

Discharge (pull-down)



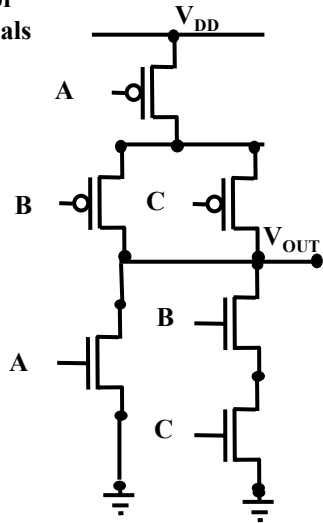
$$\Delta t = 0.69R_D C_{OUT} = 0.69(10\text{k}\Omega)(50\text{fF}) = 345 \text{ ps}$$

Discharge (pull-up)

$$\Delta t = 0.69R_U C_{OUT} = 0.69(10\text{k}\Omega)(50\text{fF}) = 345 \text{ ps}$$

NMOS and PMOS use the same set of input signals

CMOS Logic Gate



PMOS only in pull-up

PMOS conduct when input is low

PMOS do not conduct when $A + (BC)$

NMOS only in pull-down

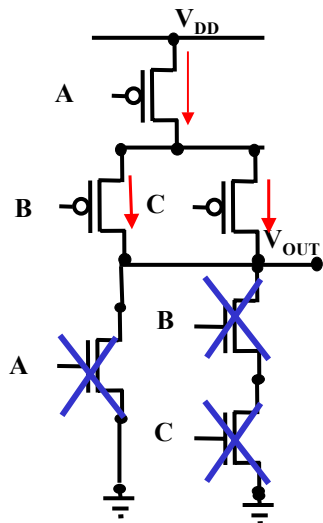
NMOS conduct when input is high.

NMOS conduct for $A + (BC)$

Logic is Complementary and produces $F = \overline{A + (BC)}$

CMOS Logic Gate: Example Inputs

A = 0
B = 0
C = 0



PMOS all conduct

Output is High

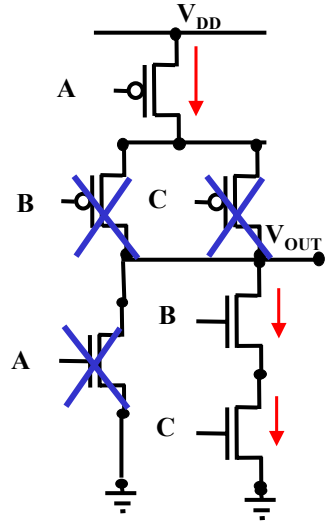
$= V_{DD}$

NMOS do not conduct

Logic is Complementary and produces $F = 1$

CMOS Logic Gate: Example Inputs

A = 0
B = 1
C = 1



PMOS A conducts; B and C Open

Output is High

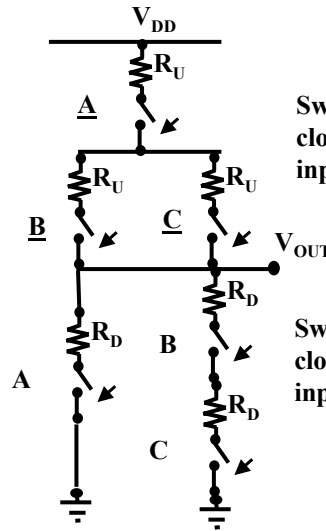
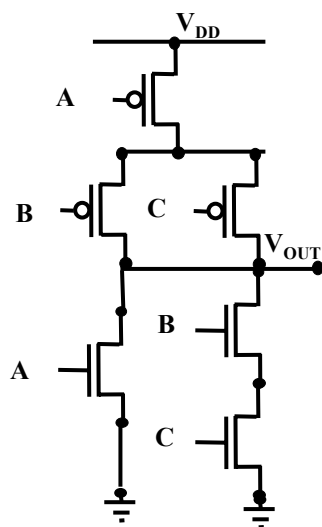
= 0

NMOS B and C conduct; A open

Logic is Complementary and produces F = 0

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Switched Equivalent Resistance Network



Switches close when input is low.

Switches close when input is high.

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