EECS 42 Introduction to Electronics for Computer Science

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Lecture # 19 Logic Transients

Handout of Wed Lecture.

A) Quiz
B) Worst Case CMOS Delay
C) Delay in CMOS Cascade

http://inst.EECS.Berkeley.EDU/~ee42/

Game Plan 04/07/03

Last Week: Static Logic: NMOS, CMOS; Graphical Solution and VTC) {All of this will be on 2nd Midterm)

Monday 4/07/03:

- **Discharging Capacitors with NMOS and Eq. Resistance**
- **CMOS Logic and Propagation delay**

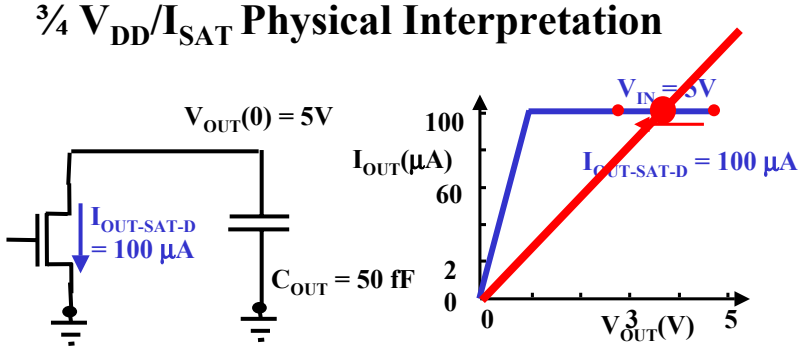
Wednesday 04/09/03:

- **QUIZ: Digital Blocks including timing diagrams and Dependent sources including Op-Amps**
- **Worst Case CMOS delay, Cascade and CMOS Latch**

Next (11th) Week: Diodes and MOS Operation

No Problem set for 4/16 as Midterm 4/16: Lectures 1-17 with emphasis on Lectures 10-17; Review Session Monday 5:30-7PM

¾ V_{DD}/I_{SAT} Physical Interpretation



¾ V_{DD} is the average value of V_{OUT}

Approximate the NMOS device curve by a straight line from (0,0) to ($I_{OUT-SAT-D}$, ¾ V_{DD}).

Interpret the straight line as a resistor with

$$\text{slope} = 1/R = ¾\ V_{DD}/I_{SAT}$$

Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.

The resistance is inversely proportion to the gate width/length in the geometrical layout.

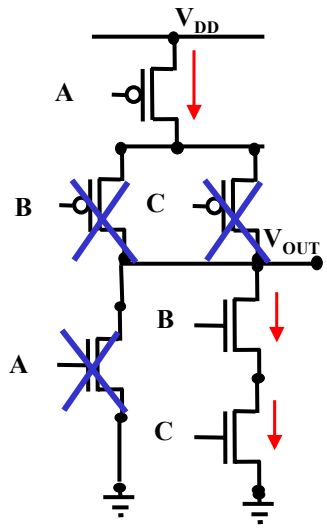
Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.

The current per unit width of the gate increases nearly inversely with the linewidth.

For convenience in EE 42 we assume $R_D = R_U = 10\ k\Omega$

CMOS Logic Gate: Example Inputs

A = 0
B = 1
C = 1



PMOS A conducts; B and C Open

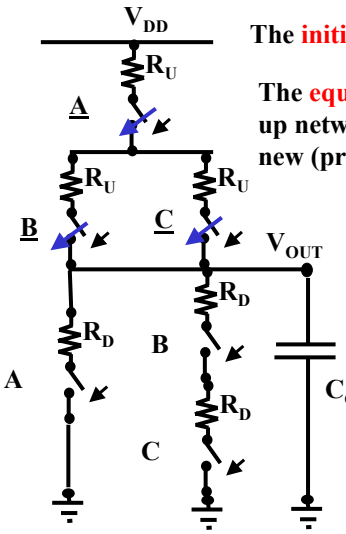
Output is High

= 0

NMOS B and C conduct; A open

Logic is Complementary and produces F = 0

Logic Gate Propagation Delay: Initial State



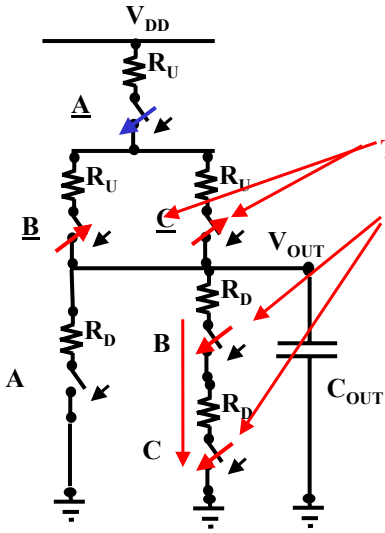
The initial state depends on the old (previous) inputs.

The equivalent resistance of the pull-down or pull-up network for the transient phase depends on the new (present) input state.

Example: A=0, B=0, C=0 for a long time.

These inputs provided a path to V_{DD} for a long time and the capacitor has precharged up to V_{DD} = 5V.

Logic Gate Propagation Delay: Transient



At t=0, B and C switch from low to high (V_{DD}) and A remains low.

This breaks the path from V_{OUT} to V_{DD}

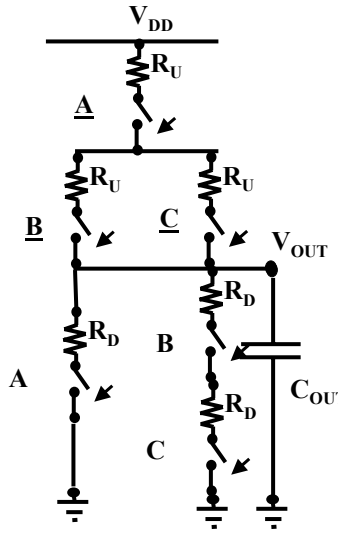
And opens a path from V_{OUT} to GND

C_{OUT} discharges through the pull-down resistance of gates B and C in series.

$$\Delta t = 0.69(R_{DB}+R_{DC})C_{OUT}$$
$$= 0.69(20k\Omega)(50fF) = 690 \text{ ps}$$

The propagation delay is two times longer than that for the inverter!

Logic Gate: Worst Case Scenarios



What combination of previous and present logic inputs will make the Pull-Up the fastest?

What combination of previous and present logic inputs will make the Pull-Up the slowest?

What combination of previous and present logic inputs will make the Pull-Down the fastest?

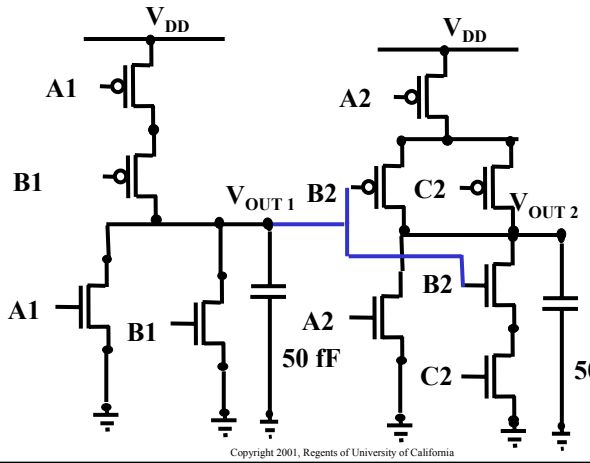
What combination of previous and present logic inputs will make the Pull-Down the slowest?

Fastest overall?

Slowest overall?

Logic Gate Cascade

To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.



$B2 = V_{OUT\ 1}$

The four independent input are A1, B1, A2 and C2.

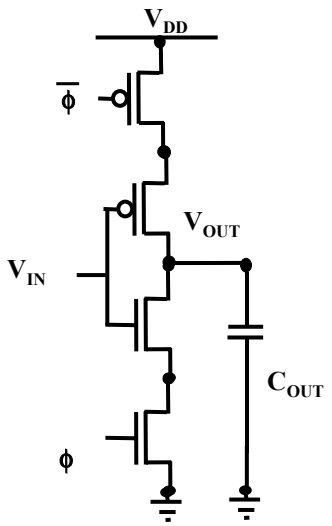
A2 high discharges gate 2 without even waiting for the output of gate 1.

C2 high and A2 low makes gate 2 wait for Gate 1 output

Data Synchronization problem

- Combinatorial logic gates can give incorrect answers prematurely and may take several gate propagation delays produce an answer.
- Clocks (signals as to when to proceed) and latches (which capture and hold the correct outputs) can provide synchronization.

Latch Controlled by a Clock

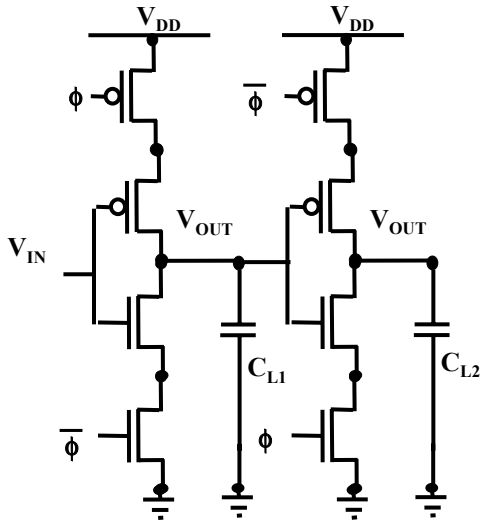


An inverter with clocked devices in series can form a latch.

When the clock ϕ is high its complement $\overline{\phi}$ is low and the inverter operates.

To synchronize the data the clock remains low until the data is correct at all locations on the chip. When the clock goes high the inverse of the data is passed.

Latch Work Best In Pairs



The first stage operates while the clock is low and inverts and amplifies the arriving signal and charges or discharges C_{L1}.

The second stage operates while the clock is high and inverts the signal on C_{L1} to charge or discharge C_{L2} and downstream logic gate inputs.