

EECS 42 Intro. electronics for CS Spring 2003 Lecture 19: 04/09/03 A.R. Neureuther  
Version Date 04/05/03

## EECS 42 Introduction to Electronics for Computer Science

### Andrew R. Neureuther

### Lecture # 19 Logic Transients

Handout of Wed Lecture.

A) Quiz  
B) Worst Case CMOS Delay  
C) Delay in CMOS Cascade

<http://inst.EECS.Berkeley.EDU/~ee42/>

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## Switched Equivalent Resistance Values

The resistor values depend on the properties of silicon, geometrical layout, design style and technology node.

n-type silicon has a carrier mobility that is 2 to 3 times higher than p-type.

The resistance is inversely proportion to the gate width/length in the geometrical layout.

Design styles may restrict all NMOS and PMOS to be of a predetermined fixed size.

The current per unit width of the gate increases nearly inversely with the linewidth.

**For convenience in EE 42 we assume  $R_p = R_n = 10\text{ k}\Omega$**

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## Game Plan 04/07/03

Last Week: Static Logic: NMOS, CMOS; Graphical Solution and VTC (All of this will be on 2<sup>nd</sup> Midterm)

Monday 4/07/03:

- Discharging Capacitors with NMOS and Eq. Resistance
- CMOS Logic and Propagation delay

Wednesday 04/09/03:

- QUIZ: Digital Blocks including timing diagrams and Dependent sources including Op-Amps
- Worst Case CMOS delay, Cascade and CMOS Latch

Next (11<sup>th</sup>) Week: Diodes and MOS Operation

**No Problem set for 4/16 as Midterm 4/16: Lectures 1-17 with emphasis on Lectures 10-17; Review Session Monday 5:30-7PM**

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## CMOS Logic Gate: Example Inputs

A = 0  
B = 1  
C = 1

PMOS A conducts; B and C Open

Output is High

= 0

NMOS B and C conduct; A open

Logic is Complementary and produces  $F = 0$

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## $\frac{3}{4} V_{DD}/I_{SAT}$ Physical Interpretation

$\frac{3}{4} V_{DD}$  is the average value of  $V_{OUT}$

Approximate the NMOS device curve by a straight line from  $(0,0)$  to  $(I_{OUT-SAT-D}, \frac{3}{4} V_{DD})$ .

Interpret the straight line as a resistor with slope  $= 1/R = \frac{3}{4} V_{DD}/I_{SAT}$

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## Logic Gate Propagation Delay: Initial State

The **initial state** depends on the old (previous) inputs.

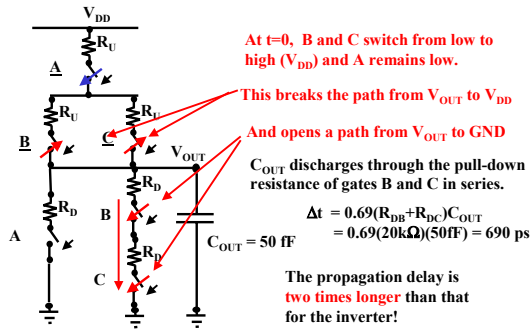
The **equivalent resistance** of the pull-down or pull-up network for the transient phase depends on the new (present) input state.

Example: A=0, B=0, C=0 for a long time.

These inputs provided a path to  $V_{DD}$  for a long time and the capacitor has precharged up to  $V_{DD} = 5V$ .

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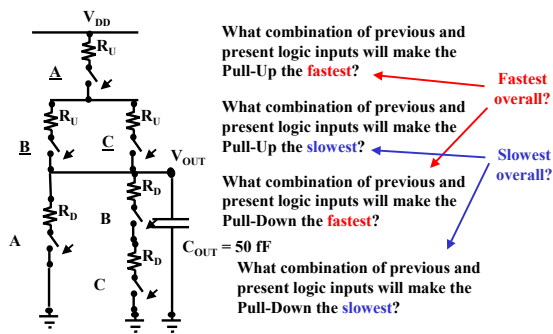
### Logic Gate Propagation Delay: Transient



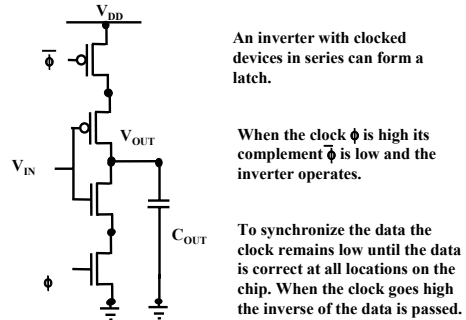
### Data Synchronization problem

- Combinatorial logic gates can give incorrect answers prematurely and may take several gate propagation delays produce an answer.
- Clocks (signals as to when to proceed) and latches (which capture and hold the correct outputs) can provide synchronization.

### Logic Gate: Worst Case Scenarios

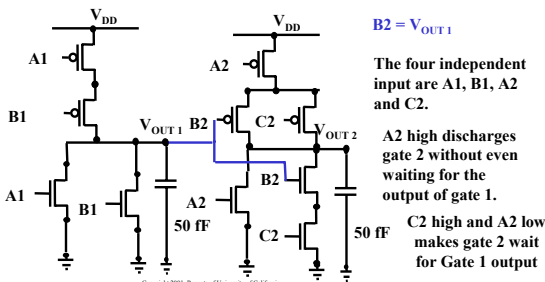


### Latch Controlled by a Clock



### Logic Gate Cascade

To avoid large resistance due to many gates in series, logic functions with 4 or more inputs are usually made from cascading two or more 2-4 input blocks.



### Latch Work Best In Pairs

