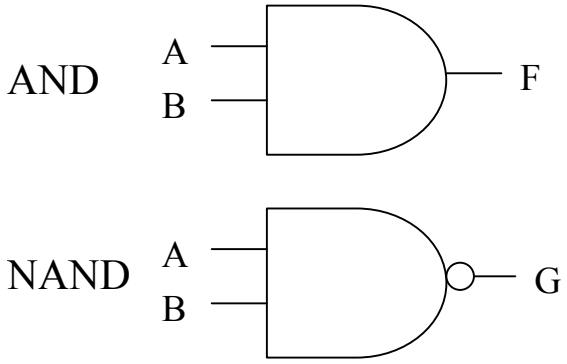
Department of EECS

University of California, Berkeley

Logic gates – Prelab

1. AND VS NAND

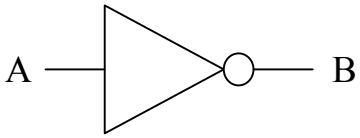
Write the truth table for an AND gate and a NAND gate. How are they different?



A	B	F	G
0	0		
0	1		
1	0		
1	1		

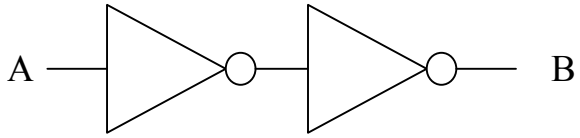
2. NOT Gate

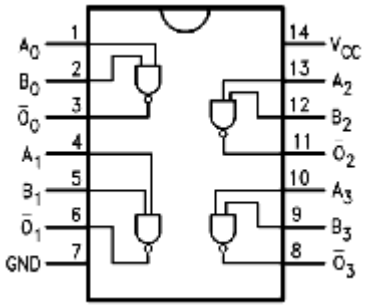
(a) A NOT gate is basically an inverter. If the input is 0, then the output is 1.



Using the result from the truth table above, draw how you will construct a NOT gate using a NAND gate.

(b) Now draw the circuit diagram of how you will construct a chain of 2 inverters using the MM74HC00 chip. Remember to label the input (A) and output (B) and connect pin 14 and pin 7 correctly.





3. Gate Delay

A NOT gate has a low-to-high delay of 25 ns and a high-to-low delay of 10 ns. What is the average propagation delay of this NOT gate? If a chain of 2 inverters is constructed using two of these NOT gates, what is the total propagation delay of this chain of 2 inverters?