Name:_____
TA: _____
Section:_____

EECS 40/43
Prelab: Debugging Circuits

1. A XOR logic gate can be constructed using 4 NANDs as shown in Figure 2a of the experiment write-up. Write down the truth table for the XOR for nodes C to F.

INPUTS		OUTPUTS			
A	**B**	**C**	**D**	**E**	**F**
0	0				
0	1				
1	0				
1	1				

2. What are some of the common errors students would make when building circuits? What is the approach to debug those errors?

3. An EE 43 student would like to build the following circuit and a picture of the constructed circuit was taken. Being a nice classmate of this poor student, please help him identify his errors. (Hint: there are 4 mistakes)
http://www-inst.eecs.berkeley.edu/~ee43/f02/prelabs/debug.jpg