Department of EECS

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Logic gates – Lab Report

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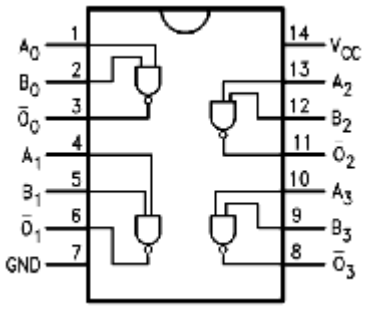
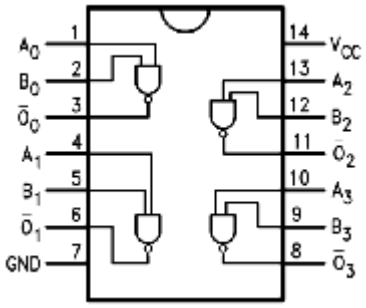
1. Construct your LED logic probe. What color LED do you have (red is best)? Describe how is the LED a simple visual indicator of a NOT gate?

2. What R do you use in your LED logic probe and how much current is flowing through the LED? What is its brightness at 2V and 5V? WARNING: THE INPUT LOGIC VOLTAGE CANNOT EXCEED V_{CC} !!!

3. Draw the circuit schematic of how you construct a NOT gate using the MM74HC00 chip. What is the high-to-low and low-to-high delay for Vcc = 5V and Vcc = 2V?



4. Draw the circuit schematic of how you construct a chain of 4 inverters using the MM74HC00 chip. What is the high-to-low and low-to-high delay for each inverter?



Vcc = 5V	1 gate	2 gates	3 gates	4 gates
High-to-low				
Low-to-high				
Avg gate delay				

Vcc = 2V	1 gate	2 gates	3 gates	4 gates
High-to-low				
Low-to-high				
Avg gate delay				

5. Now using the digital probes, what is the high-to-low and low-to-high delay for each inverter for Vcc = 5V and Vcc = 2V?

Vcc = 5V	1 gate	2 gates	3 gates	4 gates
High-to-low				
Low-to-high				
Avg gate delay				

Vcc = 2V	1 gate	2 gates	3 gates	4 gates
High-to-low				
Low-to-high				
Avg gate delay				

6. Based on the gate delay difference between 1 and 3 gates (two gate delays) what is the average gate delay at each of the supply voltages. (Note: we do not want to use the difference between 2 and 4 delays because the last gate is not loaded by the input to any other logic circuit). Average Gate Delay = _____ at 5V; Average Gate Delay = _____ at 2V.