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Logic gates

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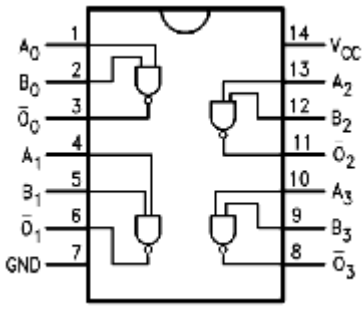
September 1st 2001

1. Introduction

This lab introduces digital logic. You use commercially available "Quad NAND Gates" to breadboard some simple logic functions, especially the NOT gate and the XOR gate. You will build a simple logic probe with an LED and verify static logic operation. You will also measure propagation delays by using the oscilloscope.

2. Commercial NAND Gates

In this lab, you will be using the CMOS NAND gate family to construct logic circuits. In particular, you will be using the MM74HC00, a Quad NAND array (or the Quad NAND "chip").



NOTE : This is a **TOP VIEW**. The tiny "half circle" helps you orient the chip package to the diagram.

Figure 1. The MM74HC00

There are 4 NAND gates in one package (see connection diagram above), hence it is named "Quad NAND". Two special symbols require attention. One is the Vcc designation on pin 14; this is the power to the chip and is from +2 to +6V [1]. The other is GND on pin 7, where you will connect the circuit ground. The full data sheets are attached at the end of this document.

3. Normal Operation and Absolute Maximum Ratings

Please observe from the data sheets especially the Absolute Maximum Ratings.
In particular:

1) **The VCC pin CANNOT BE MADE NEGATIVE of ground**
2) **The inputs, Aor B CANNOT BE MADE NEGATIVE of ground**
3) **The inputs are NOT ALLOWED TO EXCEED V_{CC}**

[1] **DO NOT USE A NEGATIVE VOLTAGE OR A VOLTAGE VALUE HIGHER THAN +7 V**, **OTHERWISE YOU WILL DESTROY THE CHIP**.

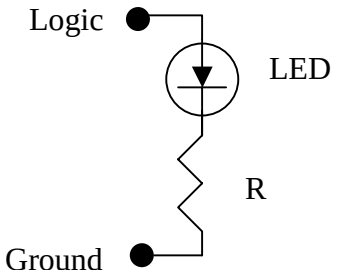
The latter caution is somewhat subtle and particularly easy to violate (burning out the chip). For example if you are studying normal operation at 5V you may be tempted to use logic levels of 0 and 5 V at the inputs. Now if you turn down V_{CC} and you continue to drive the inputs with a 5V logic signals, you will violate rule 3!!!! THEREFORE BE CAREFUL TO NEVER DRIVE THE INPUTS WITH VOLTAGES EXCEEDING V_{CC} .

Another feature to note from the data sheets is the dependence of the gate delay performance on V_{CC}. "Nominal worst case" operation is at V_{CC} = 4.5V (because that is the lower end of the nominal power supply range of 5V +/- 10%). But these devices are also designed to work at much lower values of V_{CC}, down to 2V. This provides a great opportunity to observe gate delays in a regime where they are very easy to measure.

Hands On

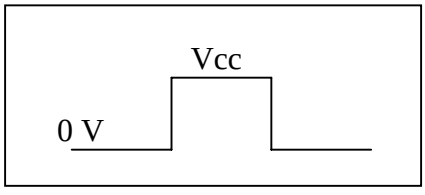
1. Logic detector circuit and its calibration

To detect the logic level of a given circuit node one can of course use a voltmeter or scope. But for static measurements it is attractive to have a simple visual indicator. You can build such a logic probe using an LED in series with a resistor. Note that the LED is a diode with a polarity (Hint: the longer leg is the positive end). You must orient it properly. The amount of current you need (typically from 1 to 10 mA) to be able to clearly see the LED light depends on the LED efficiency. The high current end is limited by the output of the NAND gate which is about 10mA at 5V. Assuming a diode drop of about 1.6 to 1.8V, a resistor in the range of 330 ohms may be adequate for the full voltage range, but you must test your detector for correct operation and adequate LED brightness over the range 2 to 5V. Observe the brightness and write it down in your report at 2V and 5V applied.



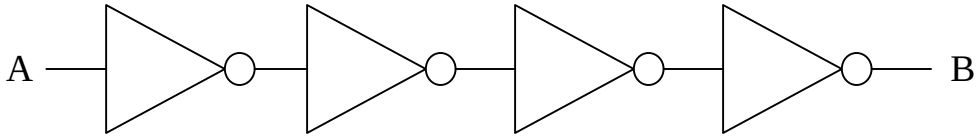
2. Single Gate Delay

Wire a single NAND gate as an inverter (by connecting the two inputs together). Use the function generator as input to the inverter. A 1k Hz square wave should work. Use the oscilloscope to make sure that the function generator output is a square wave of Vmin = 0V and Vmax = Vcc, otherwise the chip may be burned out (you will have to use an offset of Vpp/2 for the function generator). Next, use the oscilloscope to probe the input and output of the inverter, find any edge and zoom in to estimate the high-to-low and low-to-high transition delay. The delay is defined as the point where the input is 50% of its final value to the time the output is 50% of it's final value. Do this exercise for Vcc = 5V and Vcc = 2V.



Input

3. Inverter Chain



Now you can construct a chain of 4 inverters using the chip. This simple circuit will allow you to verify your static logic level detector and to calibrate your measurement of gate delay. On your "lab report" sheet draw the circuit diagram of the chain of inverters constructed using the MM74HC. (That means the top view of the MM74HC plugged into your prototype board and the wiring used to complete the circuit. HINT: no single pin on the package should be without at least one connection.). In this diagram you can show the internal wiring of the prototype board explicitly.

Verify the static operation of the chain of inverters for Vcc = 5V and Vcc = 2V.

Measure the delay of each inverter as previously, we are interested in the delay from the input to a given gate transition.

4. Digital Probes

Each of the oscilloscopes in the lab has digital probes that are perfect for measuring digital logic. Turn off the analog channels by hitting the A1 button and hitting the softkey that turns it off. Repeat for A2. Turn on the digital probes by pressing the D0 - D15 button in the digital section of the scope, you should notice softkey that activate either D0-D7 or D8 – D15. Each probe should be marked with a bit number, make sure the probes you are using are active. Use the probes to connect all the important signals of the chip (hint: important signals are inputs, outputs, and ground). Now the triggering must be set. Hit the pattern key, the Pattern line will appear that displays the triggering style for each bit. Each bit can be set to trigger on a different event; X signifies no triggering. Use the Select knob to find the input bit, you can tell what is active either by the highlighted bit number or Source on the bottom left of the screen, and trigger on the rising edge. The delay of each gate can be easily measured all at the same time, again using the time/div knob (notice the digital readout shows perfect square waves, you don't have to think about 50% levels its done by the scope). Using these delay values an estimate of the average gate delay can now be found.

$$\tau_{propagationdelay} = \frac{\tau_{low-to-high} + \tau_{high-to-low}}{2}$$

The average gate delay can also be found by noting the difference between the delay of gate 1 and gate 3. Once you have the propagation delay to gate 1 and to gate 3, you can determine the inherent propagation delay of each gate; delay = (delay 3 – delay 1)/2. This would give you a more accurate value of the propagation delay per gate because it eliminates the capacitance of probe.

Complete this exercise for Vcc = 5V and Vcc = 2V.

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