EECS 151/251A Homework 6

Due Friday, October 25th, 2019

Problem 1: Riscy Hazards [5 pts]

Assume the datapath is pipelined as such:

1. Assuming a 5-stage RISC-V processor pipeline without any forwarding implemented (like below), draw a pipeline table for the following code snippet. What is the CPI? Note that the table is just an example and is not complete.

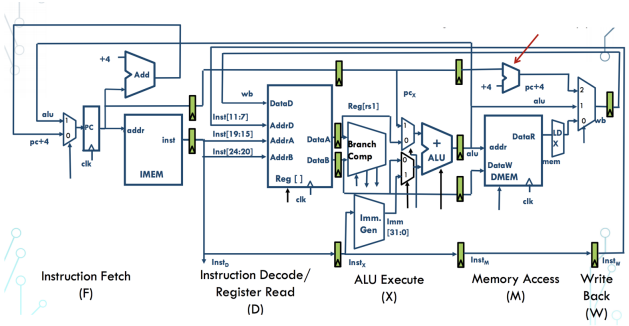


Figure 1: 5-stage pipeline

```
sub x3, x2, x4
add x1, x2, x3
add  x5, x4, x1
lw x1, 0(x2)
add x5, x4, x1
```

Cycle	IF	EX	WB
1	sub	-	-
2	add	sub	-

2. Now redraw the 5 stage pipeline with forwarding paths from the ALU output (as you've done in the past) as well as a new path from the output RD of the data memory block. How many cycles will the instructions take to execute? Are there any disadvantages from forwarding from the output of the data memory vs. from the pipeline register clocking RD?

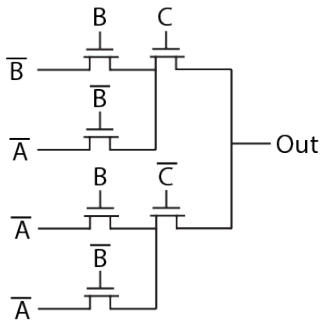
Problem 2: Complex CMOS gates [5 pts]

1. Implement the logic function $Y = \overline{AB + AC + BC}$ using a complementary pull-up and pull-down network. Remember to properly size the gates for equivalent worst-case pull-up and pull-down delays.

2. Now implement the logic function $Y = \overline{\overline{AB} + AC + BC}$. Can you have complementary pull-up and pull-down networks? Properly size the gates for equivalent worst-case pull-up and pull-down delays. Also what are the worst case output voltage limits assuming a threshold voltage, V_t.

Problem 3:Pass Gates and VTCs [5 pts]

1. Draw a truth table and derive the logic function based off the following pass gate circuit diagram.



2. Is this a static gate? Explain your reasoning.

3. Assuming $V_{dd} = 1V$, $GND = 0V$, $V_t = 0.2V$, and that each transistor acts like a perfect switch with an on resistance of R_{on} and infinite off resistance, AND that all inverted gate inputs are generated with ideal inverters with switching thresholds of 0.5 V, draw the voltage transfer characteristics of V_{out} as a function of A when B and C are 1 and 0, respectively.

4. Does the circuit go rail to rail? Draw a complimentary CMOS version of the original function. It's okay to use inverted signals as primary inputs.