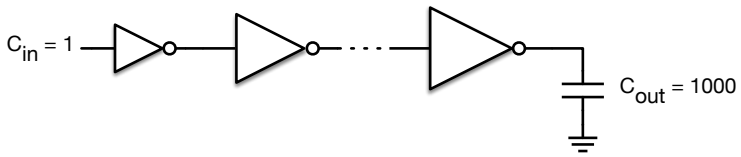
EECS 151/251A Homework 8

Due Friday, Nov 8th, 2019

Problem 1: Buffer Chain

Assume that we have the situation shown below with an inverter chain used to drive a large capacitive load (F = 1000) with minimal delay. How many buffers (inverter stages) would be optimal (or near optimal) in this case? What should be the fanout, f, be at each stage?



Solution:

We know from lecture that a simple, common choice of fanout is $f = 4$ close to the optimal for $\gamma = 1$. We also know that the fanout of each stage should be roughly equal. With that in mind, we can come up with the number of stages necessary:

$$\begin{aligned} f^N &= 1000 \\ N &= \log_f(1000) \\ &= 4.9829 \end{aligned}$$

We can't have fractional inverters, so we round this up to $N = 5$. Now we can determine the fanout of each stage again either (a) assuming that each stage is equal:

$$\begin{aligned} f &= \sqrt[5]{1000} \\ &= 3.9811 \end{aligned}$$

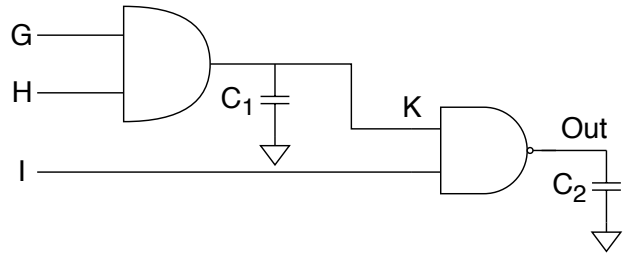
or (b) setting as many stages as possible to $f = 4$ and adjusting the last one, f':

$$\begin{aligned} f' &= 1000/4^4 \\ &= 3.9062 \end{aligned}$$

Problem 2: Transition Activity

Consider a 3-input NAND gate constructed from 2-input AND and NAND gates, as shown below. Assume that $C_2 = \frac{C_1}{4} = C$ and that there are no other capacitances in the circuit. The circuit is

driven by supply V_{DD} and frequency f. Each input has a probability of being high denoted P_X where X is G, H, I for the corresponding inputs.



a) Calculate the total power dissipation in terms of V_{DD}, f, P_G, P_H, P_I, and C.

Solution:

$$P = V_{DD}^2 \cdot f \cdot (\alpha_{1,0\to1} \cdot C_1 + \alpha_{2,0\to1} \cdot C_2)$$
$$P = V_{DD}^2 \cdot f \cdot C \cdot (4 \cdot \alpha_{1,0\to1} + \alpha_{2,0\to1})$$

$$\alpha_{1,0\to1} = (1 - P_A P_B) \cdot P_A P_B$$

$$\alpha_{2,0\to1} = P_D P_C \cdot (1 - P_D P_C)$$
$$\alpha_{2,0\to1} = P_A P_B P_C \cdot (1 - P_A P_B P_C)$$

$$P = V_{DD}^2 \cdot f \cdot C(4 \cdot (1 - P_A P_B) \cdot P_A P_B + P_A P_B P_C \cdot (1 - P_A P_B P_C))$$

b) What is the total power dissipation (in μW) of the circuit for $P_G = 0.7$, $P_H = 0.2$, $P_I = 0.5$? Assume that $V_{DD} = 1$, $f = 1GHz$, and $C = 10pF$.

Solution:

$$\alpha_{1,0\to1} = (1 - P_A P_B) \cdot P_A P_B = (1 - 0.7 \cdot 0.2) \cdot 0.7 \cdot 0.2 = 0.1204$$

$$\alpha_{2,0\to1} = P_A P_B P_C \cdot (1 - P_A P_B P_C) = 0.7 \cdot 0.2 \cdot 0.5 \cdot (1 - 0.7 \cdot 0.2 \cdot 0.5) = 0.0651$$

$$P = V_{DD}^2 \cdot f \cdot C \cdot (4 \cdot \alpha_{1,0\to1} + \alpha_{2,0\to1})$$
$$P = 1^2 \cdot 1G \cdot 10p \cdot (4 \cdot 0.1204 + 0.0651) = 5.467mW$$

c) For the same probabilities as part (b), suggest a more energy-efficient way of organizing the inputs. What is the power dissipation in this case?

Solution:

Ensure that the highest activity factor is placed on input C since that only affects the effective capacitance at the output. Thus, $P_C = 0.7$. The other two don't matter since the result is the same, so pick $P_A = 0.5$ and $P_B = 0.2$.

$$\alpha_{1,0\to1} = (1 - P_A P_B) \cdot P_A P_B = (1 - 0.5 \cdot 0.2) \cdot 0.5 \cdot 0.2 = 0.09$$

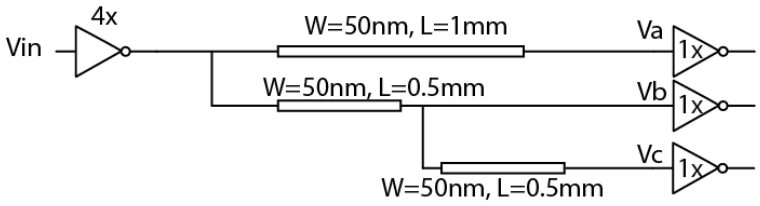
$$\alpha_{2,0\to1} = P_A P_B P_C \cdot (1 - P_A P_B P_C) = 0.5 \cdot 0.2 \cdot 0.7 \cdot (1 - 0.5 \cdot 0.2 \cdot 0.7) = 0.0651$$

$$P = V_{DD}^2 \cdot f \cdot C \cdot (4 \cdot \alpha_{1,0\to1} + \alpha_{2,0\to1})$$
$$P = 1^2 \cdot 1G \cdot 10p \cdot (4 \cdot 0.09 + 0.0651) = 4.251mW$$

Problem 3: Elmore Delay

For the following problem, $C_G = C_D = 2fF/\mu m$, the minimum sized (1x) inverter has $L = 0.1\mu m$, $W_p = 1\mu m$, $W_n = 1\mu m$ and for this technology $R_{n,on} = R_{p,on} = 10k\Omega/\square$ (i.e. the on resistance of a transistor with width W and length L is equal to $10k\Omega\frac{L}{W}$. Note that a 4x inverter has 4 times the width of a 1x inverter.

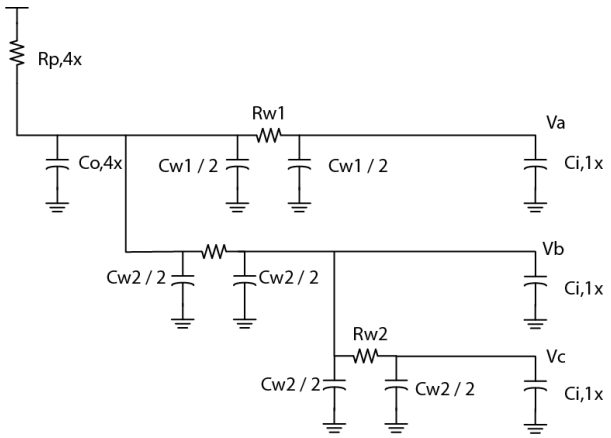
The wire has resistance $R_{wire} = 0.1\Omega/\square$, parallel plate capacitance $C_{pp} = 20aF/\mu m^2$ and the fringing capacitance per side of the wire is $C_{fr} = 14aF/\mu m$. The wire widths and lengths are shown in the diagram.



a) Using the π wire model, draw the equivalent RC model. What is the propagation delay from a step at V_{in} to V_a, V_b, and V_c.

Solution:

The equivalent RC circuit is:



For the 1x inverter:

$$R_{N,1x} = R_{P,1x} = 10k\Omega\frac{0.1\mu m}{1\mu m} = 1k\Omega$$
$$C_{i,1x} = C_{o,1x} = (1\mu m + 1\mu m) \cdot 2fF/\mu m = 4fF$$

For the 4x inverter:

$$R_{N,4x} = R_{P,4x} = R_{N,1x}/4 = 250\Omega$$
$$C_{o,4x} = 4 \cdot C_{o,1x} = 16fF$$

For the top wire:

$$R_{w1} = 0.1\Omega \cdot \frac{1000\mu m}{0.05\mu m} = 2k\Omega$$
$$C_{w1} = 20aF/\mu m^2 \cdot 0.05\mu m \cdot 1000\mu m + 2 \cdot 14aF/\mu m \cdot 1000\mu m = 29fF$$

For the next wire (and the one below that):

$$R_{w2} = 0.5 \cdot R_{w1} = 1k\Omega$$
$$C_{w2} = 20aF/\mu m^2 \cdot 0.05\mu m \cdot 500\mu m + 2 \cdot 14aF/\mu m \cdot 500\mu m = 14.5fF$$

The delay from the input to V_a is:

$$t_{p,a} = \ln 2 \cdot R_{w1} \cdot \left(C_{i,1x} + \frac{C_{w1}}{2}\right) +$$
$$\ln 2 \cdot R_{p,4x} \cdot \left(C_{i,1x} + \frac{C_{w1}}{2} + C_{i,1x} + \frac{C_{w2}}{2} + \frac{C_{w2}}{2} + \right.$$
$$\left. C_{i,1x} + \frac{C_{w2}}{2} + \frac{C_{w2}}{2} + \frac{C_{w1}}{2} + C_{o,4x}\right)$$
$$\rightarrow t_{p,a} = \ln 2 \cdot 58.5ps = 40.549ps$$

The delay from the input to V_b is:

$$t_{p,b} = \ln 2 \cdot \Big(R_{p,4x} \cdot \Big(C_{i,1x} + \frac{C_{w1}}{2} \frac{C_{w1}}{2} + \frac{C_{w2}}{2} + C_{o,4x} \Big) + \Big(R_{p,4x} + R_{w2} \Big) \cdot \Big(\frac{C_{w2}}{2} + C_{i,1x} + \frac{C_{w2}}{2} + \frac{C_{w2}}{2} + C_{i,4x} \Big) \Big)$$
$$\rightarrow t_{p,b} = \ln 2 \cdot 51.25ps = 35.52ps$$

The delay from the input to V_c is:

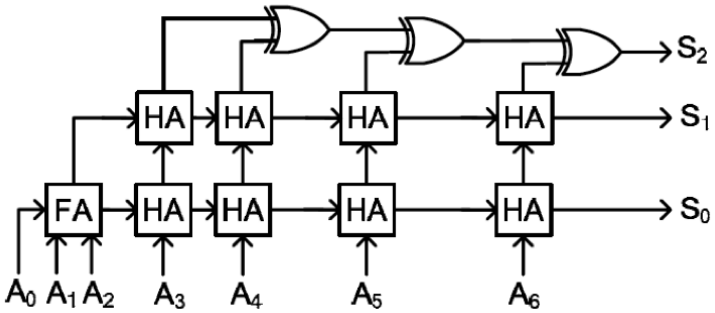
$$t_{p,c} = \ln 2 \cdot \Big(R_{p,4x} \cdot \Big(C_{i,1x} + \frac{C_{w1}}{2} + \frac{C_{w1}}{2} + \frac{C_{w2}}{2} + C_{o,4x} \Big) + \Big(R_{p,4x} + R_{w2} \Big) \cdot \Big(\frac{C_{w2}}{2} + C_{i,1x} + \frac{C_{w2}}{2} \Big) + \Big(R_{p,4x} + R_{w2} + R_{w2} \Big) \cdot \Big(\frac{C_{w2}}{2} + C_{i,1x} \Big) \Big)$$
$$\rightarrow t_{p,c} = \ln 2 \cdot 62.5ps = 43.32ps$$

b) What is the skew between pairs of V_a, V_b, and V_c? (i.e. what is the difference in arrival time between V_a and V_b, V_a and V_c, V_b and V_c?)

Solution:

$$t_{skew,ab} = |t_{p,b} - t_{p,a}| = 5.0253ps$$
$$t_{skew,ac} = |t_{p,c} - t_{p,a}| = 2.773ps$$
$$t_{skew,bc} = |t_{p,c} - t_{p,b}| = 7.798ps$$

Problem 4: Arithmetic



a) Explain the functionality of the circuit shown above. (FA stands for full-adder, HA stands for half-adder)

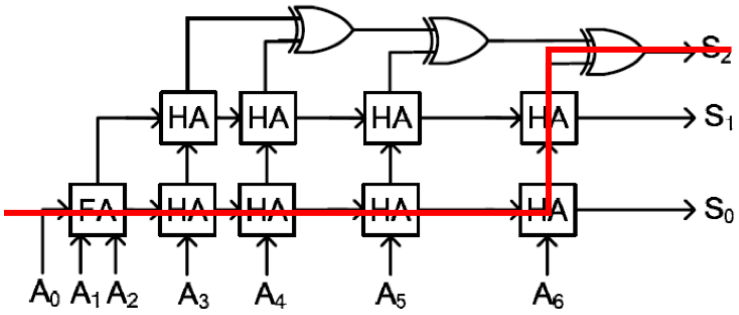
Solution:

The circuit adds together 7 1-bit binary numbers into one 3-bit output. The first row adds all 1-bit numbers together. All the carries are added by the second row. Finally, the XOR gates perfoms the final carry additions (remember that $s_i = a_i \oplus b_i$).

b) What is the critical path of the circuit? You may assume that each of the FA, HA and XOR blocks have a delay equal to t_{gate}. Show the critical path on the schematic.

Solution:

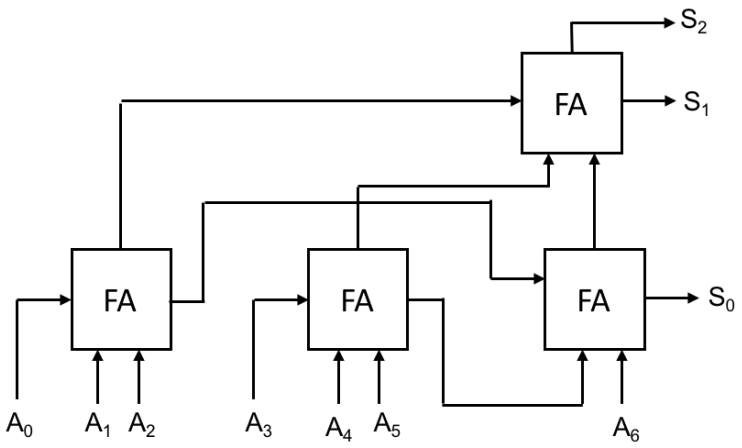
The critical path is $7 \cdot t_{gate}$, shown on the diagram below. Note that there are more than one critical paths in the circuit - any of them is correct, as long as its delay is $7 \cdot t_{gate}$.



c) Design a circuit with exactly the same functionality but shorter critical path. You are allowed to use FA, HA and XOR blocks.

Solution:

Since XORs, HAs and FAs are assumed to have the same delay, we can replace the half-adders with full adders in order to reduce hardware and the critical path, maintaining the same functionality. One example of how to make this circuit faster is shown below. The new critical path is $3 \cdot t_{gate}$.


S2
FA
S1
FA
FA
FA
S0
A0
A1
A2
A3
A4
A5
A6