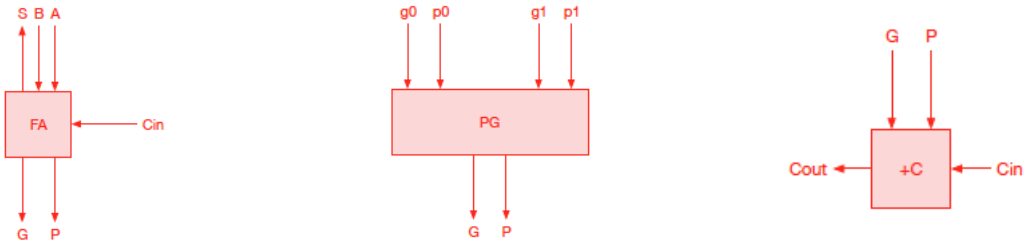
EECS 151/251A Homework 9

Due Monday , November 25th, 2019

Problem 1: Carry-Lookahead

In this problem, we would like to build an 8-bit carry-lookahead adder

a) You are given the following building blocks. Write down the expression for each building block.



(a) Full Adder (b) Propagate and Generate (c) Carry

Figure 1: CLA building blocks

b) Construct a 8-bit CLA adder with the building blocks, and highlight its critical path on the diagram.

c) Now we would like to build a 8-bit Kogge-Stone adder to optimize for delay. Again you are given the building blocks shown below. Notice that $P_{i:j}$ and $G_{i:j}$ denote the propagate and generate functions for a group of bits from i to j. Derive the expression for each building block.

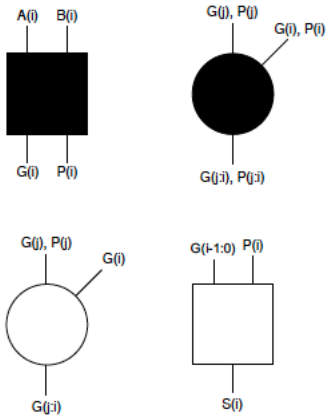


Figure 2: Building Blocks for Kogge-Stone Adder

d) Using the logic blocks, construct an 8-bit Kogge-Stone adder with a carry input and a carry output. User a radix-2 implementation, and highlight the critical path of your design. How does this compare to the previous design?

Problem 2: Multipliers

In this problem we will explore several structures of 4x4 multiplier. You are allowed to use Full Adders, Half Adders and AND gates.

a) Draw the array multiplier, and calculate its critical path using t_{carry}, t_{sum} and t_{and}.

b) Implement the same adder using the Carry-Save structure, and compute the new critical path.

c) Draw the wallace tree dot diagram, and implement the tree structure. What is the critical path now?

Problem 3: Latches/FF

1. Derive the truth table for the following circuit.

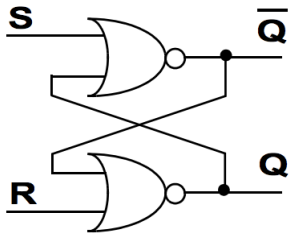


Figure 3: SR latch

2. This circuit can be used as a latch, but it has a potential problem. Explain why it can be used as a latch, and what is the problem?

3. We propose a solution for the problem above. Rederive the truth table for the structure below, and explained how it can be used as a latch.

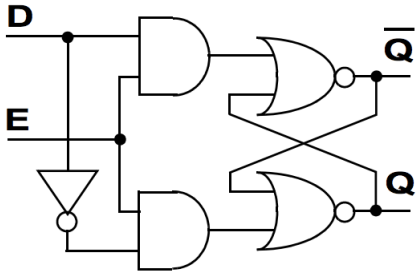


Figure 4: Transparent D latch

4. Finally, we have come up with the following flip-flop structure. Is this flip flop posedge triggered or negedge triggered?

5. In this structure, we call the first SR latch the master latch, and the later one slave latch. Assume Q was originally storing 0. When a 1 appears at D, describe what happens during one clock cycle.

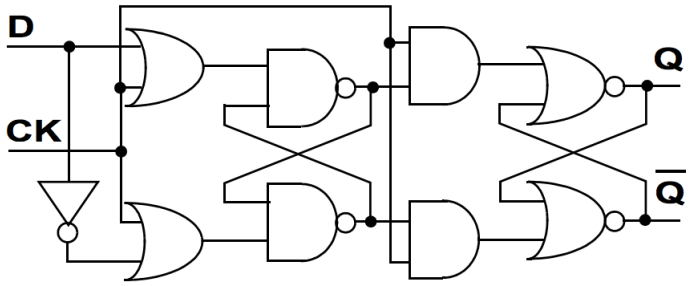


Figure 5: Master-slave flip flop

Problem 4: Timing

Consider the following logic function. The minimum and maximum delays of the logic modules are annotated on the figure. The flip-flops have the following timing properties: $t_{clk-q} = 50ps$, $t_{setup} = 50ps$, and $t_{hold} = 25ps$. You may assume that the clock has no jitter.

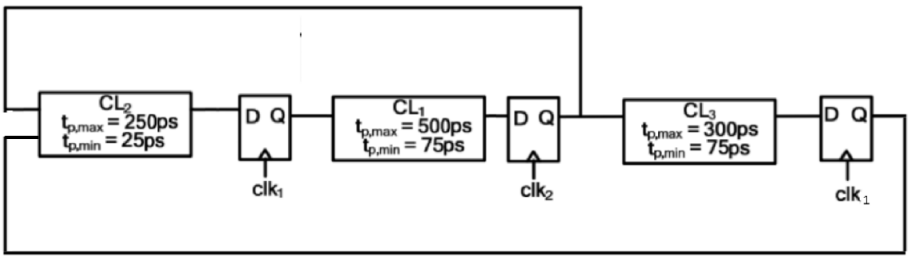


Figure 6: Circuit diagram

1. Assuming there is no skew between clocks, what is the minimum clock cycle time for this pipeline?
2. Under the condition established so far, does the circuit meet all hold time requirements?
3. Now assume that $clk1$ and $clk2$ can be randomly skewed relative to each other by up to +/- 60ps, what is the minimum clock cycle time? Does this solution cause hold time violations?

Problem 5: SRAM

Consider the 8T SRAM cell given below. With this design, there is a Write Word Line (WWL) that is used to write the values of Write Bit Line (WBL) and $\overline{WBL}$ into the cell, and a separate Read Word Line (RWL) that is used to read the content of the cell on the Read Bit Line (RBL)

1. Determine which transistors are involved in a Write operation, and comment on their relative sizing.
2. Determine which transistors are involved in a Read operation, and comment on their relative sizing.

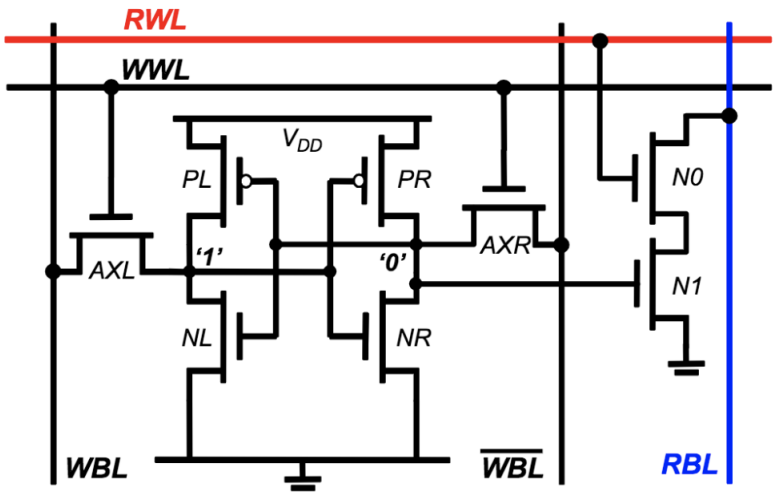


Figure 7: 8T SRAM

3. Compare this structure with the 6T SRAM cell. What are the advantages and disadvantages?

4. Qualitatively explain how increasing cell supply voltage (without changing other signal levels) affect the read stability, read access time and writability of the cell.