EECS 151/251A Homework 1

Due Friday, Sept 11^{th}, 2020

Problem 1: Dennard Scaling [4 pts]

Imagine that we still live in the world of ideal Dennard scaling. You designed a brilliant laptop microprocessor that runs at 4GHz, but dissipates 45W. What would be its power and performance in the next technology node, with features that are scaled by a factor of 0.8?

Solution:

$s = 0.8, \kappa = \frac{1}{0.8} = 1.25$

Delay improves by 1.25, so the max frequency can be $4 \cdot 1.25 = 5\,\text{GHz}$.

Power density remains the same, but power dissipation scales with s^2, so power dissipation is $45 \cdot (0.8)^2 = 28.8\,\text{W}$

Problem 2: Wafer Yield [4 pts]

You want to fabricate a new chip using TSMC's 5nm node. You will use 600 mm wafers with $\alpha = 3$ and a defect per unit area of $0.001\,/\text{mm}^2$. The die area is $1\,\text{cm}^2$ and the wafer cost is \$80k. What is your die yield and die cost?

Solution:

$$\text{Die Yield} = \left(1 + \frac{0.001\,/\text{mm}^2 \cdot 100\,\text{m}^2}{3}\right)^{-3} = 0.906$$

$$\text{Dies per wafer} = \frac{\pi \cdot (600\,\text{mm}/2)^2}{100\,\text{mm}^2} - \frac{\pi \cdot 600\,\text{mm}}{\sqrt{2 \cdot 100\,\text{mm}^2}} = 2700$$

$$\text{Die Cost} = \frac{\$80,000}{31000 \cdot 0.906} = \$32.70$$

Problem 3: Power and Energy [6 pts]

(a) Briefly explain why as a designer you would be concerned with the following. Give 2 reasons each. Think about the applications of your design. [1 pt each]

- Energy Consumption
- Power Consumption

(b) You find yourself are in charge of designing a battery and charger for a new laptop that dissipates 50W. If you expect this laptop to have 9 hours of battery life, how much energy (in Joules) must the battery hold at a full charge? [2 pts]

(c) To ensure that users can use the laptop while it charges, you decide that the laptop should charge from 0 to 100% in 2 hours if it is in use. How much power should the charger be able to supply for this to be possible? [2 pts]

Solution:

(a) Answers may vary. Examples of reasons are battery life and total cost of ownership.

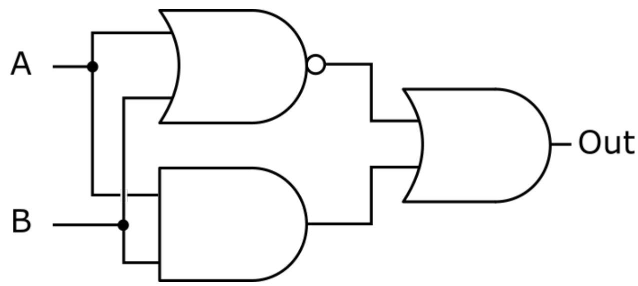
(b) Answers may vary. Examples of reasons are heating, cost of cooling.

(c) $Energy = Power \cdot Time = 50W \cdot 9h = 50W \cdot 32400s = 1,620kJ$

(d) $Power = Power\_to\_charge + Power\_to\_run = frac1,620kJ2 \cdot 3600s + 50W = 275W$

Problem 4. Boolean Logic [6 pts]

(a) For the digital logic circuit shown below, give the truth table. What is the equivalent boolean operation of this circuit? [3 pts]



(b) By inspection, draw the equivalent circuit for the given truth table using simple logic gates. You should not use more than 4 logic gates. [3 pts]

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

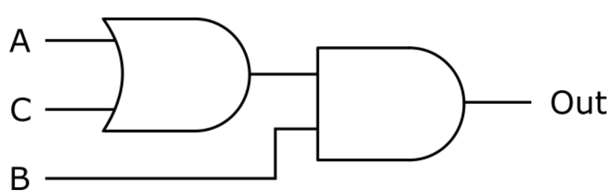
Solution:

(a) Truth Table

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

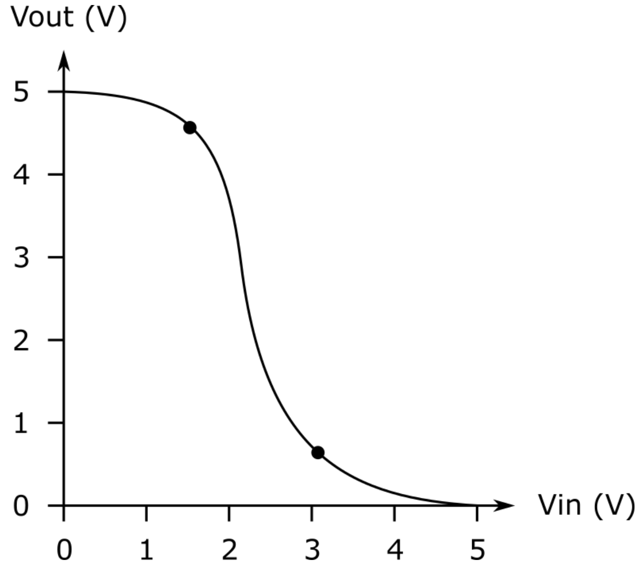
This is the XNOR boolean function.

(b) By inspection, `Out` is only 1 when `B` is 1 and either `A` or `C` is 1. An equivalent circuit for this is shown below:



Problem 5. Noise Margins [5 pts]

Estimate V_{OH}, V_{IH}, V_{OL}, V_{IL}, and the noise margins for the voltage transfer characteristic shown below. The dots along the line show roughly where the *slope* $= -1$.



Solution:

Will accept any answers within 0.25 of the following values.

$V_{OH} \approx 4.5$, $V_{IH} \approx 3.0$, $NM_H \approx 1.5$, $V_{OL} \approx 0.5$, $V_{IL} \approx 1.5$, $NM_L \approx 1.0$