EECS 151/251A Homework 3

Due Friday, Sept 25th, 2020

For this HW Assignment

You will be asked to write several Verilog modules as part of this HW assignment. You will need to test your modules by running them through a simulator. A useful tool is https://www.edaplayground.com, a free, online Verilog simulator.

For all problems, include your Verilog code, test bench, and test results (including the simulation output and a waveform). Also explain what aspects of your design are being verified by your testbench.

Problem 1: Logic Simplification [5 pts]

Take this truth table consisting of 4 input variables(A, B, C, D) and 1 output(Out):

A	**B**	**C**	**D**	**Out**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

1. Write a sum-of-products directly from the truth table. [1 pt]
2. Use a Karnaugh Map to simplify the logic and write the simplified sum-of-products and product-of-sums representations. [2 pts]
3. Using the simplified sum-of-products representation, draw the circuit that implements this function. Transform this circuit such that it is made up only of inverters and NAND gates. All gates should have 2 inputs and 1 output. [2 pts]

Problem 2: Combinational Logic [4 pts]

Consider the following Boolean function:

$$\bar{a}\bar{b}\bar{c}\bar{d} + \bar{a}\bar{b}\bar{c}d + \bar{a}\bar{b}cd + a\bar{b}d + \overline{(\bar{a} + \bar{b} + c)} + \overline{(\bar{a} + \bar{b} + \bar{c})}$$

(a) Use a K-map to simplify. Show your work. [1 pts]

(b) Use a Boolean algebra to simplify. Show your work. [1 pts]

(c) Using the simplified sum-of-products representation, draw the circuit that implements this function. Then bubble push to transform the circuit into products-of-sum form. All gates should have 2 inputs and 1 output. [2 pts]

Problem 3: FSM DNA sequencing[6 pts]

Help your TAs design a DNA sequencing machine! We want the machine to be able to detect some DNA sequences of bases(A, C, G, T) that we are interested in. The machine receives a one-hot encoded ACGT input every clock cycle, and outputs whether the sequence has been detected. `OUT` is pulled high for 1 clock cycle to indicate a pattern is detected, and then pulled low to prepare for the next match. The machine also has a `RESET` button that lets the user interrupt and start over at any time.

sequence to detect: `ACCTG`
inputs: `ACGT(4 bits), RESET(1 bit)`
output: `OUT`

(a) Draw the state diagram of this circuit, marking the transition conditions and output values. Your implementation should be in the style of a Moore machine. [1 pts]

(b) Write the Verilog that corresponds to your circuit in part a). Simulate your circuit using both the given and other sequences. Show the waveform. [2 pts]

(c) Draw the state diagram of this circuit as a Mealy state machine. [1 pts]

(d) Write the Verilog that corresponds to your circuit in part (c). Simulate your circuit using both the given and other sequences. Show the waveform. [2 pts]