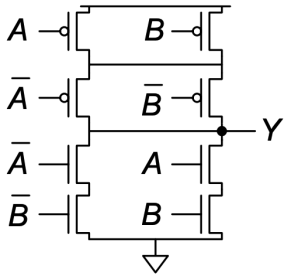
EECS 151/251A Homework 6

Due Friday, Oct 23rd, 2020

Problem 1: Complementary CMOS [8 pts]

(a) Write the simplified boolean expression for the function described by the CMOS circuit below. Hint: Writing a truth table with inputs A, B and output Y may make the answer more apparent. [2 pts]



Solution:

Using the PUN:

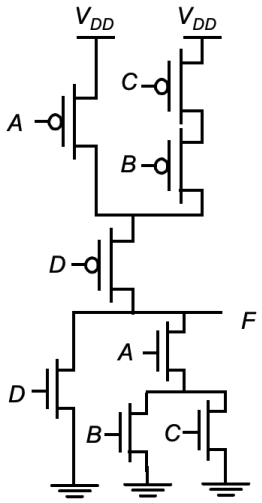
$$\begin{aligned} Y &= (\overline{A} + \overline{B}) \cdot (A + B) \\ &= \overline{A}\,A + \overline{A}\,B + \overline{B}\,A + \overline{B}\,B \\ &= 0 + \overline{A}\,B + \overline{B}\,A + 0 \\ &= \overline{A}\,B + \overline{B}\,A \\ &= A \oplus B \end{aligned}$$

Using the PDN:

$$\begin{aligned} Y &= \overline{\overline{A} \cdot \overline{B} + AB} \\ &= \overline{\overline{A} \cdot \overline{B}} \cdot \overline{AB} \\ &= (A + B) \cdot (\overline{A} + \overline{B}) \end{aligned}$$

Which can be simplified as above.

(b) Write the simplified boolean expression for the function described by the CMOS circuit below. [2 pts]



Solution:

Using the PUN:

$$Y = (\overline{A} + \overline{B}\,\overline{C}\,)\overline{D}$$

Using the PDN:

$$Y = \overline{A(B+C)+D}$$

(c) Implement the logic function $Y = \overline{A + BC}$ using a complementary pull-up and pulldown network. [2 pts]

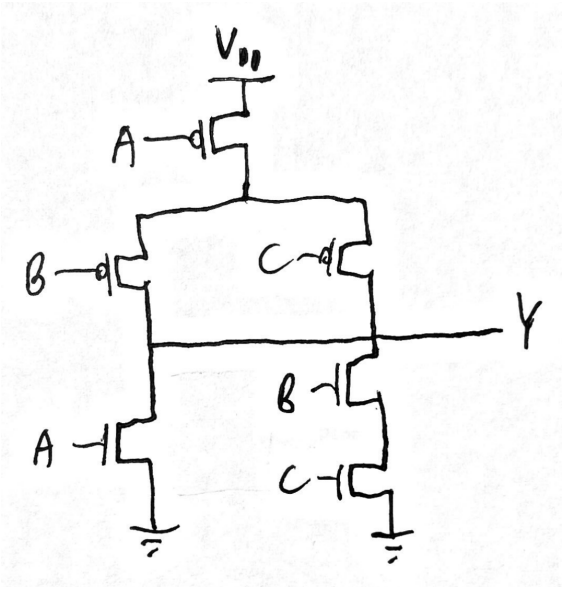
Solution:

Draw the PDN using $\overline{Y} = A + BC$. Use De Morgan's Law to draw the PUN:

$$Y = \overline{A + BC}$$

$$Y = \overline{A} \cdot \overline{BC}$$

$$Y = \overline{A}\,(\overline{B} + \overline{C}\,)$$



(d) Implement the logic function $Y = \overline{A(B+C) + \overline{B}\,C}$ using a complementary pull-up and pulldown network. For this question, assume you have $\overline{A}$, $\overline{B}$, and $\overline{C}$ available in addition to A, B, and C. [2 pts]

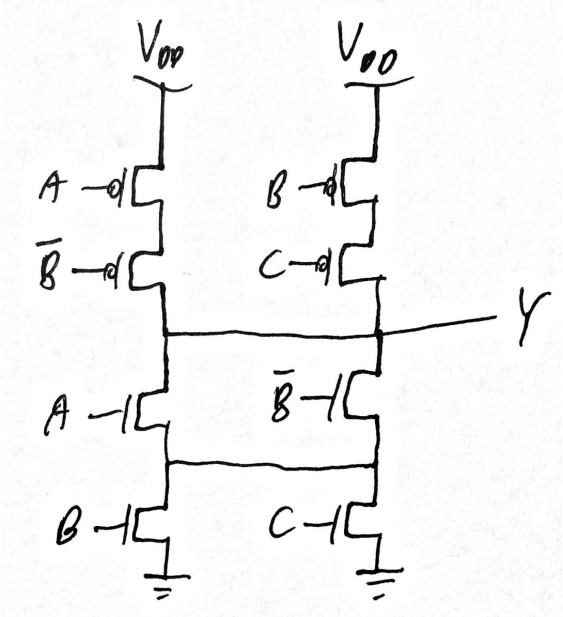
Solution:

First, simplify the expression (not required).

$$\begin{aligned}\overline{Y} &= A(B+C) + \overline{B}\,C \\ &= A(B+C) + 0 + \overline{B}\,C \\ &= A(B+C) + \overline{B}\,B + \overline{B}\,C \\ &= A(B+C) + \overline{B}\,(B+C) \\ &= (A+\overline{B}\,)(B+C)\end{aligned}$$

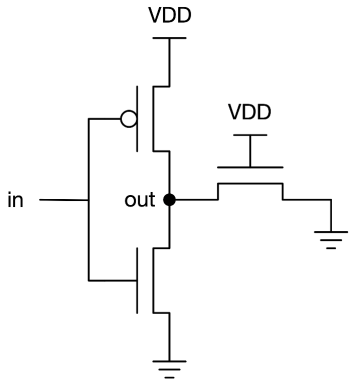
Then, use this to draw the PDN. To draw the PUN, use De Morgan's Law:

$$\begin{aligned}Y &= \overline{(A+\overline{B}\,)(B+C)} \\ &= \overline{(A+\overline{B}\,)} + \overline{(B+C)} \\ &= \overline{A}\,B + \overline{B}\,\overline{C}\end{aligned}$$


V_{DD}
V_{DD}
A
$\bar{B}$
B
C
Y
A
$\bar{B}$
B
C

Problem 2: Voltage Transfer Characteristic (VTC) [4 pts]

Using the transistor-as-a-switch model, draw the voltage transfer characteristic for the circuit below. You will eventually recognize this as half of a 6T CMOS SRAM bitcell. Assume that $|V_{th,p}| = V_{th,n} < V_{DD}/2$ and that $R_{on,p} = R_{on,n}$.



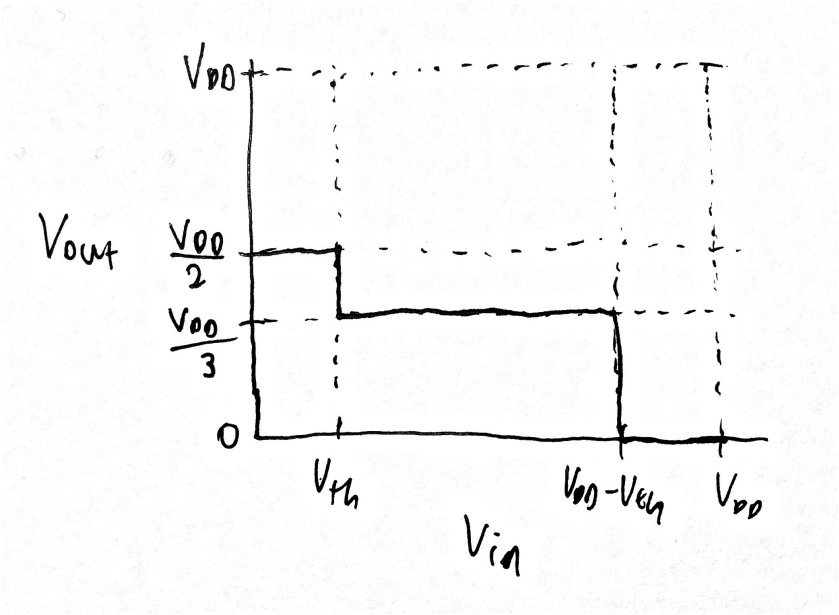
Solution:

With the transistor-as-a-switch model, we treat each transistor as having a constant resistance R_{on} while it is on.

The NMOS on the right can be treated as a resistor R_{on}, since its input is V_{DD}.

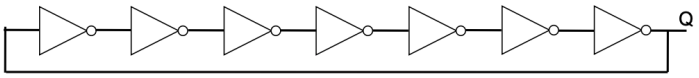
There are 3 possible situations:

1. $0 < V_{in} < V_{th}$: The top transistor is on and the bottom transistor is off. This creates a voltage divider between the top and right transistors, resulting in a V_{out} of $\frac{V_{DD}}{2}$.
2. $V_{th} < V_{in} < V_{DD} - V_{th}$: All transistors are on, creating a voltage divider with V_{DD} and R_{on} on one end, and GND and $\frac{R_{on}}{2}$ on the other end. This results in a V_{out} of $\frac{V_{DD}}{3}$.
3. $V_{DD} - V_{th} < V_{in} < V_{DD}$: The bottom and right transistors are on, so they both pass a V_{out} of GND.

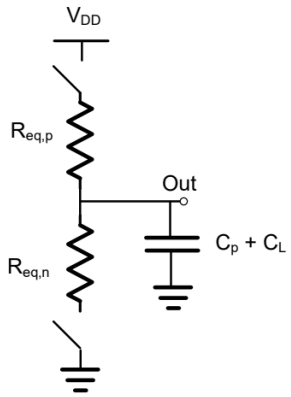

V_{DD}
V_{out}
$\frac{V_{DD}}{2}$
$\frac{V_{DD}}{3}$
0
V_{th}
$V_{DD}-V_{th}$
V_{DD}
V_{in}

Problem 3: Inverter Delay [3 pts]

By taking advantage of the fact that logic gates take some time to propagate changes in their input, we can build a simple ring oscillator (a circuit that switches back and forth between 0 and 1) from an odd number of inverters, as shown below. Suppose we use 7 inverters to do so.



For this question, we will use the model of a transistor as a resistor and a capacitor. Here is the diagram of an inverter under this model:



(a) Say $R_{eq,n} = R_{eq,p} = 5m\Omega$ and $C_P = C_{in} = 2nF$. What is the propagation delay of an inverter in this design? [2 pts]

Solution:

Each inverter's load capacitance, C_L, is equal to the following inverter's input capacitance C_{in}. Assuming each inverter has an ideal VTC (the switches switch at $V_{DD}/2$), the propagation delay is $ln(2)$ times the time constant τ.

$$\tau = R_{eq}(C_P + C_L) = (5\ \text{m}\Omega)(2\ \text{nF} + 2\ \text{nF}) = 20\ \text{ps}$$

$$t_p = ln(2)\tau \approx 0.7(20\ \text{ps}) = 14\ \text{ps}$$

(b) At what frequency will the output signal oscillate? Assume Q is not connected to anything outside the ring. [1 pt]

(Note: Our solution here is easy to find because the inverters are connected in a loop. As you will find, this problem becomes more complicated when the chain of inverters is connected to a different circuit.)

Solution:

T, the period of the oscillation, is how long it takes for all 7 inverters to switch from 0 to 1 and back to 0.

$$T = 2 \cdot 7t_p = 14t_p$$

$$f = \frac{1}{T} = \frac{1}{14t_p} \approx \frac{1}{196\,\text{ps}} \approx 5.1\,\text{GHz}$$