EECS 151/251A Homework 7

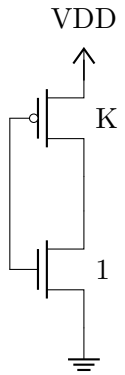
Due Friday, Oct 30th, 2020

Problem 1: RC Delay and Logical Effort Basics

Take a CMOS inverter in a process where $\gamma = \frac{C_d}{C_g}$ ($\gamma = 1$ in lecture), and the PMOS effective on-resistance is equal to K times that of the NMOS (i.e. $R_p = K \cdot R_n$, $K = 1$ in lecture) for minimally sized transistors.

(a) Draw the inverter at the transistor-level and size each FET for equal pull-up and pull-down strength. Assume the NMOS is of size '1', normalized to the minimum width of the process.

Solution:



(b) Write down the delay of this unloaded inverter using RC time constants in terms of γ, R_n, and C_g. Call this delay $t_{parasitic}$. Assume input step transitions.

Solution:

$$\begin{aligned} t_{parasitic} = \ln(2) \cdot R_{eq} \cdot C_{eq} &= \ln(2) \cdot R_n \cdot (C_{d,n} + C_{d,p}) \\ &= \ln(2) \cdot R_n \cdot (\gamma C_g + K\gamma C_g) \\ &= \ln(2) \cdot R_n \cdot (K+1)\gamma C_g \end{aligned}$$

(c) Now let the inverter have a load of C_L attached to its output. Call the quantity $f = C_L/C_{in}$. Write the delay of the inverter in terms of γ, $t_{parasitic}$, and f.

Solution:

$$
\begin{aligned}
C_{in} &= (W_p + W_n) \cdot C_g = (K+1) \cdot C_g \\
t_{inv,loaded} &= \ln(2) \cdot R_n \cdot (\gamma C_g + K\gamma C_g + C_L) \\
&= \ln(2) \cdot R_n \cdot (C_g\gamma(K+1) + C_L) \\
\text{Multiplying by } \frac{C_{in}}{C_{in}} &: = \ln(2) \cdot R_n(K+1)C_g \cdot (\gamma + \frac{C_L}{C_{in}}) \\
&= \frac{t_{parasitic}}{\gamma} \cdot (\gamma + f)
\end{aligned}
$$

We notice that the delay isn't affected by K, as expected. We also see a linear relation between inverter loading and delay.

No matter how we large we size the inverter, its intrinsic delay is always the same, but a larger inverter is able to drive a large external load faster, at the expense of increasing its input capacitance.

In the lecture slides we call the quantity $\frac{t_p}{\gamma}$ as t_{inv} which is treated as a process constant.

(d) Recall that the gate delay for any CMOS gate can be expressed as:

$$t_{p,gate} = \tau_{inv}(p + f \cdot LE)$$

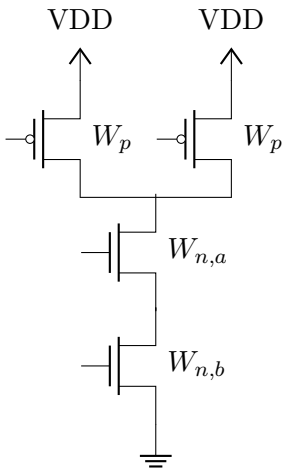
where τ_{inv} is a process constant, p is the intrinsic delay of the gate, and LE is the logical effort of the gate.

What are these values for an inverter?

Solution:

$$
\begin{aligned}
\text{Comparing the equation from above: } t_{inv} &= \frac{t_p}{\gamma} \\
p_{inv} &= \gamma \\
LE_{inv} &= 1
\end{aligned}
$$

(e) Take the following sizing of a NAND2 gate. What is W_p for inverter equivalent delay? Prove that $W_{n,a} = W_{n,b} = 2$ so the gate has equivalent self-loaded delay to an inverter and consumes minimal area.



Solution:

$$W_p = K \text{ for equivalent inverter pull-up strength}$$
$$\text{Area } = W_{n,a} + W_{n,b}$$
$$R_{n,a} + R_{n,b} = R_{inv} \rightarrow \frac{R_n}{W_{n,a}} + \frac{R_n}{W_{n,b}} = R_n$$
$$\text{This relation must hold: } W_{n,a} + W_{n,b} = W_{n,a} \cdot W_{n,b}$$

We can then show that to minimize area under the constraint, $W_{n,a} = W_{n,b} = 2$.

(f) Find the logical effort of this NAND2 gate for both inputs. What happens to the LE as K increases, and why does it make intuitive sense?

Solution:

The LE of a gate sized such that it has inverter-equivalent pull-up and pull-down strength is:

$$LE_{gate} = \frac{C_{in,gate}}{C_{in,inv}}$$
$$LE_{nand2} = \frac{KC_g + 2C_g}{KC_g + C_g} = \frac{K+2}{K+1}$$

We notice that as K increases, the LE tends towards 1. This can be intuitively understood as the minimal inverter's PMOS needing ever increasing upsizing, which decreases the relative difference between the inverter and NAND2 input capacitance.

(g) What is the intrinsic delay of a NAND2 gate (i.e. find p_{NAND2})? Make the assumption that $K = 2$.

Solution:

$$
\begin{aligned}
t_{NAND,RC,loaded} &= t_{NAND,gate,delay,equ} \\
\ln(2) \cdot R_n \cdot (6C_g\gamma + C_L) &= \ln(2) \cdot R_n \cdot 3 \cdot C_g(p_{NAND2} + \frac{4}{3}f) \\
3(2\gamma + \frac{C_L}{3C_g}) &= 3(p_{NAND2} + \frac{4}{3}f) \\
2\gamma + \frac{4}{3}f &= p_{NAND2} + \frac{4}{3}f \\
p_{NAND2} &= 2\gamma
\end{aligned}
$$

Problem 2: Complementary CMOS

(a) Design a complex CMOS logic gate that implements the function below:

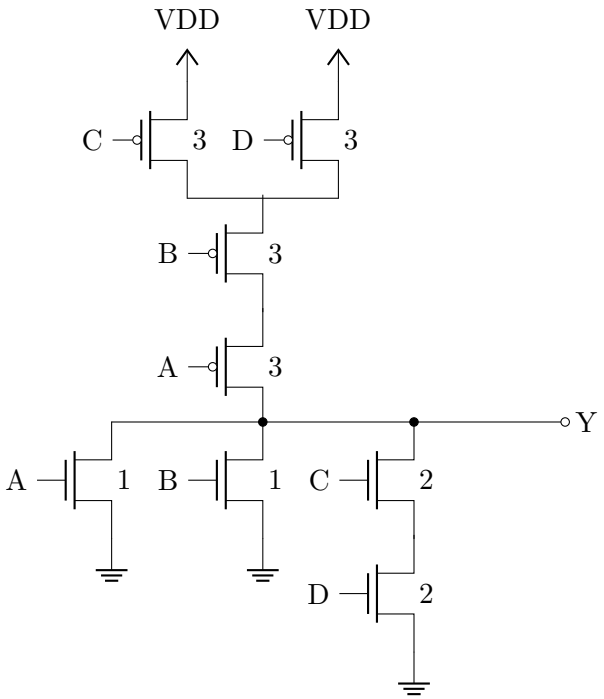
$$Y = \overline{(A+B)} \cdot \overline{CD} \tag{1}$$

(b) You are using a modern technology in which a minimum sized inverter has PMOS with width 1 and NMOS with width 1 ($R_{ON,PMOS} = R_{ON,NMOS}$). Size your design in (a) and try to minimize the overall area. Assume the total area is proportional to the sum of transistors' width.

Solution:

Use De Morgan's law:

$$\begin{aligned} Y &= \overline{(A+B)} \cdot \overline{CD} \\ &= \overline{A+B+CD} \end{aligned} \tag{2}$$



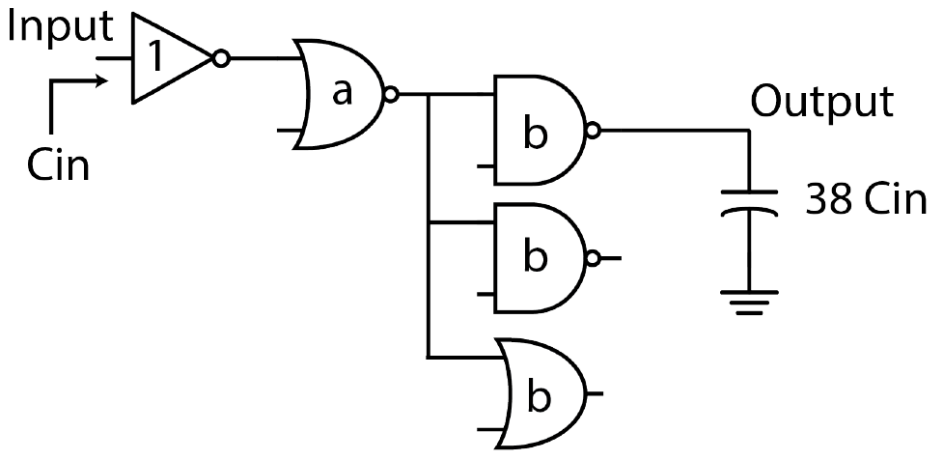
(c) Calculate the logic effort for input A and C with the assumptions in (b).

Solution:

$$LE_A = \frac{3+1}{2} = 2$$
$$LE_C = \frac{3+2}{2} = 2.5$$

Problem 3: Path delay with logical effort

For this problem, assume you have a reference inverter with $W_P = W_N = 1$. This technology has $\gamma = 1.2$



(a) Determine the path effort from input to output, and optimal stage effort for the circuit shown above. Note that a and b are the input capacitance of each input.

Solution:

$$FO_{path} = \frac{38C_{in}}{C_{in}} = 38$$
$$LE_{path} = 1 \times \frac{3}{2} \times \frac{3}{2} = \frac{9}{4} = 2.25$$
$$B_{path} = 1 \times 3 \times 1 = 3$$
$$PE = FO_{path} \cdot LE_{path} \cdot B_{path} = \frac{513}{2} = 256.5$$
$$SE_* = \sqrt[3]{PE} = \sqrt[3]{\frac{513}{2}} \approx 6.35$$

(b) Find the optimun a and b in terms of C_in for minimum delay in the critical path (input to output).

Solution:

$$b = \frac{38C_{in}}{SE_*} \cdot 1.5 \cdot 1 \approx 8.98C_{in}$$
$$a = \frac{b}{SE_*} \cdot 1.5 \cdot 3 \approx 6.35C_{in}$$

Full credit if using a=6.35, b=8.98