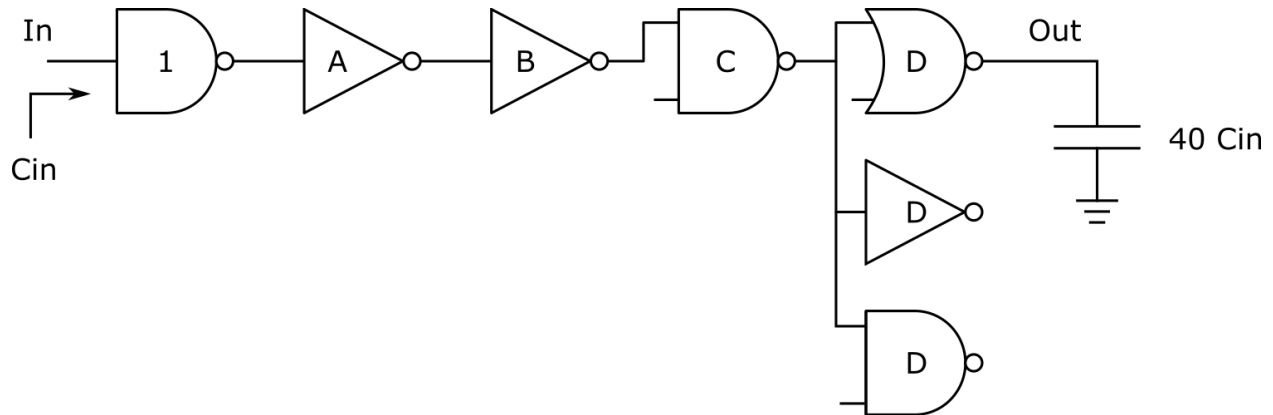# EECS 151/251A Homework 8

Due Friday, Nov 6th, 2020

Problem 1: Path delay with logical effort [10 pts]

For this problem, assume you have a reference inverter with $W_P = W_N = 1$. This technology has $\gamma = 1.5$

(a) Determine the path effort from input to output, and optimal stage effort for the circuit shown above. Note that A, B, C, and D are the input capacitances of each gate.

(b) Find the optimum A, B, C, and D in terms of C_{in} for minimum delay in the critical path (input to output).

(c) Consider the case where out output load is increased to $C_{out} = 60 * C_{in}$. To achieve the shortest path delay, is it better to add stages (two inverters in series) or to resize the current stages? If adding stages is the better option, where should they be inserted, and how should they be sized? If resizing the existing stages is better, what should the new sizing be?

Problem 2: Elmore Delay [8 pts]

For the following problem, $C_G = C_D = 2fF/um$, the minimum sized (labeled as 1x in the picture) inverter has $L = 0.1um$, $W_p = 2um$, $W_n = 1um$ and for this technology $R_{n,on} = 10k\Omega/sq.$ (i.e. the resistance of an NMOS with width W and length L is equal to $10k\Omega\frac{L}{W}$) and $R_{p,on} = 20k\Omega/sq.$ (i.e. the resistance of a PMOS with width W and length L is equal to $20k\Omega\frac{L}{W}$). Note that a 6x inverter has 6 times the width of a 1x inverter

For the wire, $R_{wire} = 0.1\Omega/sq.$, the parallel plate capacitance is $C_{pp} = 20aF/um^2$ and the fringing capacitance per each side of wire is $C_{fr} = 14aF/um$. The wire widths and lengths are shown in the picture.
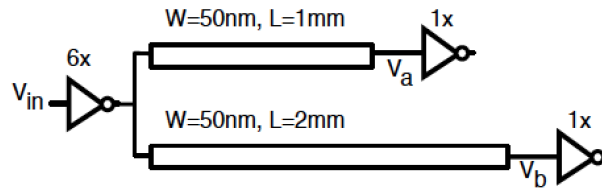
(a) Using the π wire model, draw the equivalent RC switch model. What is the propagation delay from a step at Vin to Va and Vb?

(b) What is the skew (difference in arrival time between Va and Vb)?

Problem 3: Power, Energy, and Performance [12 pts]

151Laptops & Co. is producing a new line of computers tailored for specific workloads. They've come to you for advice on how to optimally configure their processors for each target workload.

The processor for each of these machines will be based on the company's newest RISC-V Core. This base core has been designed to run at a frequency of 3.8 GHz with a supply voltage of 1.0 V. The core has a total capacitance load of approximately 60nF. The design team has also informed you that by raising the supply voltage to 1.3V, the core can be overclocked to run at 4.4GHz. You can alternatively connect two cores together to build a multicore processor. The extra logic required to connect the cores adds 5nF of capacitance load. A characterization team has found that over a number of benchmarks, the average switching rate of gates never exceeds 10%. Use this worst case value in your calculations.

a. How much power does the base core consume?

b. How much power does the single overclocked core configuration consume?

c. How much power does the multicore configuration consume?

d. The first custom machine targets graphic design and rendering workloads. The characterization team has benchmarked these workloads and found that 70% is parallel, and 30% is

sequential. What configuration of the processor has the best throughput? What is its speedup over the base core?

e. How efficient is each configuration: how much energy does each configuration consume to run the workload? You can leave this answer in terms of the time it takes the base core to run the workload t_b.

f. Repeat (d) and (e) for a workload where only 20% the workload is parallel.