EECS 151/251A Homework 9

Due Friday, Nov 20$^{\text{th}}$, 2020

Problem 1: Adders

a) Draw the block diagram of an 8-bit ripple carry adder and an 8-bit carry-lookahead adder. For each, derive the critical path in terms of the following constants. Use only 2-input gates. Include the final carry-out bit.

$t_{MUX} = 6ps$
$t_{OR} = 5ps$
$t_{AND} = 4ps$
$t_{XOR} = 6ps$

b) Now derive, generally, the critical path and area for an N-bit ripple-carry adder and an N-bit carry-lookahead adder. It is okay to make approximations for cases where $\sqrt{N}$ or $log_2(N)$ are not integers. Use only 2-input gates and include the final carry-out bit.

Problem 2: Tree Adders

The goal of this problem is to design a 10-bit Kogge-Stone adder optimized for delay:

a) Design the following logic blocks at a gate level. You may draw the gates or write the Boolean functions. Use the given inputs and outputs as hints.

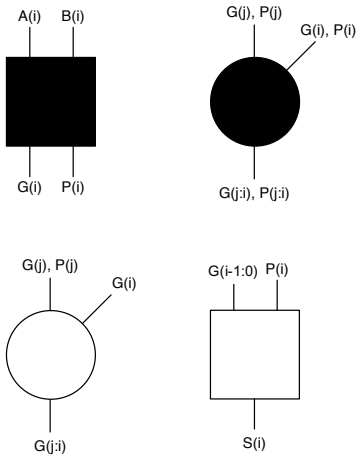

Figure 1: Building Blocks for Kogge-Stone Adder

b) Using the logic blocks you designed in part (a), design a 10-bit logarithmic adder with a carry

input and a carry output. Use a radix-2 Kogge-Stone implementation. Highlight the critical path of your design? Give a block-level estimate, assuming that more complex blocks have more delay.

Problem 3: Multipliers

a) Draw a 5 x 5 Carry-Save multiplier and compute the critical path using t_{carry}, t_{sum} and t_{and}.

b) Draw a wallace tree for a 5 x 5 multiplier using Full Adder and Half Adder cells. What is the critical path?

Problem 4: Latches & Flip-flops

Consider the latch design shown below. You may assume that the inverters are symmetrical with input capacitance C, self-loading capacitance also C and equivalent driving resistance R. The transmission gate is sized to have an equivalent resistance R and parasitic capacitance C on each side.

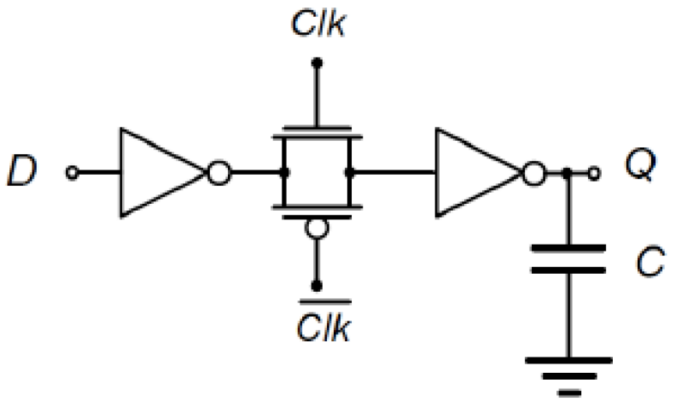

Figure 2: Dynamic Latch

a) Calculate the Clk-Q and D-Q delays as a function of R and C of this latch. In each case, show the equivalent RC circuit and explain.

b) What is the approximate setup time for this latch? Explain your answer.

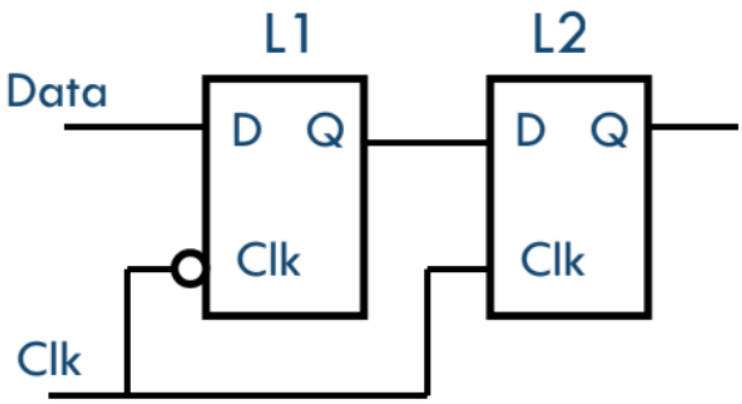

Figure 3: flip-flop

c) We build a flip-flop(figure 3) with two dynamic latches. Is the flip-flop positive-edge triggered or negative-edge triggered?