Intel Unveils Second-Generation Neuromorphic Chip

October 5, 2021, Intel has unveiled its second-generation neuromorphic computing chip, Loihi 2, the first chip to be built on its Intel 4 process technology. Designed for research into cutting-edge neuromorphic neural networks, Loihi 2 brings a range of improvements. They include a new instruction set for neurons that provides more programmability, allowing spikes to have integer values beyond just 1 and 0, and the ability to scale into three-dimensional meshes of chips for larger systems.

Intel's Loihi 2 second-generation neuromorphic processor. (Source: Intel)
Review

• Core FPGA building blocks:
  • Configurable Logic Blocks (CLBs)
  • Configurable Interconnect
    • Switch boxes

• Modern FPGA Designs:
  • BRAMs, DSPs, and AI Engines

• CMOS process is used for producing chips
  • Planar bulk process used up to 28nm node
  • finFET and FDSOI used below the 22nm node
MOS Transistors
MOS Transistors

- **Symbol**

N-type NMOS

- **Devices are symmetrical**
  - NMOS: Drain is at higher voltage
  - PMOS: Source is at higher voltage

- **W/L**

- **Contacts**

  - Polysilicon (or metal)

  - Source (S)
  - Drain (D)

- **N+ diffusion**

- **Gate oxide**

- **Contacts**

  - Gate (G)

- **P+ diffusion**

  - P-type PMOS
Different Kinds of MOS Transistors

- **Planar bulk CMOS**

  N-type NMOS

- **FinFET**

  Intel 10nm IEDM 2017

  Fin Width = $T_{Si}$

  Fin Height $H_{FIN}$

  W is discrete!
Transistor Dimensions are Quantized

- FinFET widths are discrete \( W = kW_{\text{unit}} \)
  - \( k \) is an integer

- Lengths are quantized because of lithography
  - Also are quantized lower metal layers, contacts...
Ohm’s Law

• Resistors

\[ R \]

\[ I \]

\[ V \]

\[ I = \frac{V}{R} \]

• Variable resistors

\[ R \]

\[ I \]

\[ V \]

\[ I = \frac{V}{R} \]

• Physical resistors

\[ R = \rho \frac{L}{TW} \]

• In a planar process, designer controls \( W \) and \( L \)
Series and Parallel

• With two identical resistors, $R$

$$R_{\text{series}} = 2R$$

Equivalent to doubling length

$$R_{\text{parallel}} = R/2$$

Equivalent to doubling width
An n-Channel MOS Transistor

- **$V_D = 0V$**
- **$V_G = 0V$**
- **$V_S = 0V$**

- Polysilicon gate, dielectric, and substrate form a capacitor.

- When $V_{GS} < V_{Th}$ transistor is off

$V_D > 0$, transistor leaks

**$V_{DS} > 0$, $I_{DS} \sim nA$**
An n-Channel MOS Transistor

When $V_{GS} < V_{Th}$ transistor is off

When $V_{GS} > V_{Th}$, small region near the surface turns from p-type to n-type.

Current is proportional to $V_{DS}$
An n-Channel MOS Transistor

\[ V_D > 0 \]

\[ V_{GS} > V_{Th} \]

\[ V_S = 0V \]

\[ V_{DS} \text{ and } V_{GS} \text{ change } I_{DS} \]

\[ V_{GD} < 0 \]

\[ V_{G} > V_{Th} \]

\[ V_S = 0V \]

\[ V_{GD} < V_{Th} \text{ transistor saturates } \]

\[ (V_{DS} > V_{GS} - V_{Th}) \]
MOS Transistors

- NMOS Transistor I-V characteristics

Old transistor

\[ I_D \sim K(V_{GS} - V_{Th}) \]

\[ V_{GS} = V_{DD} \]
\[ V_{GS} = 0 \]

\[ V_{DS} \]

\[ I_D \]

\[ V_{GS} \]

Nearly linear

Variable resistor!

~7nm transistor
Velocity Saturation

• Carrier velocity in the channel saturates

  Velocity linearly proportional to \( E \), \( v = \mu E \)

  Velocity saturated at \( v \approx 10^5 \text{ m/s} \)
  (for fields > 1V/m)

• All submicron transistors are velocity saturated

• Other effects (drain-induced barrier lowering) cause \( I_{DS} \) to increase in saturation
Administrivia

• Homework 5 will be posted later this week, due next week

• No lab this week
  • Lab 6 (last) after the midterm

• Midterm 1 on October 7, 7-8:30pm
  • You will be assigned a classroom
  • One double-sided page of notes allowed
  • Material includes FPGAs
MOS Transistor as a Switch
• $V_{GS}$ controls the switch
  • (it also charges the channel capacitor)
ON/OFF Switch Model of MOS Transistor

\[ |V_{GS}| < |V_T| \]

\[ |V_{GS}| \geq |V_T| \]

\[ R_{on} \]
A More Realistic Model

- It is a dimmer!

\[ |V_{GS}| < |V_T| \]

\[ |V_{GS}| > |V_T| \]
A Logic Perspective

NMOS Transistor

\[ V_{GS} > V_{Th} \]

\( Y = B \) if \( A = 1 \)

PMOS Transistor

\[ V_{GS} < V_{Th} \]

\( Y = B \) if \( A = 0 \)
AND and OR

• AND

\[ F = AB \]
\[ (F = AB + \overline{A} \cdot 0) \]

• OR

\[ F = A + B \]
\[ (F = A \cdot 1 + \overline{A}B) \]

• Keep in mind – single NMOS/PMOS transistors are imperfect switches!

• Turns off when \(|V_{GS}| = |V_{Th}|\)
Peer Instruction

• Switch logic

• Which combination of inputs implements $F = AB$?

<table>
<thead>
<tr>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
</tr>
</thead>
<tbody>
<tr>
<td>a)</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>b)</td>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>c)</td>
<td>1</td>
<td>0</td>
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<td>d)</td>
<td>1</td>
<td>1</td>
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<tr>
<td>e)</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>f)</td>
<td>None of the above</td>
<td></td>
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</tbody>
</table>
Summary

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